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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m120ansp-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m120ansp-u0</a>

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

**Table 1.2 R8C/M11A Group Register Settings**

Related Function	Register Name	Address	Bit	Setting Method for Access
INT3	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
KI0	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

### 1.1.3 Specifications

Tables 1.3 and 1.4 outline the Specifications.

**Table 1.3 Specifications (1)**

Item	Function	Description
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> <li>• Number of fundamental instructions: 89</li> <li>• Minimum instruction execution time:               <ul style="list-style-type: none"> <li>50 ns (<math>f(XIN) = 20\text{ MHz}</math>, <math>VCC = 2.7\text{ V to }5.5\text{ V}</math>)</li> <li>200 ns (<math>f(XIN) = 5\text{ MHz}</math>, <math>VCC = 1.8\text{ V to }5.5\text{ V}</math>)</li> </ul> </li> <li>• Multiplier: 16 bits <math>\times</math> 16 bits <math>\rightarrow</math> 32 bits</li> <li>• Multiply-accumulate instruction: 16 bits <math>\times</math> 16 bits + 32 bits <math>\rightarrow</math> 32 bits</li> <li>• Operating mode: Single-chip mode (address space: 1 Mbyte)</li> </ul>
Memory	ROM, RAM, data flash	See <b>Table 1.5 Product List</b> .
Reset sources		<ul style="list-style-type: none"> <li>• Hardware reset by <math>\overline{\text{RESET}}</math></li> <li>• Power-on reset</li> <li>• Watchdog timer reset</li> <li>• Software reset</li> <li>• Reset by voltage detection 0</li> </ul>
Voltage detection	Voltage detection circuit	Voltage detection with two check points: Voltage detection 0, voltage detection 1 (detection levels selectable)
Watchdog timer		<ul style="list-style-type: none"> <li>• 14 bits <math>\times</math> 1 (with prescaler)</li> <li>• Reset start function selectable</li> <li>• Count source protection function selectable</li> <li>• Periodic timer function selectable</li> </ul>
Clock	Clock generation circuits	<ul style="list-style-type: none"> <li>• 3 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator</li> <li>• Oscillation stop detection: XIN clock oscillation stop detection function</li> <li>• Clock frequency divider circuit integrated</li> </ul>
Power control		<ul style="list-style-type: none"> <li>• Standard operating mode</li> <li>• Wait mode (CPU stopped, peripheral functions in operation)</li> <li>• Stop mode (CPU and peripheral functions stopped)</li> </ul>
Interrupts		<ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External interrupt inputs: 8 (<math>\overline{\text{INT}} \times 4</math>, key input <math>\times 4</math>)</li> <li>• Priority levels: 2</li> </ul>
I/O ports	Programmable I/O ports	<ul style="list-style-type: none"> <li>• CMOS I/O: 17 (pull-up resistor selectable)</li> <li>• High-current drive ports: 8</li> </ul>
Timer	Timer RJ2	16 bits $\times$ 1 Timer mode, pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2	8 bits $\times$ 1 (with 8-bit prescaler) or 16 bits $\times$ 1 (selectable) Timer mode, programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits $\times$ 1 (with 4 capture/compare registers) Timer mode (output compare function, input capture function), PWM mode (3 outputs), PWM2 mode (1 PWM output)
Serial interface	UART0	Clock synchronous serial I/O. Also used for asynchronous serial I/O.
A/D converter		<ul style="list-style-type: none"> <li>• Resolution: 10 bits <math>\times</math> 6 channels</li> <li>• Sample and hold function, sweep mode</li> </ul>
Comparator B		2 circuits

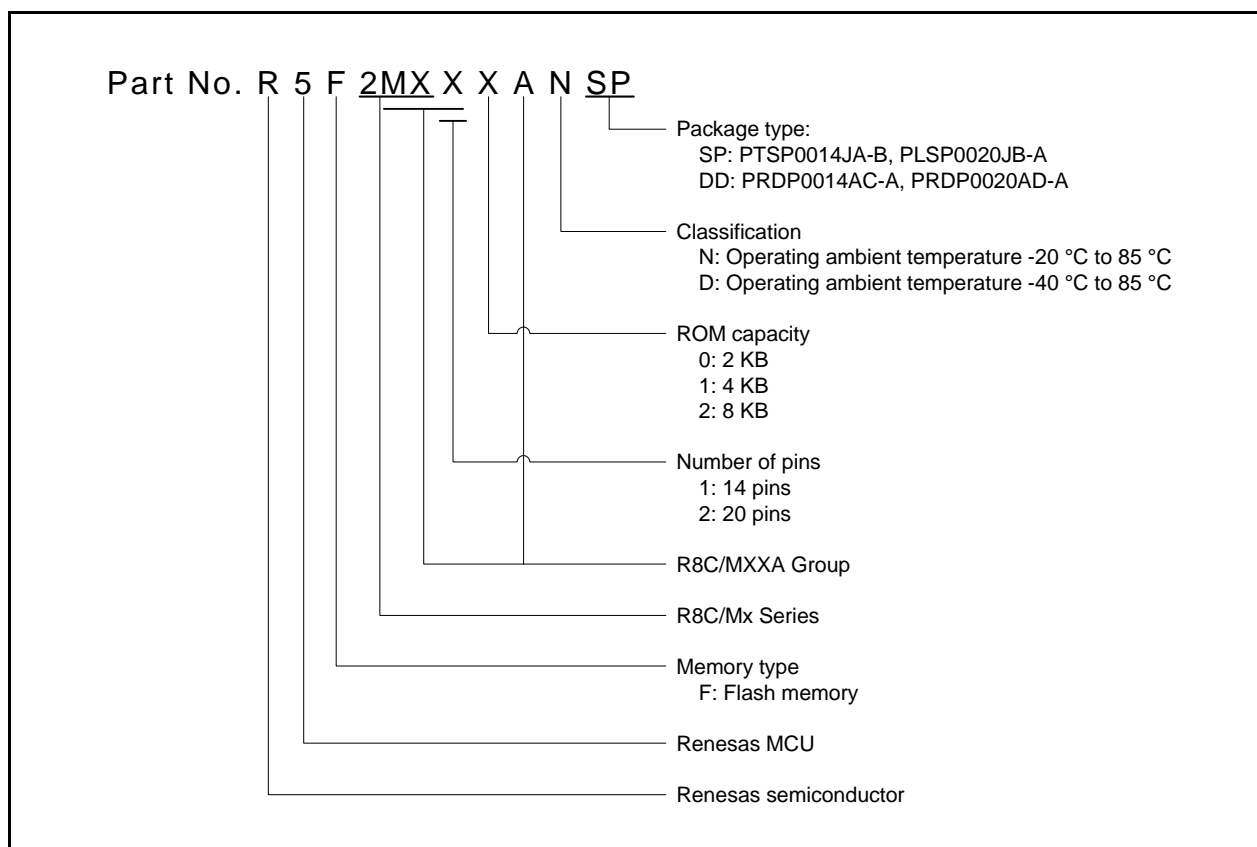
## 1.2 Product List

Table 1.5 lists the Product List. Figure 1.1 shows the Product Part Number Structure.

**Table 1.5 Product List**

**Current of May 2012**

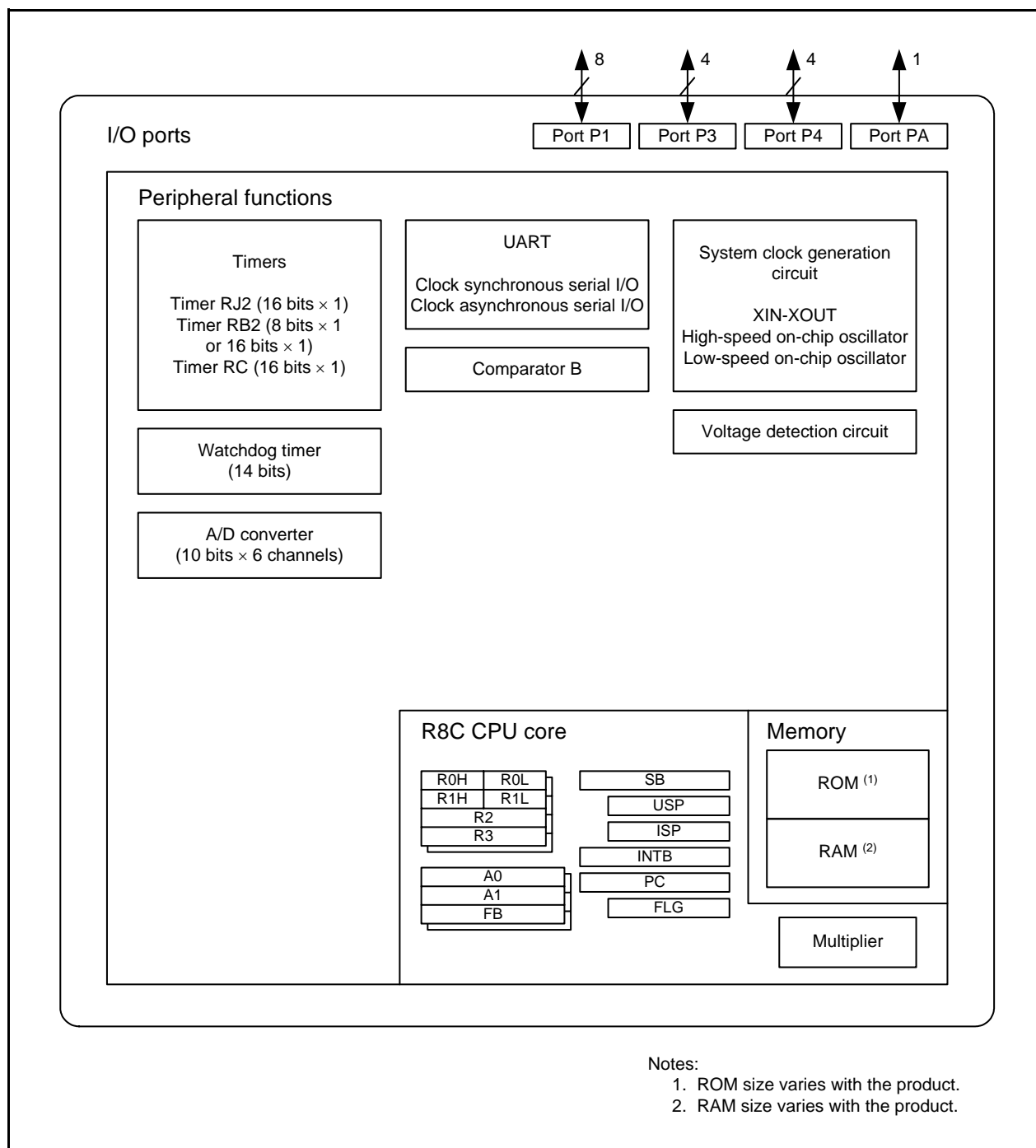
Group Name	Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
		Program ROM	Data Flash			
R8C/M11A Group	R5F2M110ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	N version
	R5F2M111ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0014AC-A	
	R5F2M111ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	D version
	R5F2M111ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		
R8C/M12A Group	R5F2M120ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	N version
	R5F2M121ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0020AD-A	
	R5F2M121ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	D version
	R5F2M121ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		



**Figure 1.1 Product Part Number Structure**

### 1.3 Block Diagram

Figure 1.2 shows the Block Diagram.



**Figure 1.2 Block Diagram**

## 1.5 Pin Functions

Table 1.7 lists the Pin Functions.

**Table 1.7 Pin Functions**

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	RESET	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit.
XIN clock output	XOUT	O	Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. <sup>(1)</sup> To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
INT interrupt input	INT0 to INT3	I	INT interrupt input.
Key input interrupt	KI0 to KI3	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	ADTRG	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

### 3. Address Space

#### 3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh. The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.

The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

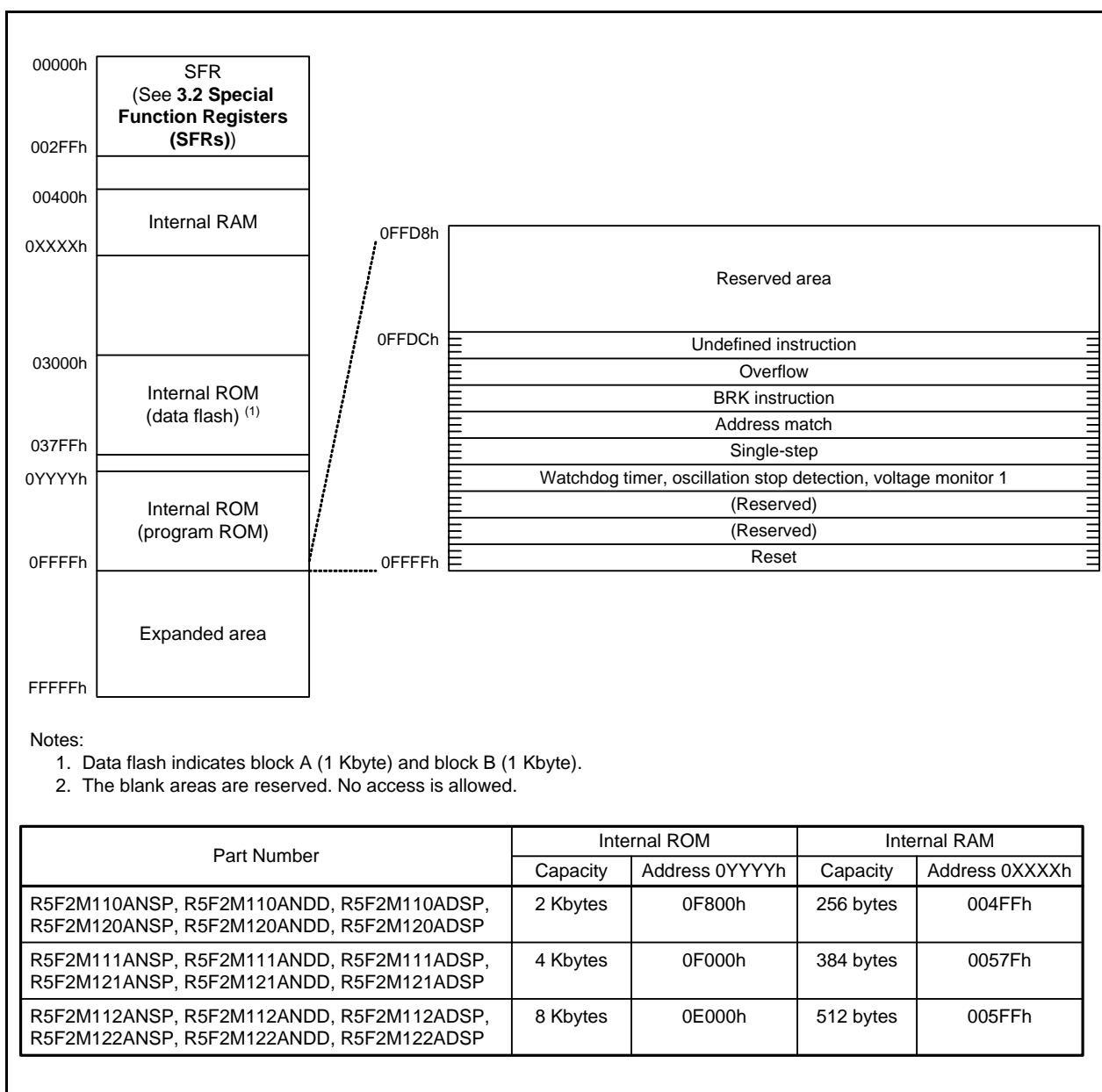


Figure 3.1 Memory Map

**Table 3.2 SFR Information (2) (1)**

Address	Register Name	Symbol	After Reset
0003Ah	INT Input Filter Select Register 0	INTF0	00h
0003Bh			
0003Ch	INT Input Edge Select Register 0	ISCR0	00h
0003Dh			
0003Eh	Key Input Enable Register	KIEN	00h
0003Fh			
00040h	Interrupt Priority Level Register 0	ILVL0	00h
00041h			
00042h	Interrupt Priority Level Register 2	ILVL2	00h
00043h	Interrupt Priority Level Register 3	ILVL3	00h
00044h	Interrupt Priority Level Register 4	ILVL4	00h
00045h	Interrupt Priority Level Register 5	ILVL5	00h
00046h	Interrupt Priority Level Register 6	ILVL6	00h
00047h	Interrupt Priority Level Register 7	ILVL7	00h
00048h	Interrupt Priority Level Register 8	ILVL8	00h
00049h	Interrupt Priority Level Register 9	ILVL9	00h
0004Ah	Interrupt Priority Level Register A	ILVLA	00h
0004Bh	Interrupt Priority Level Register B	ILVLB	00h
0004Ch	Interrupt Priority Level Register C	ILVLC	00h
0004Dh	Interrupt Priority Level Register D	ILVLD	00h
0004Eh	Interrupt Priority Level Register E	ILVLE	00h
0004Fh			
00050h	Interrupt Monitor Flag Register 0	IRR0	00h
00051h	Interrupt Monitor Flag Register 1	IRR1	00h
00052h	Interrupt Monitor Flag Register 2	IRR2	00h
00053h	External Interrupt Flag Register	IRR3	00h
00054h			
00055h			
00056h			
00057h			
00058h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
00059h			
0005Ah	Voltage Detect Register 2	VCA2	00100100b (2) 00000100b (3)
0005Bh	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0005Ch	Voltage Monitor 0 Circuit Control Register	VW0C	1100X011b (2) 1100X010b (3)
0005Dh	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
0005Eh			
0005Fh	Reset Source Determination Register	RSTFR	0000XXXXb (4)
00060h			
00061h			
00062h			
00063h			
00064h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped
00065h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped
00066h			
00067h	High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped
00068h	High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped
00069h			
0006Ah			
0006Bh			
0006Ch			
0006Dh			
0006Eh			
0006Fh			
00070h			
00071h			
00072h			
00073h			
00074h			
00075h			
00076h			
00077h			
00078h			
00079h			

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. The LVDAS bit in the OFS register is 0.
3. The LVDAS bit in the OFS register is 1.
4. The value after a reset differs depending on the reset source.



**Table 3.3 SFR Information (3) (1)**

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DDR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DDR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.6 SFR Information (6) (1)**

Address	Register Name	Symbol	After Reset
00140h			
00141h			
00142h			
00143h			
00144h			
00145h			
00146h			
00147h			
00148h			
00149h			
0014Ah			
0014Bh			
0014Ch			
0014Dh			
0014Eh			
0014Fh			
00150h			
00151h			
00152h			
00153h			
00154h			
00155h			
00156h			
00157h			
00158h			
00159h			
0015Ah			
0015Bh			
0015Ch			
0015Dh			
0015Eh			
0015Fh			
00160h			
00161h			
00162h			
00163h			
00164h			
00165h			
00166h			
00167h			
00168h			
00169h			
0016Ah			
0016Bh			
0016Ch			
0016Dh			
0016Eh			
0016Fh			
00170h			
00171h			
00172h			
00173h			
00174h			
00175h			
00176h			
00177h			
00178h			
00179h			
0017Ah			
0017Bh			
0017Ch			
0017Dh			
0017Eh			
0017Fh			

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.7 SFR Information (7) (1)**

Address	Register Name	Symbol	After Reset
00180h	Comparator B Control Register	WCMPR	00h
00181h	Comparator B1 Interrupt Control Register	WCB1INTR	00h
00182h	Comparator B3 Interrupt Control Register	WCB3INTR	00h
00183h			
00184h			
00185h			
00186h			
00187h			
00188h			
00189h			
0018Ah			
0018Bh			
0018Ch			
0018Dh			
0018Eh			
0018Fh			
00190h			
00191h			
00192h			
00193h			
00194h			
00195h			
00196h			
00197h			
00198h			
00199h			
0019Ah			
0019Bh			
0019Ch			
0019Dh			
0019Eh			
0019Fh			
001A0h			
001A1h			
001A2h			
001A3h			
001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	10000000b
001AAh	Flash Memory Control Register 0	FMR0	00h
001ABh	Flash Memory Control Register 1	FMR1	00h
001ACh	Flash Memory Control Register 2	FMR2	00h
001ADh	Flash Memory Refresh Control Register	FREFR	00h
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.8 SFR Information (8) (1)**

Address	Register Name	Symbol	After Reset
001C0h	Address Match Interrupt Register 0	AIADR0L	00h
001C1h		AIADR0M	00h
001C2h		AIADR0H	00h
001C3h	Address Match Interrupt Enable Register 0	AIEN0	00h
001C4h	Address Match Interrupt Register 1	AIADR1L	00h
001C5h		AIADR1M	00h
001C6h		AIADR1H	00h
001C7h	Address Match Interrupt Enable Register 1	AIEN1	00h
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			

Note:

1. The blank areas are reserved. No access is allowed.

## 4. Electrical Characteristics

**Table 4.1 Absolute Maximum Ratings**

Symbol	Parameter		Condition	Rated Value	Unit
V <sub>CC</sub> /AV <sub>CC</sub>	Power supply voltage			-0.3 to 6.5	V
V <sub>I</sub>	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) <sup>(1)</sup>	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) <sup>(1)</sup>	-0.3 to V <sub>CC</sub> + 0.3	V
		Other pins		-0.3 to V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) <sup>(1)</sup>	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) <sup>(1)</sup>	-0.3 to V <sub>CC</sub> + 0.3	V
		Other pins		-0.3 to V <sub>CC</sub> + 0.3	V
P <sub>d</sub>	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T <sub>opr</sub>	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature			-60 to 150	°C

Note:

1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b  
When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

**Table 4.3 A/D Converter Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	10	Bit
—	Absolute accuracy	AVcc = 5.0 V AN0 to AN4, AN7 input	—	—	±3	LSB
		AVcc = 3.0 V AN0 to AN4, AN7 input	—	—	±5	LSB
		AVcc = 1.8 V AN0 to AN4, AN7 input	—	—	±5	LSB
—	A/D conversion clock	4.0 V ≤ AVcc ≤ 5.5 V (2)	2	—	20	MHz
		3.2 V ≤ AVcc ≤ 5.5 V (2)	2	—	16	MHz
		2.7 V ≤ AVcc ≤ 5.5 V (2)	2	—	10	MHz
		1.8 V ≤ AVcc ≤ 5.5 V (2)	2	—	5	MHz
—	Permissible signal source impedance			3		kΩ
tCONV	Conversion time	AVcc = 5.0 V, A/D conversion clock = 20 MHz	2.20	—	—	μs
tSAMP	Sampling time	A/D conversion clock = 20 MHz	0.80	—	—	μs
VIA	Analog input voltage		0	—	AVcc	V

Notes:

1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

**Table 4.4 Comparator B Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	—	Vcc - 1.4	V
Vi	IVCMP1, IVCMP3 input voltage		-0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
td	Comparator output delay time (2)	Vi = Vref ± 100 mV	—	0.1	—	μs
IcMP	Comparator operating current	Vcc = 5.0 V	—	17.5	—	μA

Notes:

1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

**Table 4.7 Voltage Detection 0 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 <sup>(2)</sup>		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 <sup>(2)</sup>		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 <sup>(2)</sup>		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 <sup>(2)</sup>		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time <sup>(3)</sup>	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	μs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Wait time until voltage detection circuit operation starts <sup>(4)</sup>		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

**Table 4.8 Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_1 <sup>(2)</sup>	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 <sup>(2)</sup>	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 <sup>(2)</sup>	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 <sup>(2)</sup>	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 <sup>(2)</sup>	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B <sup>(2)</sup>	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D <sup>(2)</sup>	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F <sup>(2)</sup>	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time <sup>(3)</sup>	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	μs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Wait time until voltage detection circuit operation starts <sup>(4)</sup>		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

**Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Package	Condition	Standard			Unit
				Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	14-pin TSSOP 20-pin LSSOP	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ , $-20 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	19.2	20.0	20.8	MHz
		14-pin DIP 20-pin DIP		19.0	20.0	21.0	MHz
		14-pin TSSOP 20-pin LSSOP	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ , $-40 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register <sup>(2)</sup>	14-pin TSSOP 20-pin LSSOP	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ , $-20 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	17.694	18.432	19.169	MHz
		14-pin DIP 20-pin DIP		17.510	18.432	19.353	MHz
		14-pin TSSOP 20-pin LSSOP	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ , $-40 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	17.510	18.432	19.353	MHz
—	Oscillation stabilization time	—	—	—	—	30	$\mu\text{s}$
—	Self power consumption at oscillation	—	$V_{CC} = 5.0 \text{ V}$ , $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	530	—	$\mu\text{A}$

Notes:

1.  $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $T_{opr} = -20 \text{ }^{\circ}\text{C to } 85 \text{ }^{\circ}\text{C}$  (N version)/ $-40 \text{ }^{\circ}\text{C to } 85 \text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

**Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f <sub>LOCO</sub>	Low-speed on-chip oscillator frequency	—	60	125	250	kHz
—	Oscillation stabilization time	—	—	—	35	$\mu\text{s}$
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$ , $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	2	—	$\mu\text{A}$

Note:

1.  $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $T_{opr} = -20 \text{ }^{\circ}\text{C to } 85 \text{ }^{\circ}\text{C}$  (N version)/ $-40 \text{ }^{\circ}\text{C to } 85 \text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.

**Table 4.12 Power Supply Circuit Timing Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t <sub>d(P-R)</sub>	Time for internal power supply stabilization during power-on <sup>(2)</sup>	—	—	—	2,000	$\mu\text{s}$

Notes:

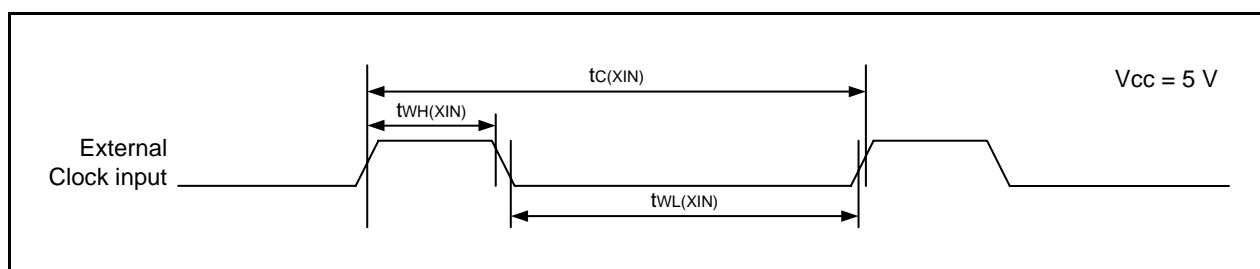
1. The measurement condition is  $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$  and  $T_{opr} = 25 \text{ }^{\circ}\text{C}$ .
2. Wait time until the internal power supply generation circuit stabilizes during power-on.



Timing Requirements ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{op} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

**Table 4.15 External Clock Input (XIN)**

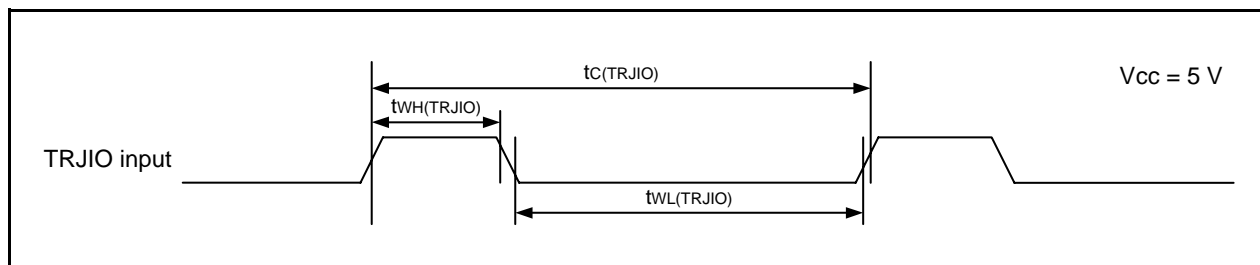
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns



**Figure 4.4 External Clock Input Timing When  $V_{CC} = 5\text{ V}$**

**Table 4.16 TRJIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns



**Figure 4.5 TRJIO Input Timing When  $V_{CC} = 5\text{ V}$**

**Table 4.20 DC Characteristics (4) [2.7 V ≤ V<sub>CC</sub> < 4.0 V]**  
**(Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)**

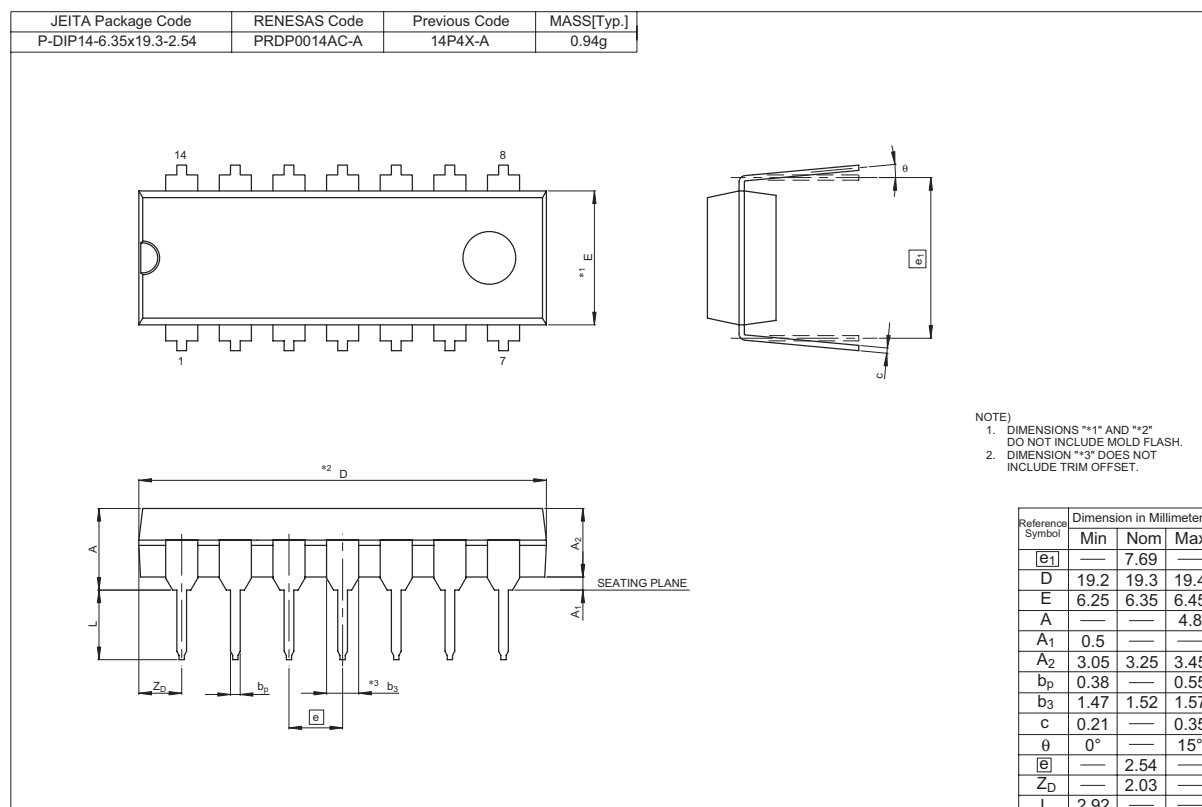
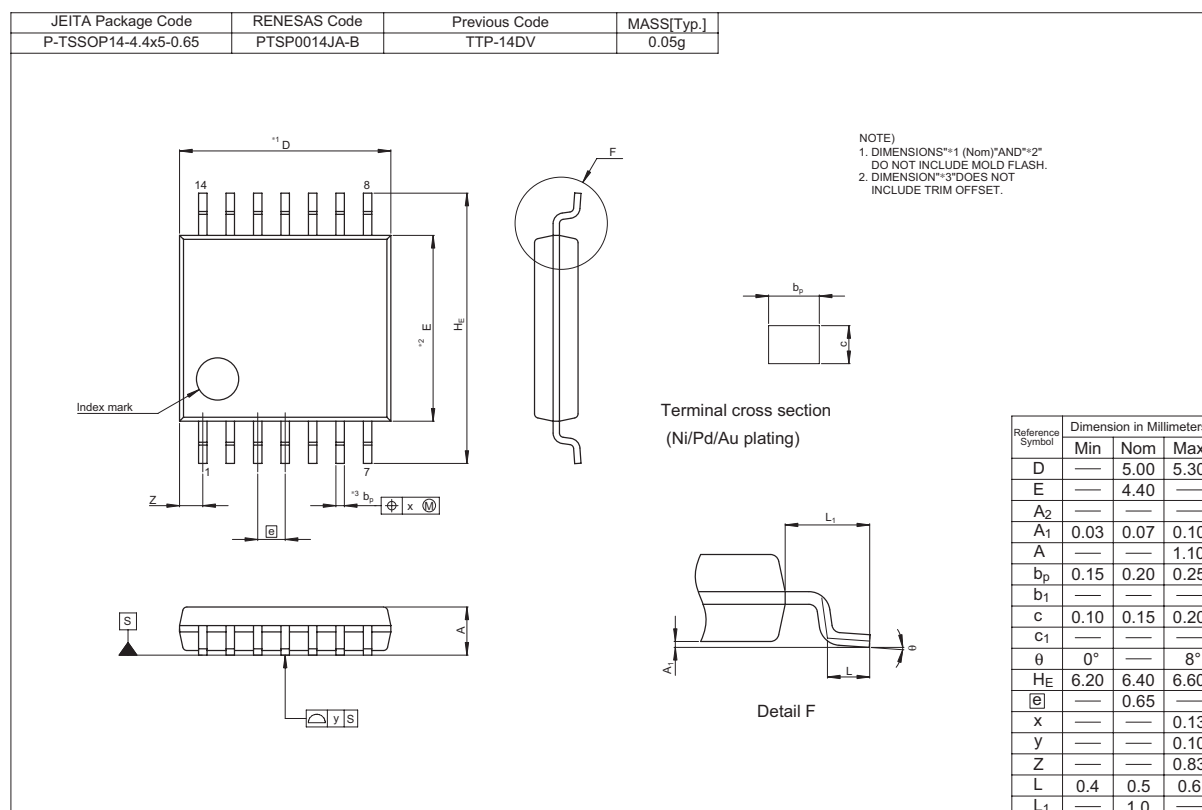
Symbol	Parameter		Condition									Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Standard			
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3.0	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.6	5.0	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	0.9	4.5	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	10 MHz (4)	125 kHz	No division			—	2.2	—	mA
			Off	10 MHz (4)	125 kHz	Division by 8			—	1.4	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	260	μA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	μA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	μA
			Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0
		Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	μA	

Notes:

1. V<sub>CC</sub> = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to V<sub>SS</sub>.
2. When the XIN input is a square wave.
3. V<sub>CC</sub> = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

## Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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