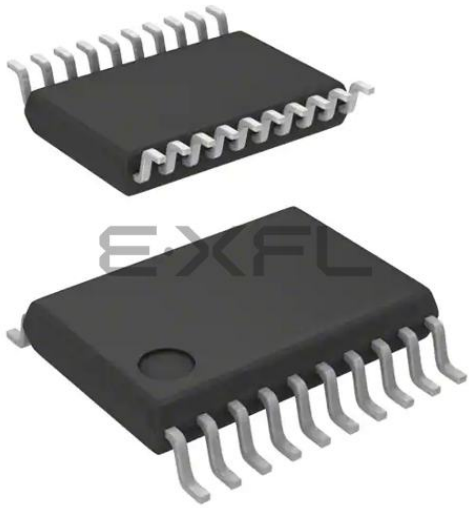

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m120ansp-w4

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

Related Function	Register Name	Address	Bit	Setting Method for Access
$\overline{\text{INT3}}$	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
$\overline{\text{KI0}}$	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

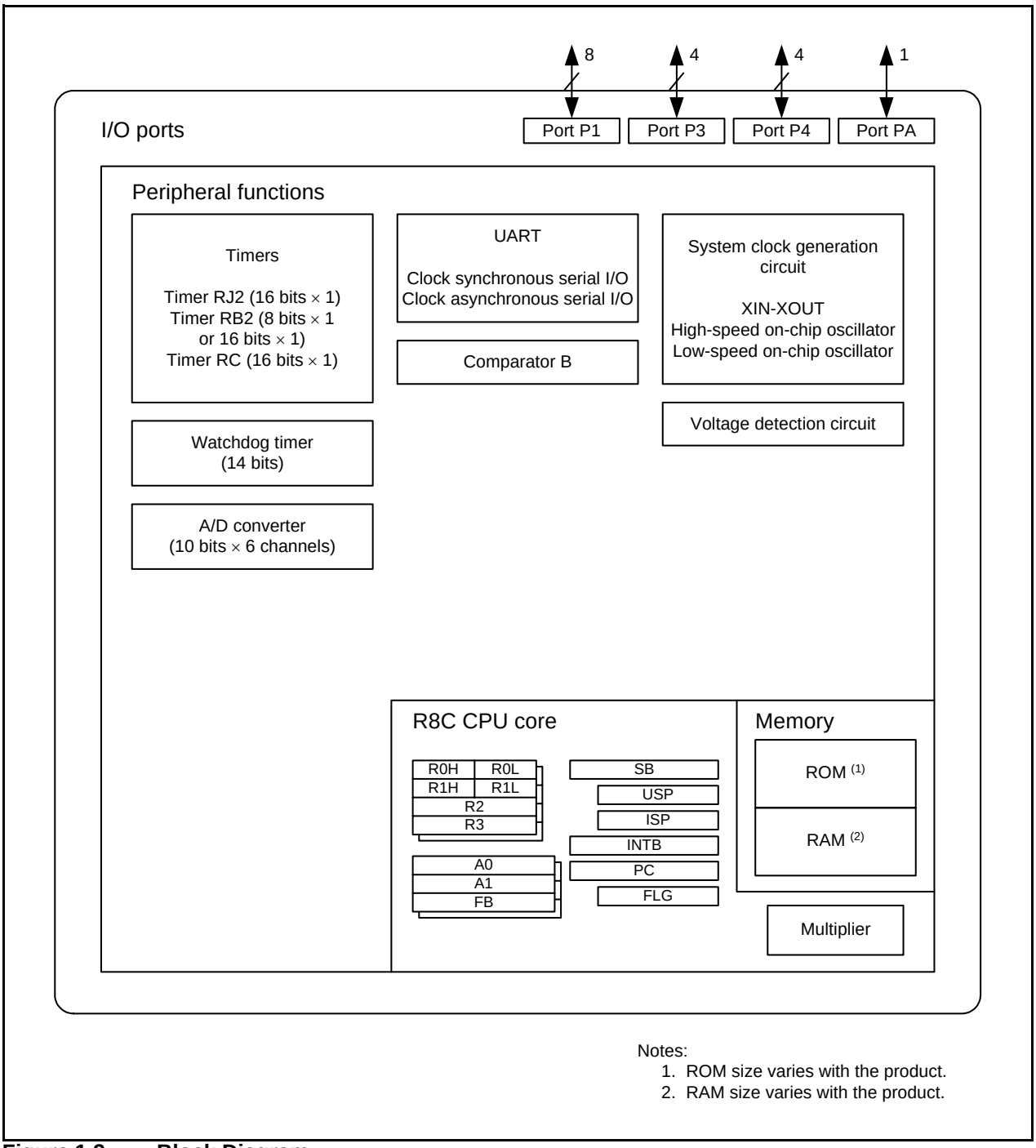


Figure 1.2 Block Diagram

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

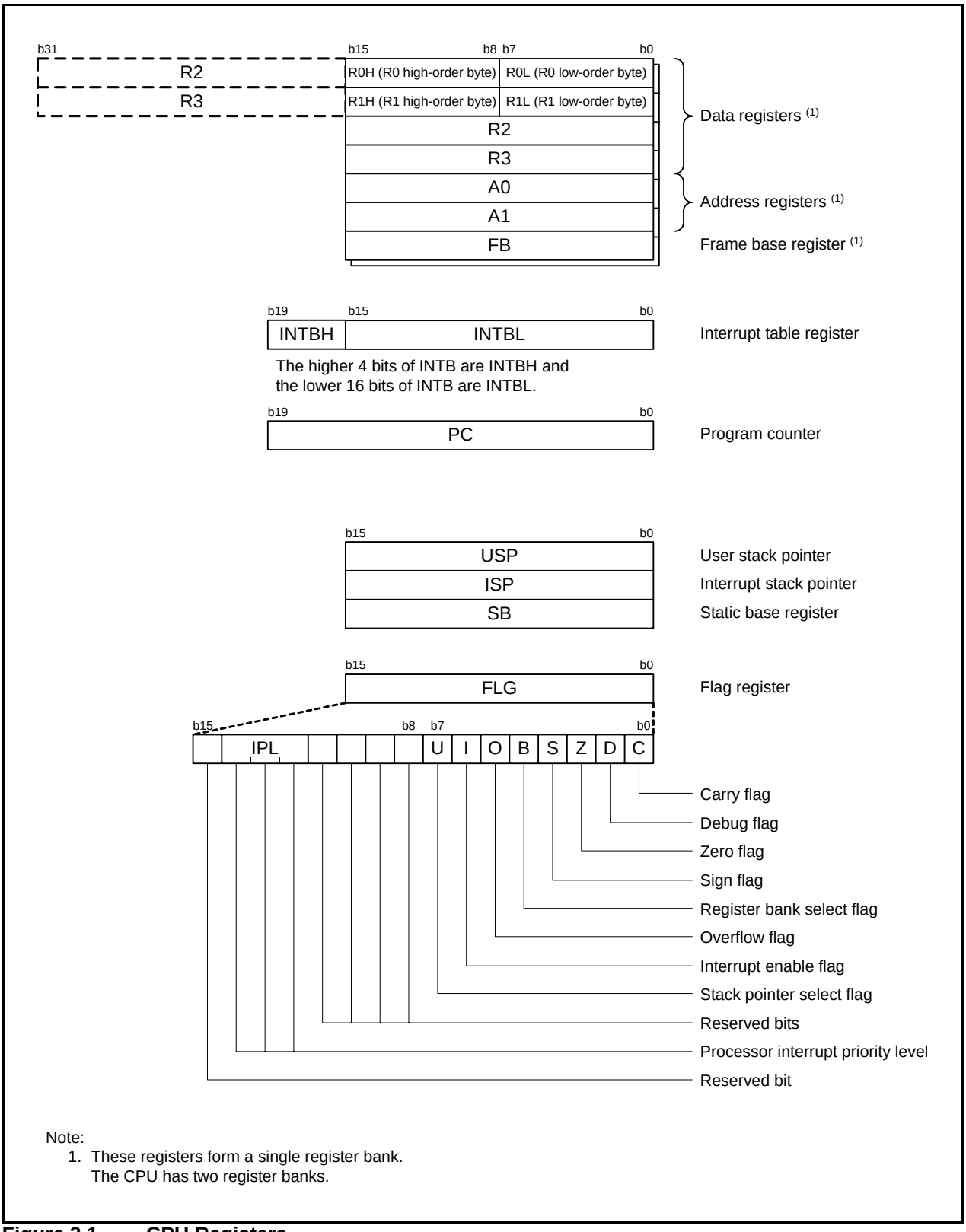
Table 1.7 Pin Functions

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

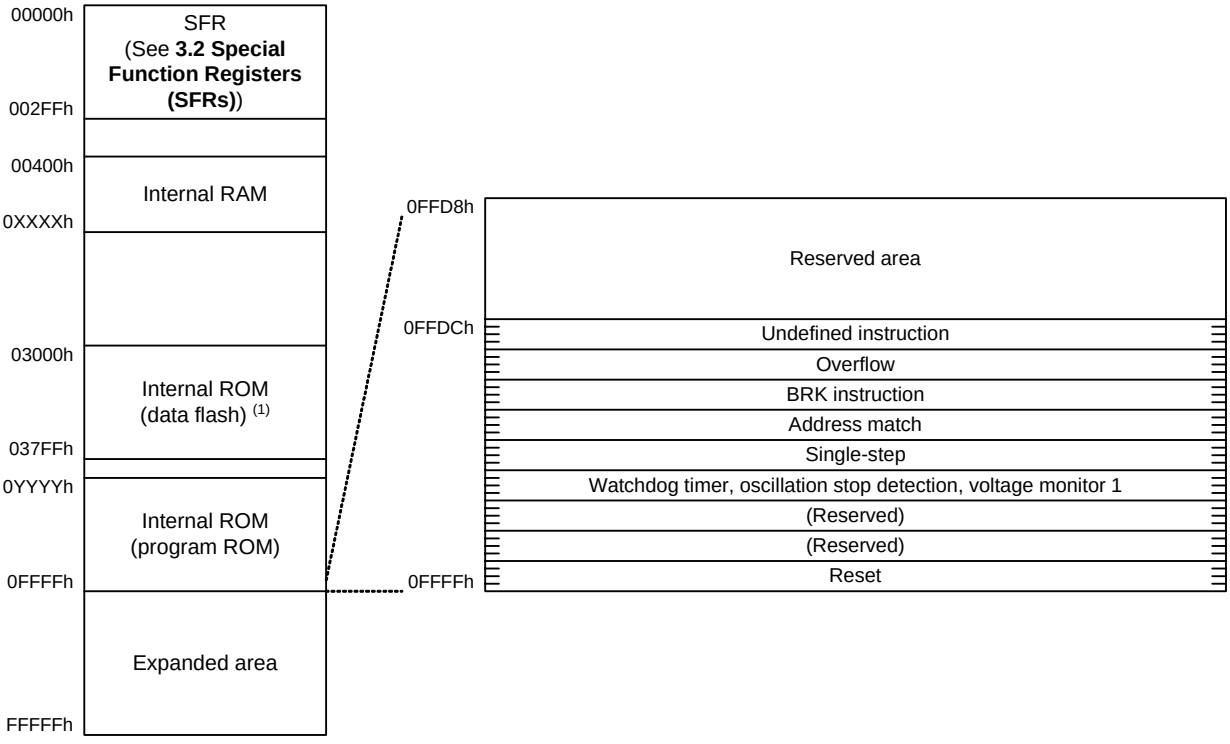
2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte) and block B (1 Kbyte).
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Capacity	Address 0YYYYh	Capacity	Address 0XXXXh
R5F2M110ANSP, R5F2M110ANDD, R5F2M110ADSP, R5F2M120ANSP, R5F2M120ANDD, R5F2M120ADSP	2 Kbytes	0F800h	256 bytes	004FFh
R5F2M111ANSP, R5F2M111ANDD, R5F2M111ADSP, R5F2M121ANSP, R5F2M121ANDD, R5F2M121ADSP	4 Kbytes	0F000h	384 bytes	0057Fh
R5F2M112ANSP, R5F2M112ANDD, R5F2M112ADSP, R5F2M122ANSP, R5F2M122ANDD, R5F2M122ADSP	8 Kbytes	0E000h	512 bytes	005FFh

Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.8 SFR Information (8) (1)

Address	Register Name	Symbol	After Reset
001C0h	Address Match Interrupt Register 0	AIADR0L	00h
001C1h		AIADR0M	00h
001C2h		AIADR0H	00h
001C3h	Address Match Interrupt Enable Register 0	AIEN0	00h
001C4h	Address Match Interrupt Register 1	AIADR1L	00h
001C5h		AIADR1M	00h
001C6h		AIADR1H	00h
001C7h	Address Match Interrupt Enable Register 1	AIEN1	00h
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Power supply voltage			1.8	—	5.5	V
V_{SS}/AV_{SS}	Power supply voltage			—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input		0.8 Vcc	—	Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
V_{IL}	Input low voltage	Other than CMOS input		0	—	0.2 Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
$I_{OH(sum)}$	Peak sum output high current	Sum of all pins $I_{OH(peak)}$		—	—	-160	mA
$I_{OH(sum)}$	Average sum output high current	Sum of all pins $I_{OH(avg)}$		—	—	-80	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high (5)	—	—	-40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high (5)	—	—	-20	mA
$I_{OL(sum)}$	Peak sum output low current	Sum of all pins $I_{OL(peak)}$		—	—	160	mA
$I_{OL(sum)}$	Average sum output low current	Sum of all pins $I_{OL(avg)}$		—	—	80	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high (5)	—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high (5)	—	—	20	mA
$f_{(XIN)}$	XIN oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz
fHOCO	High-speed on-chip oscillator oscillation frequency (3)		1.8 V ≤ Vcc ≤ 5.5 V	—	20	—	MHz
fLOCO	Low-speed on-chip oscillator oscillation frequency (4)		1.8 V ≤ Vcc ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f_S	CPU clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

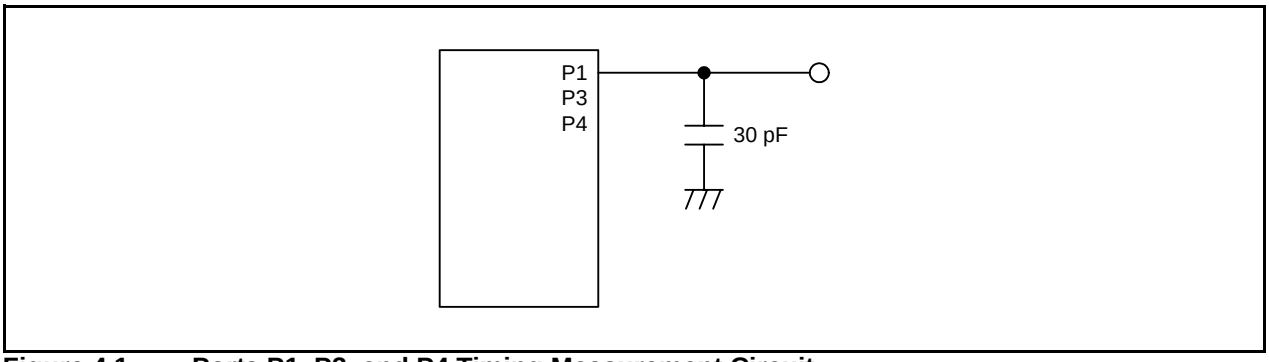


Figure 4.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 4.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

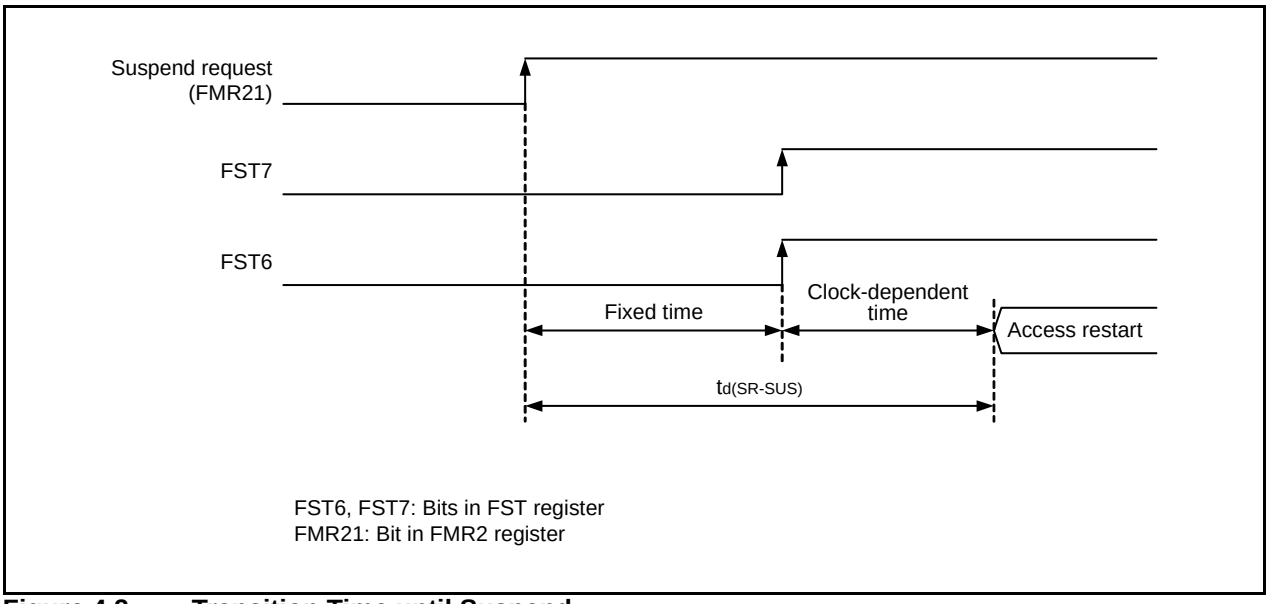
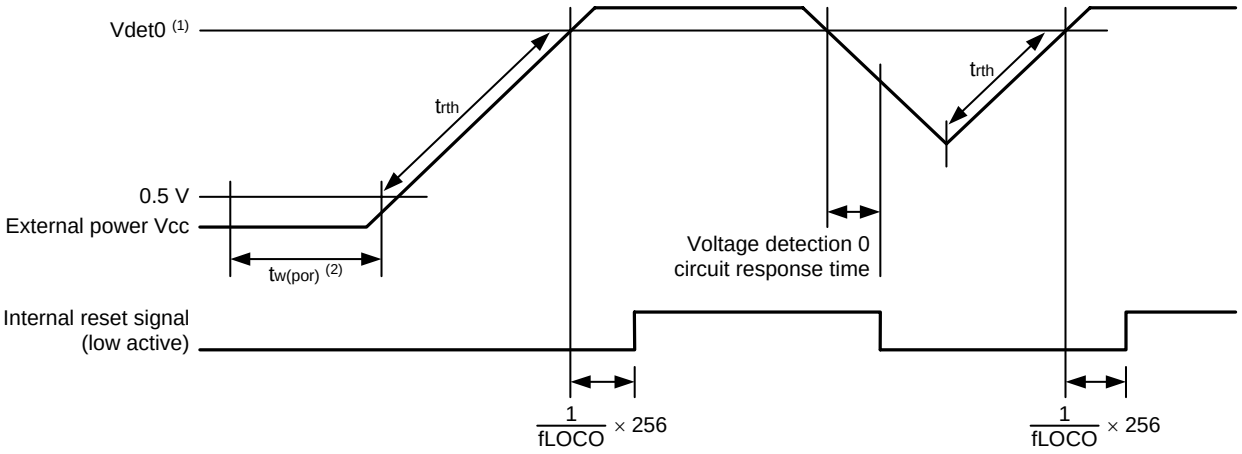


Figure 4.2 Transition Time until Suspend

Table 4.9 Power-On Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power Vcc rise gradient		0	—	50,000	mV/msec

Notes:
1. The measurement condition is Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, see **7. Voltage Detection Circuit** in the User's Manual: Hardware.
2. $t_{w(por)}$ is required for a power-on reset to be enabled with the external power Vcc held below the valid voltage (0.5 V) to enable a power-on reset. When Vcc decreases with voltage monitor 0 reset disabled and then turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 4.3 Power-On Reset Circuit Electrical Characteristics

Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Package	Condition	Standard			Unit
				Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	19.2	20.0	20.8	MHz
		14-pin DIP 20-pin DIP		19.0	20.0	21.0	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register (2)	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	17.694	18.432	19.169	MHz
		14-pin DIP 20-pin DIP		17.510	18.432	19.353	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	17.510	18.432	19.353	MHz
—	Oscillation stabilization time	—		—	—	30	µs
—	Self power consumption at oscillation	—	Vcc = 5.0 V, Topr = 25 °C	—	530	—	µA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stabilization time		—	—	35	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	2	—	µA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

Table 4.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 4.13 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -20 mA	Vcc - 2.0	—	Vcc	V
			When drive capacity is low	I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 5 mA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 5 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

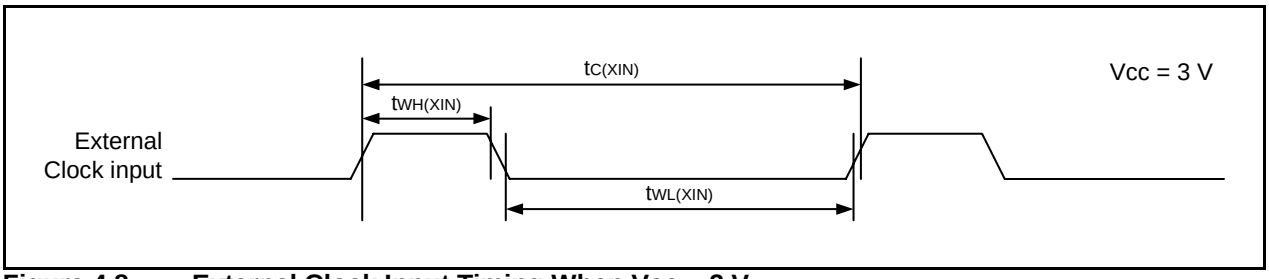


Figure 4.8 External Clock Input Timing When Vcc = 3 V

Table 4.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

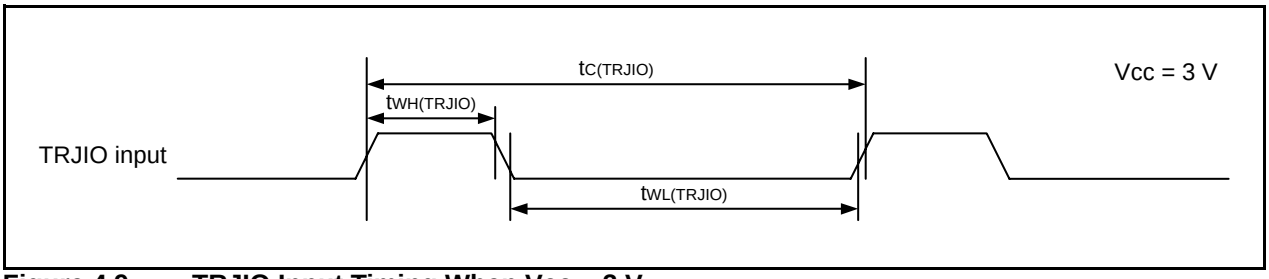


Figure 4.9 TRJIO Input Timing When Vcc = 3 V

Table 4.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{W(CKH)}$	CLK0 input high width	150	—	ns
$t_{W(CKL)}$	CLK0 input low width	150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	70	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

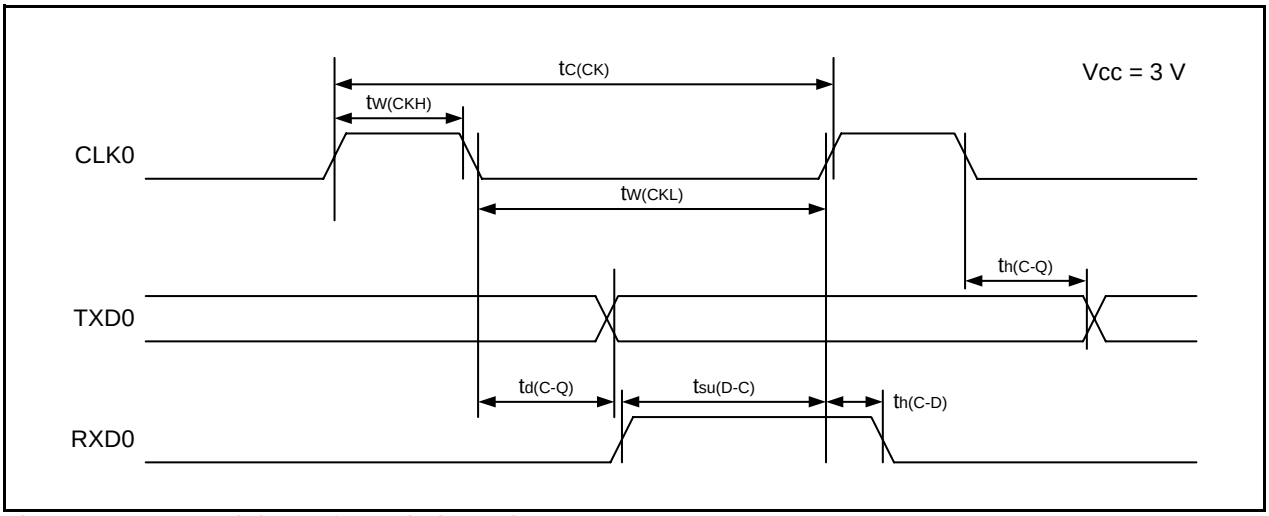


Figure 4.10 Serial Interface Timing When Vcc = 3 V

Table 4.24 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	380 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

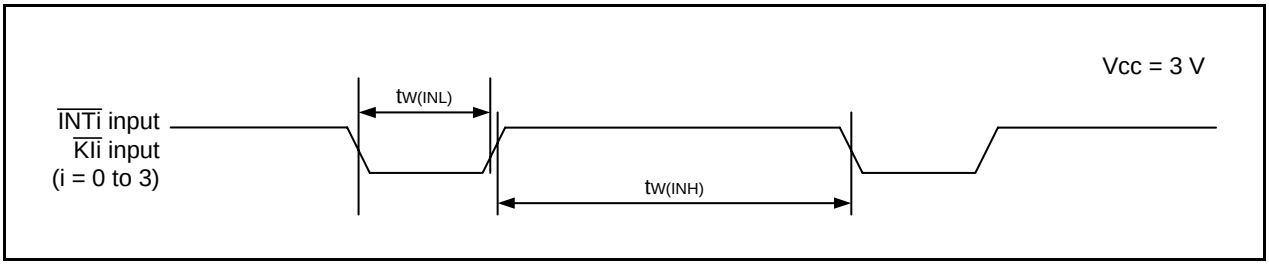
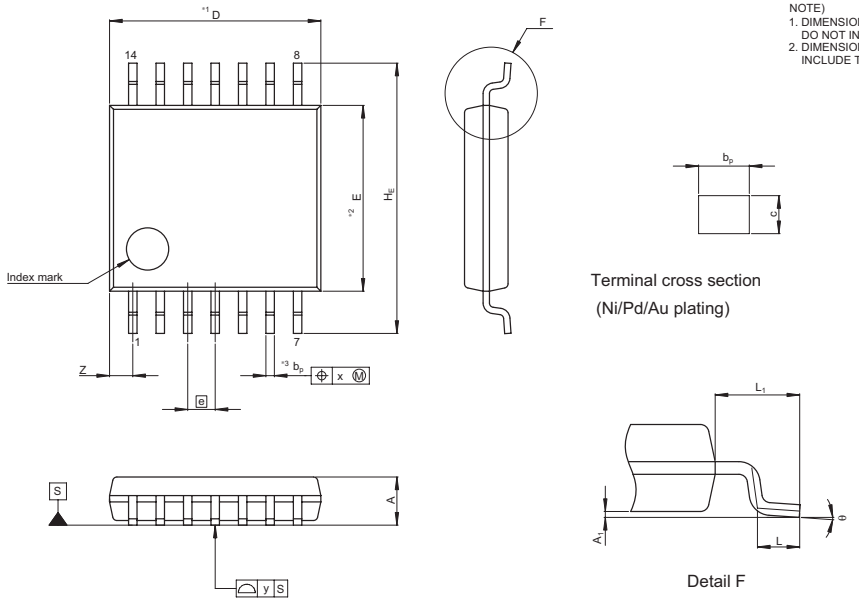


Figure 4.11 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 3 V

Package Dimensions

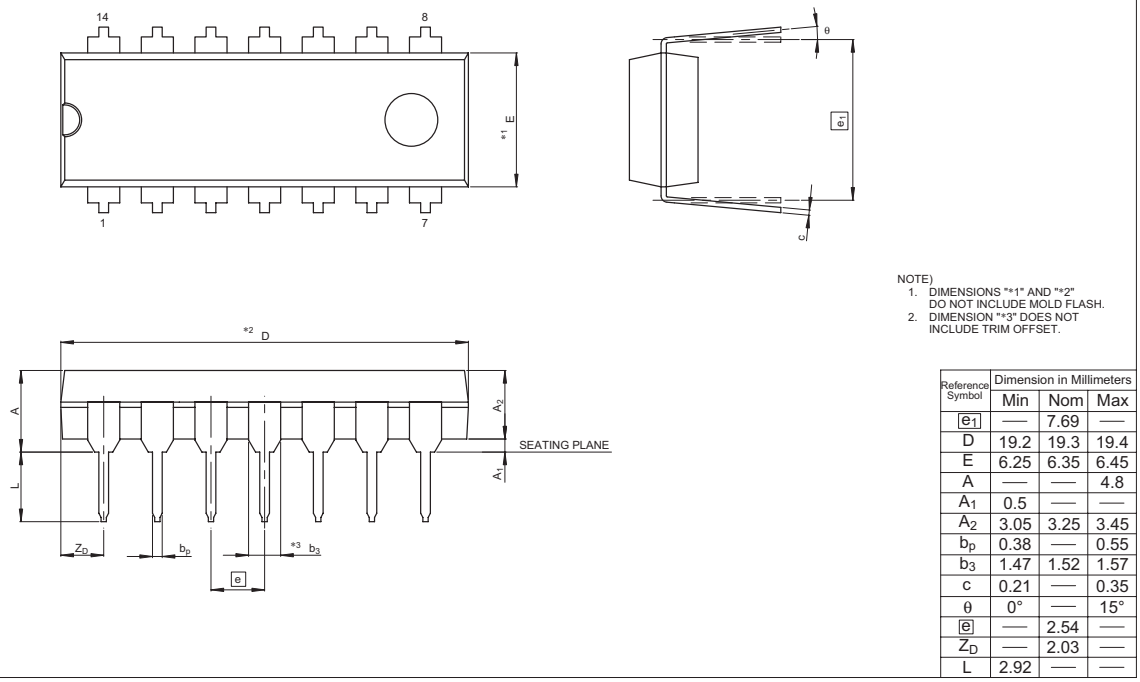
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



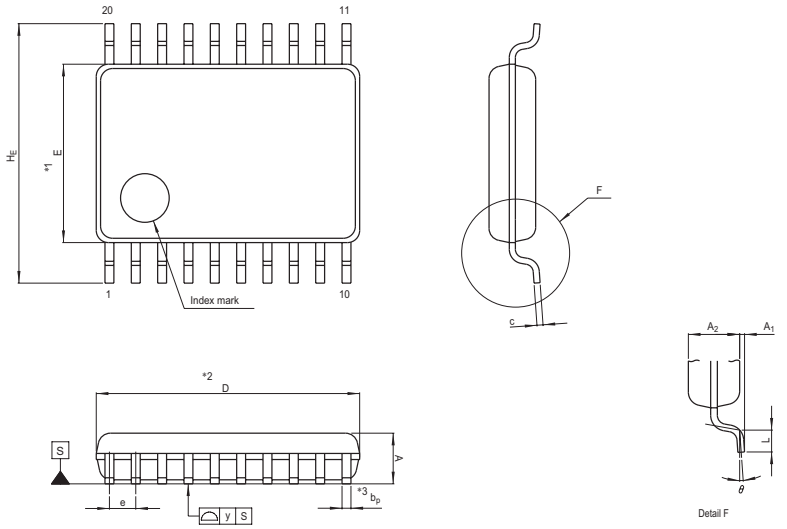
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.35x19.3-2.54	PRDP0014AC-A	14P4X-A	0.94g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.69	—
D	19.2	19.3	19.4
E	6.25	6.35	6.45
A	—	—	4.8
A_1	0.5	—	—
A_2	3.05	3.25	3.45
b_p	0.38	—	0.55
b_3	1.47	1.52	1.57
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	2.03	—
L	2.92	—	—

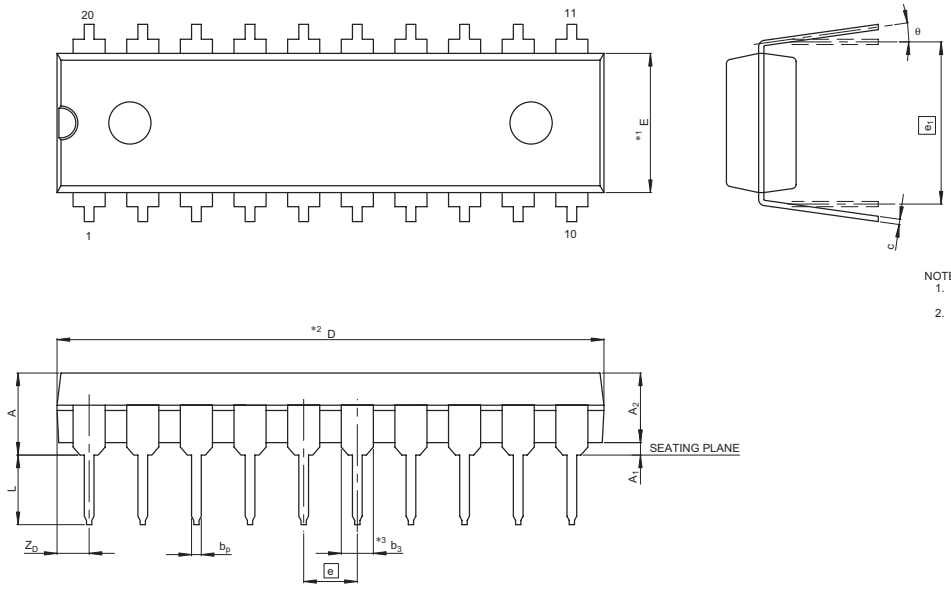
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.6x25.9-2.54	PRDP0020AD-A	20P4X-A	1.39g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.69	—
D	24.9	25.9	26.9
E	6.1	6.6	7.1
A	—	—	5.33
A_1	0.38	—	—
A_2	3.1	3.3	3.5
b_p	0.36	0.46	0.56
b_3	1.32	1.52	1.72
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	1.52	—
L	2.9	—	—

REVISION HISTORY	R8C/M11A Group, R8C/M12A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan 14, 2010	—	First Edition issued
0.10	Aug 25, 2010	—	Document No. “REJ03B0308” → “R01DS0010EJ”
		2, 3	1.1.2 Differences between Groups added
		4	Table 1.3 “Reset by voltage detection 0” deleted
		5	Table 1.4 “... ROM: VCC = 2.7 V to 5.5 V” → “... ROM: VCC = 1.8 V to 5.5 V”, “1,000 times (program ROM)” → “10,000 times (program ROM)”, Note 1 added
		6	Table 1.5 revised
		8	Figures 1.3 and 1.4 revised
		9	Table 1.6 revised
		11 to 43	2. Central Processing Unit (CPU), 3. Address Space, 4. Electrical Characteristics added
1.00	May 31, 2012	All pages	“Preliminary” and “Under development” deleted
		1	1.1 revised
		3	Table 1.2 revised
		4	Table 1.3 revised
		5	Table 1.4 Note 1 revised
		6	Table 1.5 revised
		10	Table 1.7 revised
		15	Table 3.1 revised
		18	Table 3.4 revised
		23	Table 3.9 Notes 1 and 2 revised
		26	Table 4.3 revised
		31	Table 4.10 and 4.11 revised, Note3 deleted
		45	Package added
2.00	May 31, 2012	4	“Under development” deleted
		9	Table 1.6 “Voltage detection circuit” deleted
		26	Table 4.3 revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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