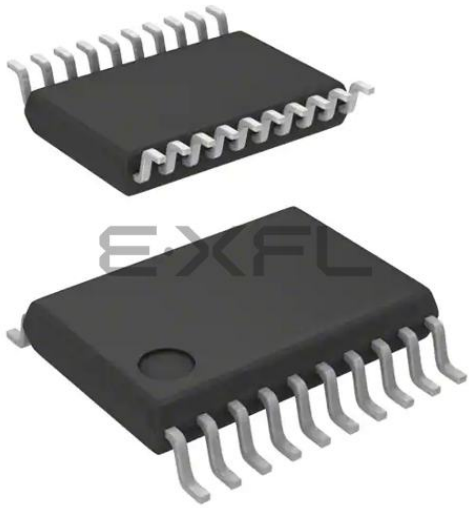

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m121ansp-w4

1.1.2 Differences between Groups

Table 1.1 lists the Specification Comparison between R8C/M11A Group and R8C/M12A Group. The explanations in 1.1.3 and subsequent sections apply to the R8C/M12A Group specifications only, unless otherwise specified.

Table 1.1 Specification Comparison between R8C/M11A Group and R8C/M12A Group

Item	Function	R8C/M11A Group	R8C/M12A Group
Interrupts	External interrupt inputs	6 ($\overline{\text{INT}}$ × 3, key input × 3)	8 ($\overline{\text{INT}}$ × 4, key input × 4)
I/O ports	Number of pins	14 Non-provided pins: P1_0/AN0/TRCIOD/$\overline{\text{KI0}}$ P3_3/IVCMP3/TRCCLK/$\overline{\text{INT3}}$ P3_4/IVREF3/TRCIOC/$\overline{\text{INT2}}$ P3_5/TRCIOD/$\overline{\text{KI2}}$/$\overline{\text{VCOUT}}$3 P4_2/$\overline{\text{TRBO}}$/$\overline{\text{TXD0}}$/$\overline{\text{KI3}}$ P4_5/$\overline{\text{INT0}}$/$\overline{\text{ADTRG}}$	20
	Number of CMOS I/O ports	11 Non-provided ports: P1_0, P3_3, P3_4, P3_5, P4_2, P4_5	17
	Number of high-current drive ports	5 Non-provided ports: P3_3, P3_4, P3_5	8
A/D converter	Number of A/D channels	5 channels Non-provided port: AN0	6 channels
Comparator B	Number of channels	Comparator B1	Comparator B1, comparator B3

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

Related Function	Register Name	Address	Bit	Setting Method for Access
$\overline{\text{INT3}}$	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
$\overline{\text{KI0}}$	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:
1. Specify the D version if it is to be used.

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

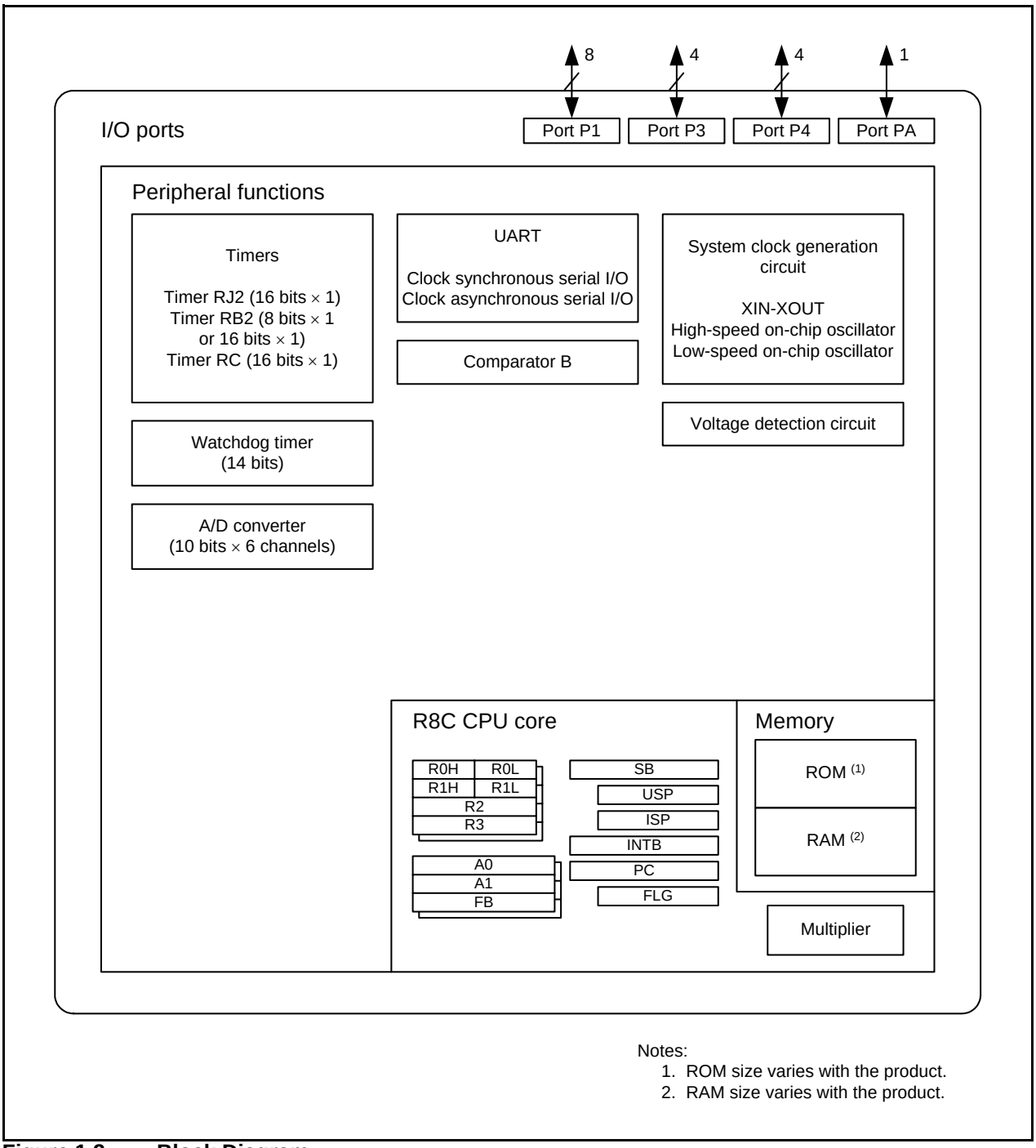


Figure 1.2 Block Diagram

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

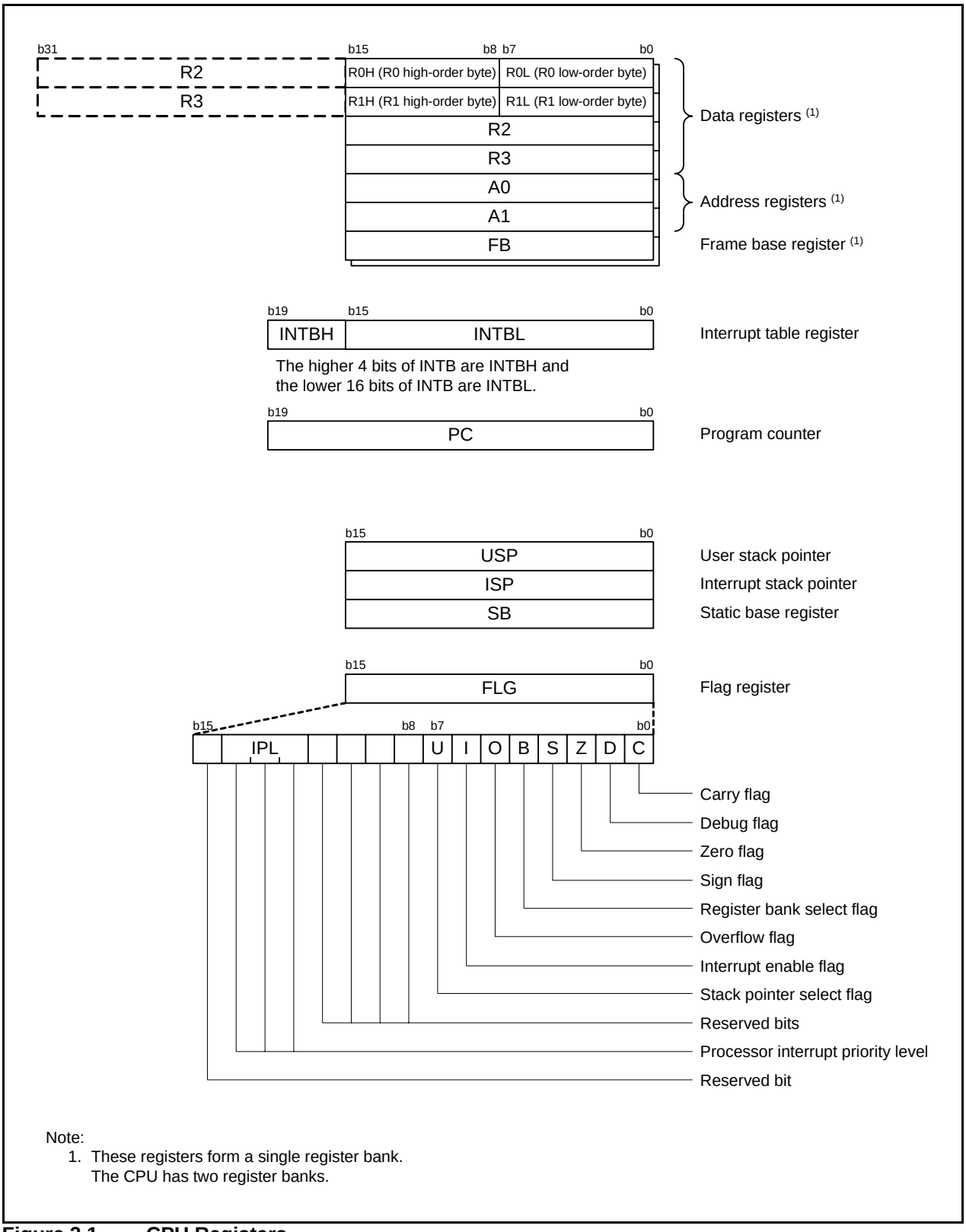
Table 1.7 Pin Functions

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

Table 3.2 SFR Information (2) (1)

Address	Register Name	Symbol	After Reset
0003Ah	INT Input Filter Select Register 0	INTF0	00h
0003Bh			
0003Ch	INT Input Edge Select Register 0	ISCR0	00h
0003Dh			
0003Eh	Key Input Enable Register	KIEN	00h
0003Fh			
00040h	Interrupt Priority Level Register 0	ILVL0	00h
00041h			
00042h	Interrupt Priority Level Register 2	ILVL2	00h
00043h	Interrupt Priority Level Register 3	ILVL3	00h
00044h	Interrupt Priority Level Register 4	ILVL4	00h
00045h	Interrupt Priority Level Register 5	ILVL5	00h
00046h	Interrupt Priority Level Register 6	ILVL6	00h
00047h	Interrupt Priority Level Register 7	ILVL7	00h
00048h	Interrupt Priority Level Register 8	ILVL8	00h
00049h	Interrupt Priority Level Register 9	ILVL9	00h
0004Ah	Interrupt Priority Level Register A	ILVLA	00h
0004Bh	Interrupt Priority Level Register B	ILVLB	00h
0004Ch	Interrupt Priority Level Register C	ILVLC	00h
0004Dh	Interrupt Priority Level Register D	ILVLD	00h
0004Eh	Interrupt Priority Level Register E	ILVLE	00h
0004Fh			
00050h	Interrupt Monitor Flag Register 0	IRR0	00h
00051h	Interrupt Monitor Flag Register 1	IRR1	00h
00052h	Interrupt Monitor Flag Register 2	IRR2	00h
00053h	External Interrupt Flag Register	IRR3	00h
00054h			
00055h			
00056h			
00057h			
00058h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
00059h			
0005Ah	Voltage Detect Register 2	VCA2	00100100b (2) 00000100b (3)
0005Bh	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0005Ch	Voltage Monitor 0 Circuit Control Register	VW0C	1100X011b (2) 1100X010b (3)
0005Dh	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
0005Eh			
0005Fh	Reset Source Determination Register	RSTFR	0000XXXXb (4)
00060h			
00061h			
00062h			
00063h			
00064h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped
00065h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped
00066h			
00067h	High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped
00068h	High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped
00069h			
0006Ah			
0006Bh			
0006Ch			
0006Dh			
0006Eh			
0006Fh			
00070h			
00071h			
00072h			
00073h			
00074h			
00075h			
00076h			
00077h			
00078h			
00079h			

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. The LVDAS bit in the OFS register is 0.
3. The LVDAS bit in the OFS register is 1.
4. The value after a reset differs depending on the reset source.

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Register Name	Symbol	After Reset
000C0h			
000C1h	Open-Drain Control Register 1	POD1	00h
000C2h			
000C3h	Open-Drain Control Register 3	POD3	00h
000C4h	Open-Drain Control Register 4	POD4	00h
000C5h	Port PA Mode Control Register	PAMCR	00010001b
000C6h			
000C7h			
000C8h	Port 1 Function Mapping Register 0	PML1	00h
000C9h	Port 1 Function Mapping Register 1	PMH1	00h
000CAh			
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	00h
000CDh	Port 3 Function Mapping Register 1	PMH3	00h
000CEh	Port 4 Function Mapping Register 0	PML4	00h
000CFh	Port 4 Function Mapping Register 1	PMH4	00h
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	00h
000D2h			
000D3h			
000D4h			
000D5h	Port 4 Function Mapping Expansion Register	PMH4E	00h
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	FFh
000D9h			FFh
000DAh	Timer RJ Control Register	TRJCR	00h
000DBh	Timer RJ I/O Control Register	TRJIOC	00h
000DCh	Timer RJ Mode Register	TRJMR	00h
000DDh	Timer RJ Event Select Register	TRJISR	00h
000DEh	Timer RJ Interrupt Control Register	TRJIR	00h
000DFh			
000E0h	Timer RB Control Register	TRBCR	00h
000E1h	Timer RB One-Shot Control Register	TRBOCR	00h
000E2h	Timer RB I/O Control Register	TRBIOC	00h
000E3h	Timer RB Mode Register	TRBMR	00h
000E4h	Timer RB Prescaler Register (2) Timer RB Primary/Secondary Register (Lower 8 Bits) (3)	TRBPRE	FFh
000E5h	Timer RB Primary Register (2) Timer RB Primary Register (Higher 8 Bits) (3)	TRBPR	FFh
000E6h	Timer RB Secondary Register (2) Timer RB Secondary Register (Higher 8 Bits) (3)	TRBSC	FFh
000E7h	Timer RB Interrupt Control Register	TRBIR	00h
000E8h	Timer RC Counter	TRCCNT	00h
000E9h			00h
000EAh	Timer RC General Register A	TRCGRA	FFh
000EBh			FFh
000ECh	Timer RC General Register B	TRCGRB	FFh
000EDh			FFh
000EEh	Timer RC General Register C	TRCGRC	FFh
000EFh			FFh
000F0h	Timer RC General Register D	TRCGRD	FFh
000F1h			FFh
000F2h	Timer RC Mode Register	TRCMR	01001000b
000F3h	Timer RC Control Register 1	TRCCR1	00h
000F4h	Timer RC Interrupt Enable Register	TRCIER	01110000b
000F5h	Timer RC Status Register	TRCSR	01110000b
000F6h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
000F7h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
000F8h	Timer RC Control Register 2	TRCCR2	00011000b
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	00h
000FAh	Timer RC Output Enable Register	TRCOER	01111111b
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	00h
000FDh			
000FEh			
000FFh			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The TCNT16 bit in the TRBMR register is 0.
3. The TCNT16 bit in the TRBMR register is 1.

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h			
00131h			
00132h			
00133h			
00134h			
00135h			
00136h			
00137h			
00138h			
00139h			
0013Ah			
0013Bh			
0013Ch			
0013Dh			
0013Eh			
0013Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
0FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
0FFDFh	ID1		(Note 2)
:			
0FFE3h	ID2		(Note 2)
:			
0FFEBh	ID3		(Note 2)
:			
0FFEFh	ID4		(Note 2)
:			
0FFF3h	ID5		(Note 2)
:			
0FFF7h	ID6		(Note 2)
:			
0FFFBh	ID7		(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

4. Electrical Characteristics

Table 4.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Power supply voltage			-0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
P_d	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T_{stg}	Storage temperature			-60 to 150	°C

Note:
1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
   When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Table 4.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Power supply voltage			1.8	—	5.5	V
V_{SS}/AV_{SS}	Power supply voltage			—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input		0.8 Vcc	—	Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
V_{IL}	Input low voltage	Other than CMOS input		0	—	0.2 Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
$I_{OH(sum)}$	Peak sum output high current	Sum of all pins $I_{OH(peak)}$		—	—	-160	mA
$I_{OH(sum)}$	Average sum output high current	Sum of all pins $I_{OH(avg)}$		—	—	-80	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high (5)	—	—	-40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high (5)	—	—	-20	mA
$I_{OL(sum)}$	Peak sum output low current	Sum of all pins $I_{OL(peak)}$		—	—	160	mA
$I_{OL(sum)}$	Average sum output low current	Sum of all pins $I_{OL(avg)}$		—	—	80	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high (5)	—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high (5)	—	—	20	mA
$f_{(XIN)}$	XIN oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz
fHOCO	High-speed on-chip oscillator oscillation frequency (3)		1.8 V ≤ Vcc ≤ 5.5 V	—	20	—	MHz
fLOCO	Low-speed on-chip oscillator oscillation frequency (4)		1.8 V ≤ Vcc ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f_S	CPU clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

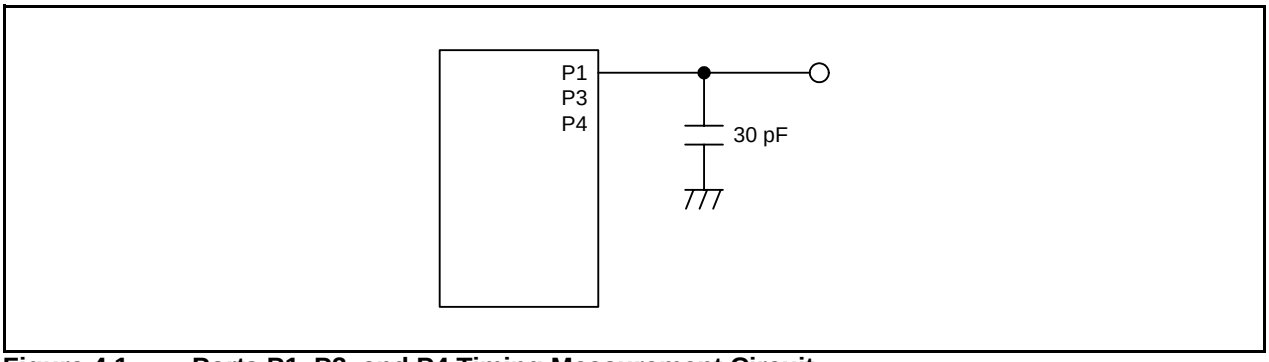


Figure 4.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 4.3 A/D Converter Characteristics

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	10	Bit
—	Absolute accuracy	AVcc = 5.0 V	AN0 to AN4, AN7 input	—	—	±3	LSB
		AVcc = 3.0 V	AN0 to AN4, AN7 input	—	—	±5	LSB
		AVcc = 1.8 V	AN0 to AN4, AN7 input	—	—	±5	LSB
—	A/D conversion clock	4.0 V ≤ AVcc ≤ 5.5 V (2)		2	—	20	MHz
		3.2 V ≤ AVcc ≤ 5.5 V (2)		2	—	16	MHz
		2.7 V ≤ AVcc ≤ 5.5 V (2)		2	—	10	MHz
		1.8 V ≤ AVcc ≤ 5.5 V (2)		2	—	5	MHz
—	Permissible signal source impedance				3		kΩ
t_{CONV}	Conversion time	AVcc = 5.0 V, A/D conversion clock = 20 MHz		2.20	—	—	µs
t_{SAMP}	Sampling time	A/D conversion clock = 20 MHz		0.80	—	—	µs
V_{IA}	Analog input voltage			0	—	AVcc	V

Notes:
1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

Table 4.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc - 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 4.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

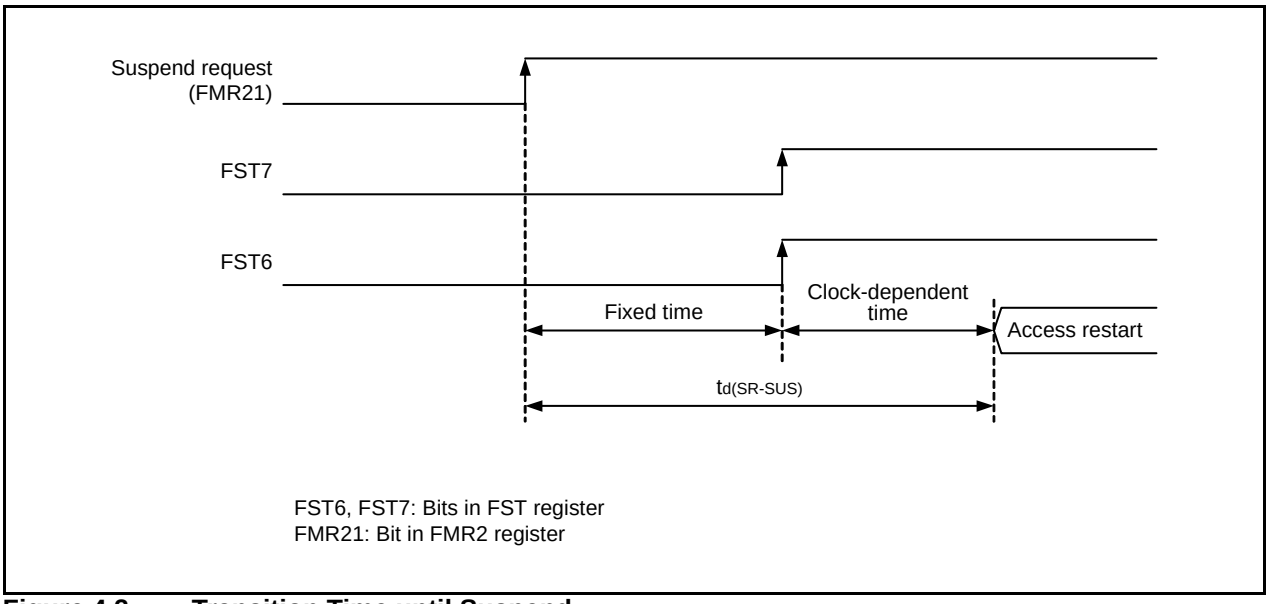


Figure 4.2 Transition Time until Suspend

Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.15 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

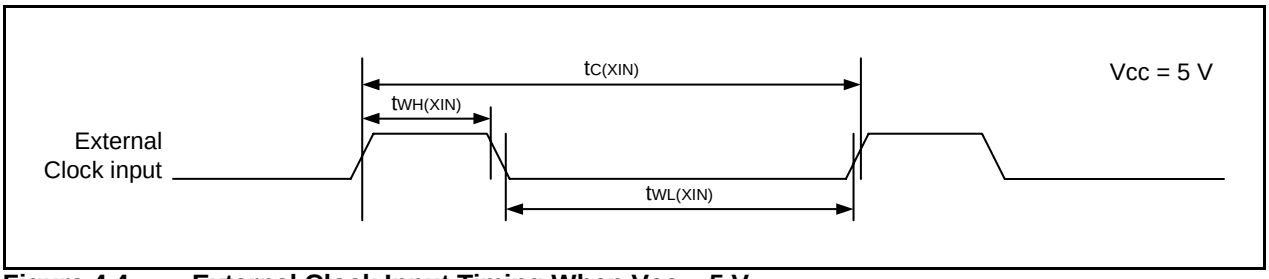


Figure 4.4 External Clock Input Timing When Vcc = 5 V

Table 4.16 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns

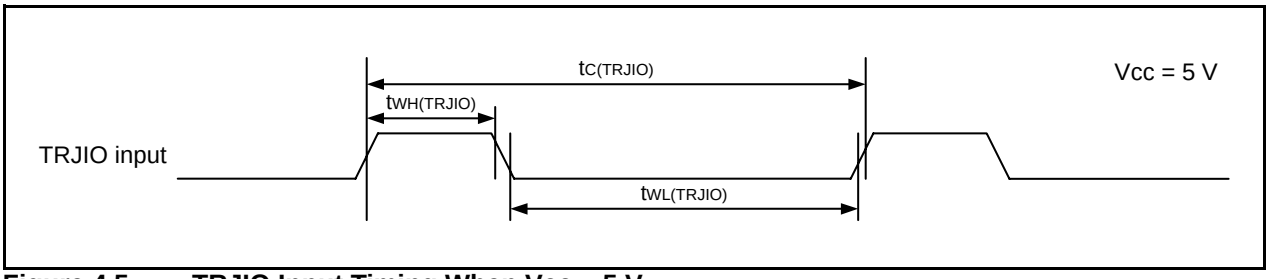


Figure 4.5 TRJIO Input Timing When Vcc = 5 V

Table 4.19 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -5 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 3 V		0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3 V, Vcc = 3.0 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 3.0 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 2.7 V ≤ Vcc < 4.0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

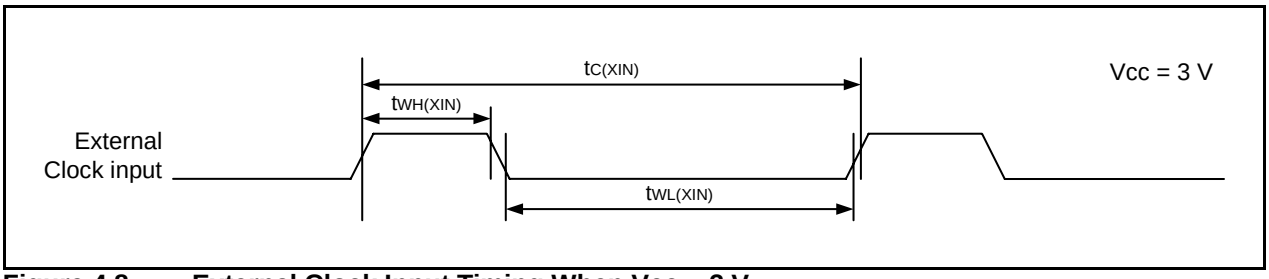


Figure 4.8 External Clock Input Timing When Vcc = 3 V

Table 4.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

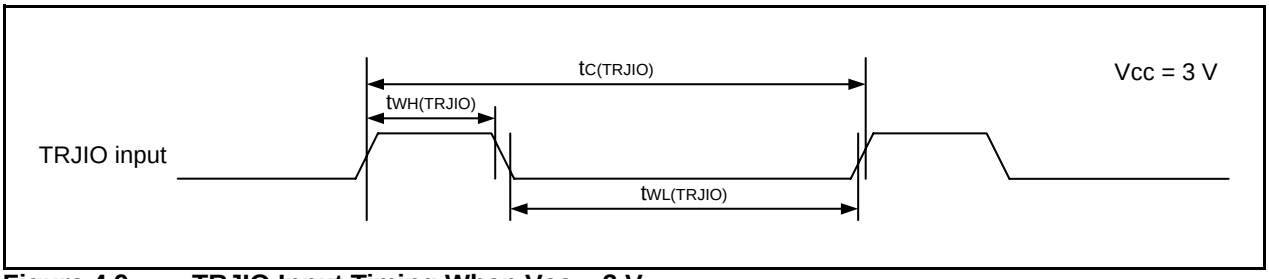


Figure 4.9 TRJIO Input Timing When Vcc = 3 V

Table 4.25 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

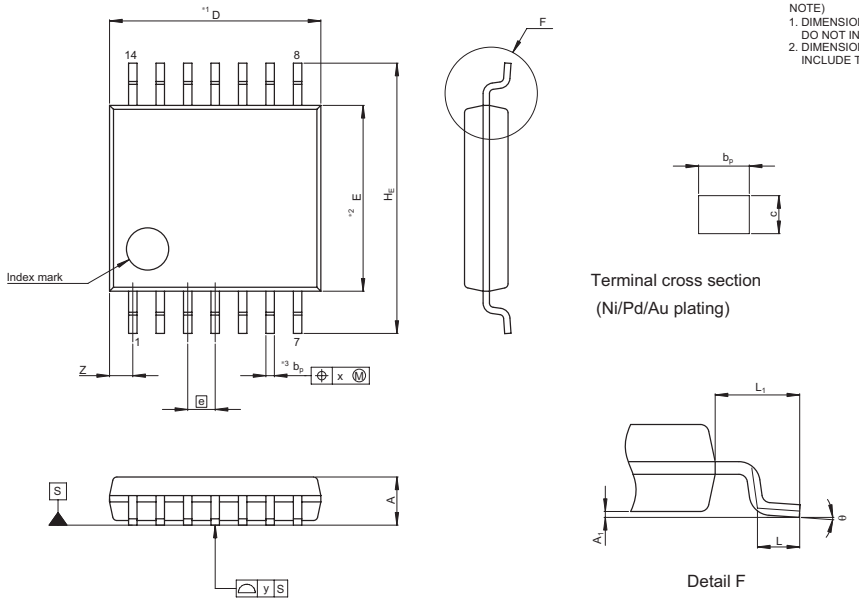
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -2 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 2.2 V		0.05	0.20	—	V
		$\overline{RESET}$	Vcc = 2.2 V		0.05	0.20	—	V
I_{IH}	Input high current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 2.2 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Package Dimensions

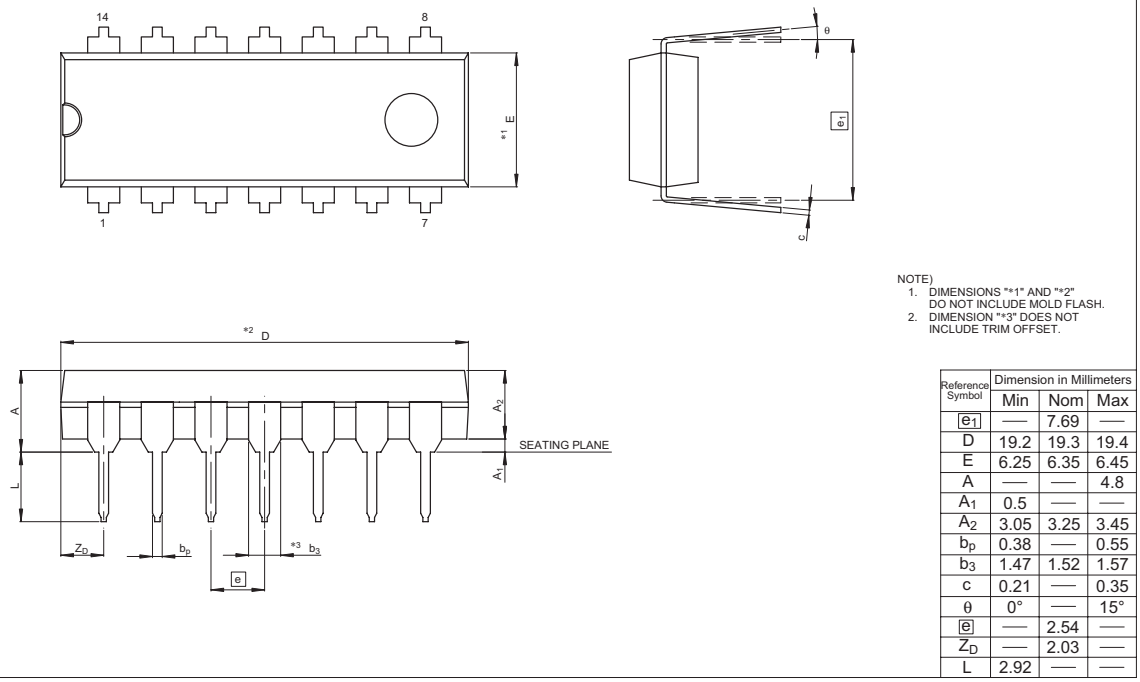
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.35x19.3-2.54	PRDP0014AC-A	14P4X-A	0.94g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.69	—
D	19.2	19.3	19.4
E	6.25	6.35	6.45
A	—	—	4.8
A_1	0.5	—	—
A_2	3.05	3.25	3.45
b_p	0.38	—	0.55
b_3	1.47	1.52	1.57
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	2.03	—
L	2.92	—	—