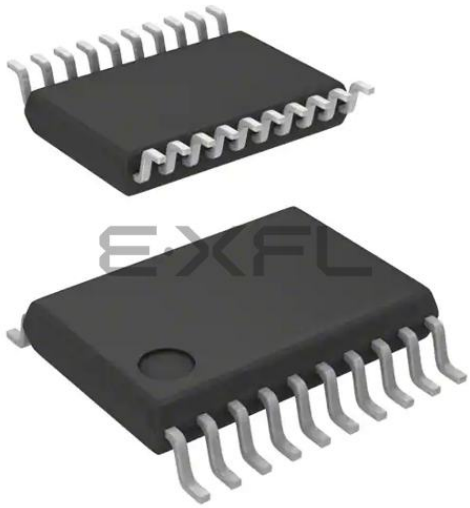

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m122ansp-u0

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:
1. Specify the D version if it is to be used.

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

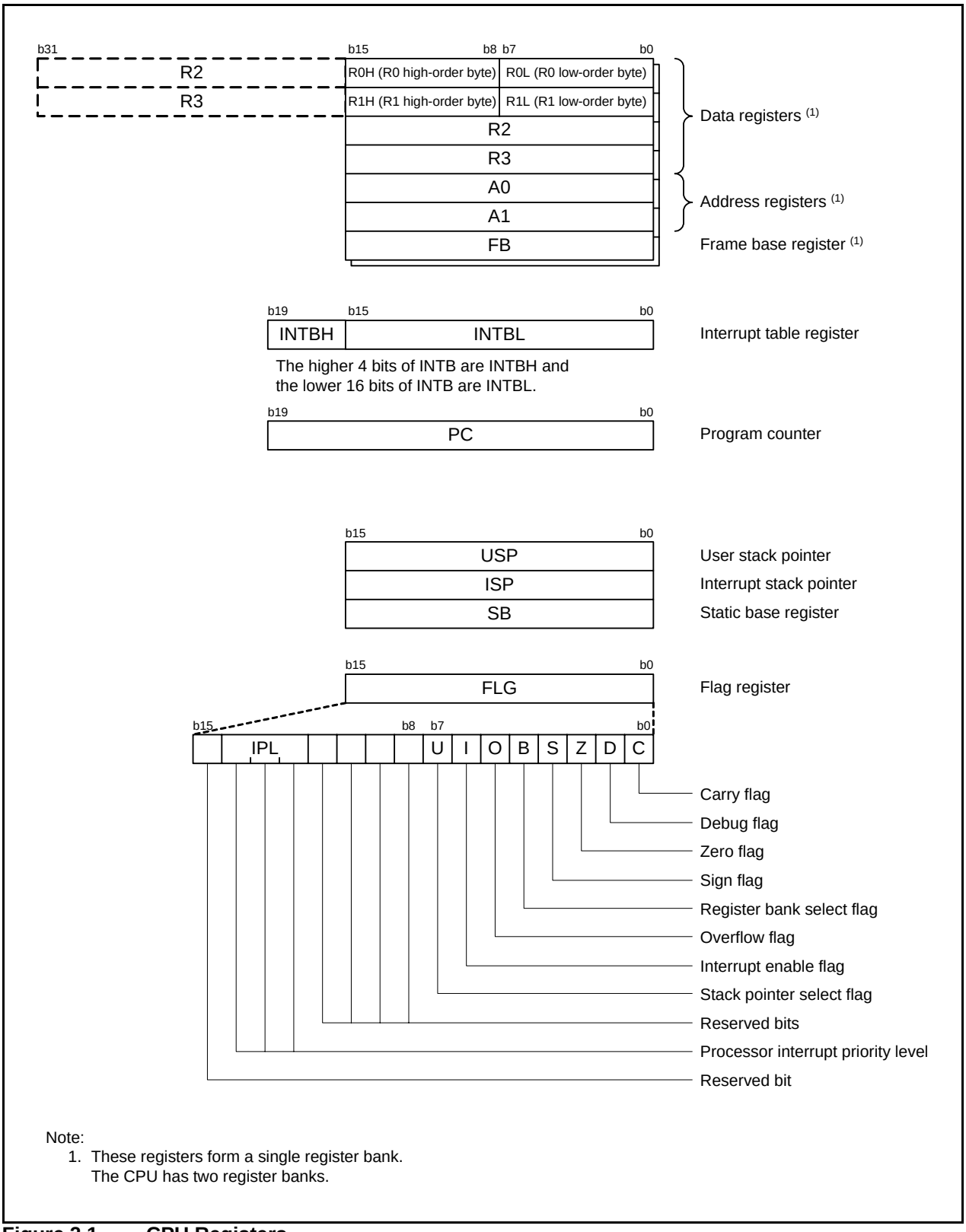
Table 1.7 Pin Functions

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled. If IPL is set to levels from 2 to 7, all maskable interrupt requests are disabled.

2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h			
00131h			
00132h			
00133h			
00134h			
00135h			
00136h			
00137h			
00138h			
00139h			
0013Ah			
0013Bh			
0013Ch			
0013Dh			
0013Eh			
0013Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
0FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
0FFDFh	ID1		(Note 2)
:			
0FFE3h	ID2		(Note 2)
:			
0FFEBh	ID3		(Note 2)
:			
0FFEFh	ID4		(Note 2)
:			
0FFF3h	ID5		(Note 2)
:			
0FFF7h	ID6		(Note 2)
:			
0FFFBh	ID7		(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 4.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Power supply voltage			1.8	—	5.5	V
V_{SS}/AV_{SS}	Power supply voltage			—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input		0.8 Vcc	—	Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
V_{IL}	Input low voltage	Other than CMOS input		0	—	0.2 Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
$I_{OH(sum)}$	Peak sum output high current	Sum of all pins $I_{OH(peak)}$		—	—	-160	mA
$I_{OH(sum)}$	Average sum output high current	Sum of all pins $I_{OH(avg)}$		—	—	-80	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high (5)	—	—	-40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high (5)	—	—	-20	mA
$I_{OL(sum)}$	Peak sum output low current	Sum of all pins $I_{OL(peak)}$		—	—	160	mA
$I_{OL(sum)}$	Average sum output low current	Sum of all pins $I_{OL(avg)}$		—	—	80	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high (5)	—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high (5)	—	—	20	mA
$f_{(XIN)}$	XIN oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz
fHOCO	High-speed on-chip oscillator oscillation frequency (3)		1.8 V ≤ Vcc ≤ 5.5 V	—	20	—	MHz
fLOCO	Low-speed on-chip oscillator oscillation frequency (4)		1.8 V ≤ Vcc ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f_S	CPU clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

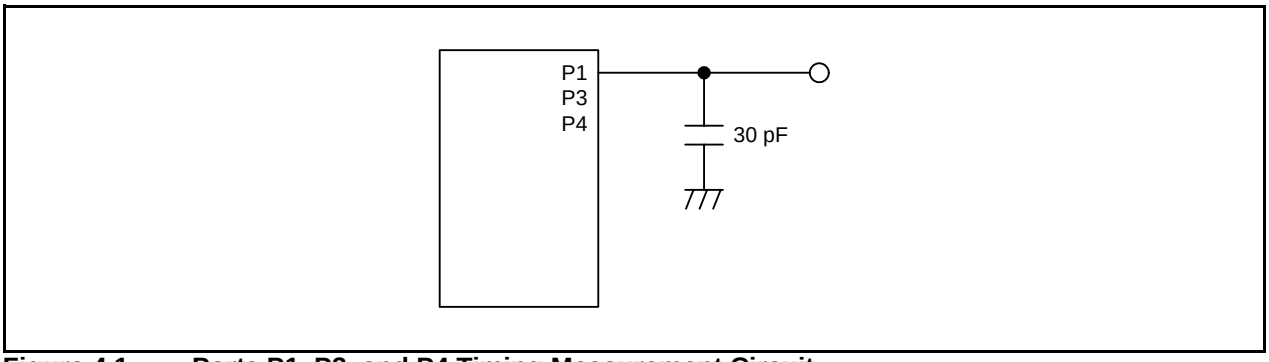


Figure 4.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 4.3 A/D Converter Characteristics

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	10	Bit
—	Absolute accuracy	AVcc = 5.0 V	AN0 to AN4, AN7 input	—	—	±3	LSB
		AVcc = 3.0 V	AN0 to AN4, AN7 input	—	—	±5	LSB
		AVcc = 1.8 V	AN0 to AN4, AN7 input	—	—	±5	LSB
—	A/D conversion clock	4.0 V ≤ AVcc ≤ 5.5 V (2)		2	—	20	MHz
		3.2 V ≤ AVcc ≤ 5.5 V (2)		2	—	16	MHz
		2.7 V ≤ AVcc ≤ 5.5 V (2)		2	—	10	MHz
		1.8 V ≤ AVcc ≤ 5.5 V (2)		2	—	5	MHz
—	Permissible signal source impedance				3		kΩ
t_{CONV}	Conversion time	AVcc = 5.0 V, A/D conversion clock = 20 MHz		2.20	—	—	µs
t_{SAMP}	Sampling time	A/D conversion clock = 20 MHz		0.80	—	—	µs
V_{IA}	Analog input voltage			0	—	AVcc	V

Notes:
1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

Table 4.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc - 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 4.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

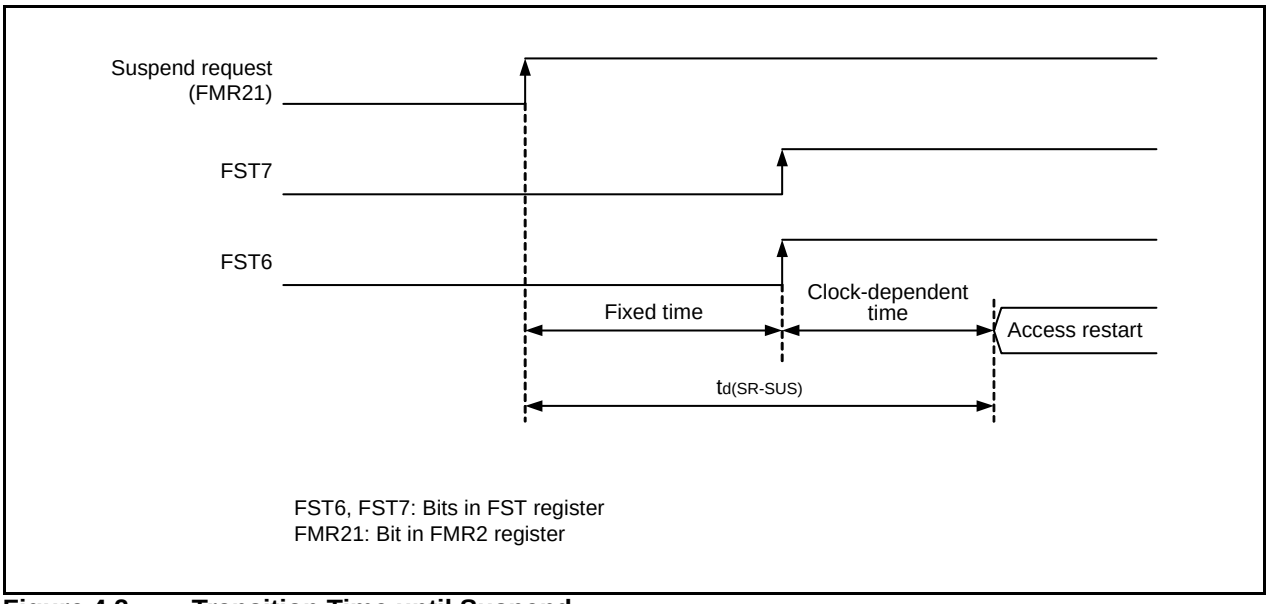


Figure 4.2 Transition Time until Suspend

Table 4.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	µs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 4.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_1 (2)	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 (2)	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 (2)	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 (2)	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 (2)	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B (2)	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D (2)	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F (2)	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	µs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Package	Condition	Standard			Unit
				Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	19.2	20.0	20.8	MHz
		14-pin DIP 20-pin DIP		19.0	20.0	21.0	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register (2)	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	17.694	18.432	19.169	MHz
		14-pin DIP 20-pin DIP		17.510	18.432	19.353	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	17.510	18.432	19.353	MHz
—	Oscillation stabilization time	—		—	—	30	µs
—	Self power consumption at oscillation	—	Vcc = 5.0 V, Topr = 25 °C	—	530	—	µA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stabilization time		—	—	35	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	2	—	µA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

Table 4.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 4.13 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -20 mA	Vcc - 2.0	—	Vcc	V
			When drive capacity is low	I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 5 mA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 5 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.15 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

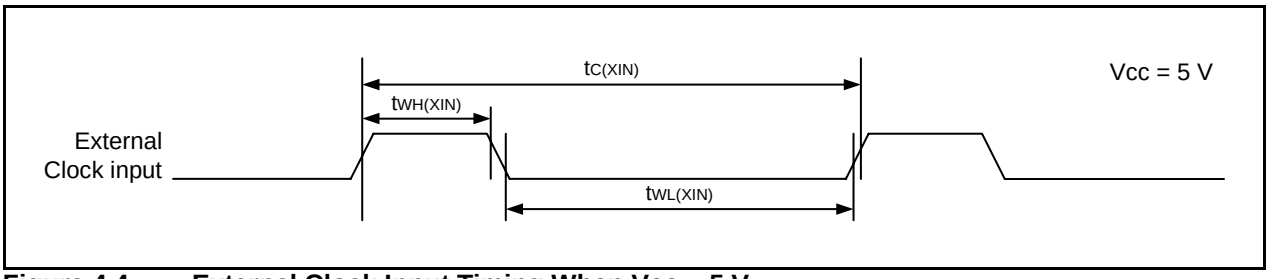


Figure 4.4 External Clock Input Timing When Vcc = 5 V

Table 4.16 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns

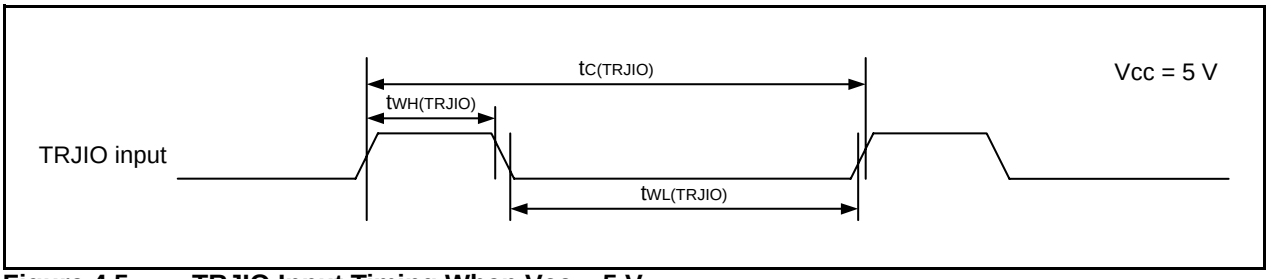


Figure 4.5 TRJIO Input Timing When Vcc = 5 V

Table 4.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{W(CKH)}$	CLK0 input high width	100	—	ns
$t_{W(CKL)}$	CLK0 input low width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

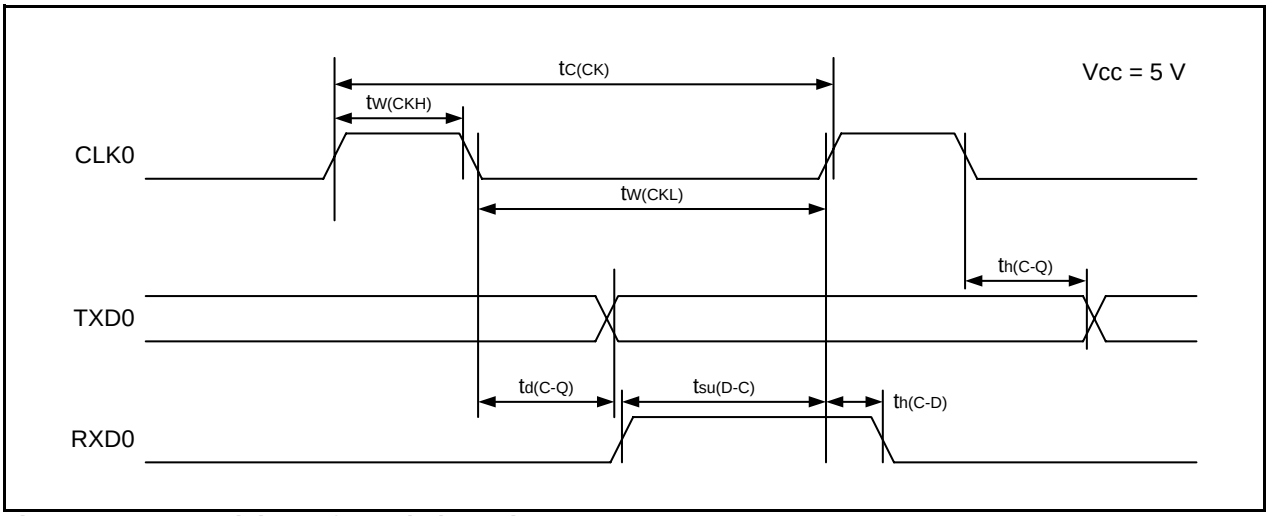


Figure 4.6 Serial Interface Timing When Vcc = 5 V

Table 4.18 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	250 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

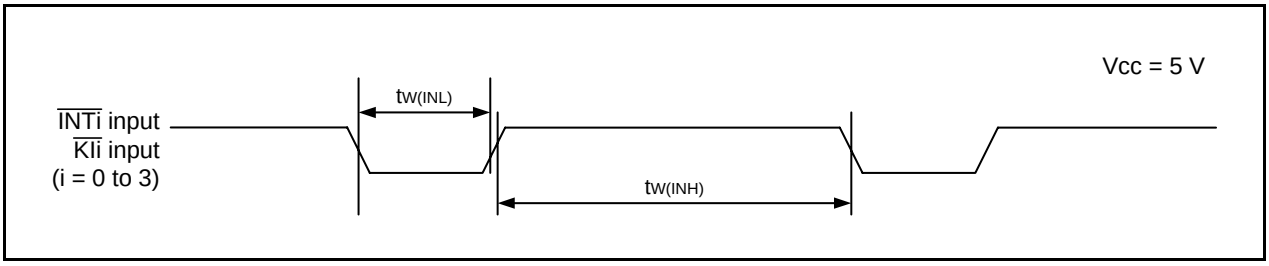


Figure 4.7 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 5 V

Table 4.20 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3.0	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.6	5.0	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	0.9	4.5	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	10 MHz (4)	125 kHz	No division			—	2.2	—	mA
			Off	10 MHz (4)	125 kHz	Division by 8			—	1.4	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	260	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

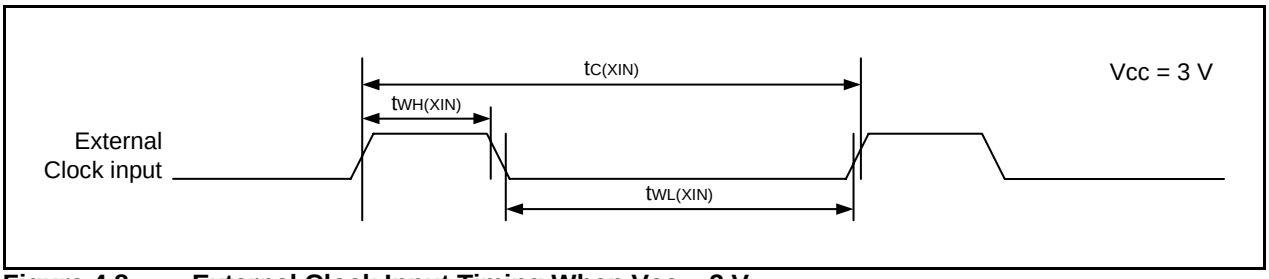


Figure 4.8 External Clock Input Timing When Vcc = 3 V

Table 4.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

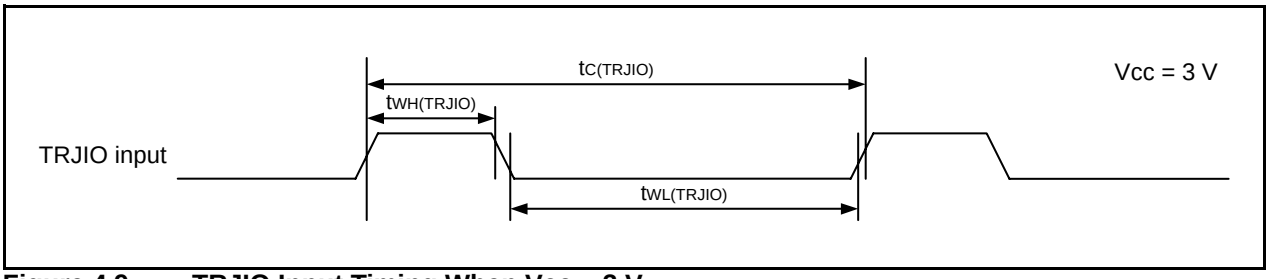


Figure 4.9 TRJIO Input Timing When Vcc = 3 V

Table 4.25 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -2 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 2.2 V		0.05	0.20	—	V
		$\overline{RESET}$	Vcc = 2.2 V		0.05	0.20	—	V
I_{IH}	Input high current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 2.2 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

REVISION HISTORY	R8C/M11A Group, R8C/M12A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan 14, 2010	—	First Edition issued
0.10	Aug 25, 2010	—	Document No. “REJ03B0308” → “R01DS0010EJ”
		2, 3	1.1.2 Differences between Groups added
		4	Table 1.3 “Reset by voltage detection 0” deleted
		5	Table 1.4 “... ROM: VCC = 2.7 V to 5.5 V” → “... ROM: VCC = 1.8 V to 5.5 V”, “1,000 times (program ROM)” → “10,000 times (program ROM)”, Note 1 added
		6	Table 1.5 revised
		8	Figures 1.3 and 1.4 revised
		9	Table 1.6 revised
		11 to 43	2. Central Processing Unit (CPU), 3. Address Space, 4. Electrical Characteristics added
1.00	May 31, 2012	All pages	“Preliminary” and “Under development” deleted
		1	1.1 revised
		3	Table 1.2 revised
		4	Table 1.3 revised
		5	Table 1.4 Note 1 revised
		6	Table 1.5 revised
		10	Table 1.7 revised
		15	Table 3.1 revised
		18	Table 3.4 revised
		23	Table 3.9 Notes 1 and 2 revised
		26	Table 4.3 revised
		31	Table 4.10 and 4.11 revised, Note3 deleted
		45	Package added
2.00	May 31, 2012	4	“Under development” deleted
		9	Table 1.6 “Voltage detection circuit” deleted
		26	Table 4.3 revised