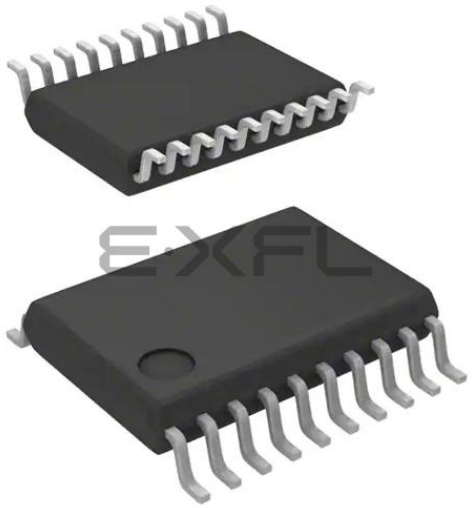
Renesas Electronics America Inc - R5F2M122ANSP#W4 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2m122ansp-w4

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

Related Function	Register Name	Address	Bit	Setting Method for Access
$\overline{\text{INT3}}$	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
$\overline{\text{KI0}}$	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

1.1.3 Specifications

Tables 1.3 and 1.4 outline the Specifications.

Table 1.3 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	See **Table 1.5 Product List**.
Reset sources		• Hardware reset by $\overline{\text{RESET}}$ • Power-on reset • Watchdog timer reset • Software reset • Reset by voltage detection 0
Voltage detection	Voltage detection circuit	Voltage detection with two check points: Voltage detection 0, voltage detection 1 (detection levels selectable)
Watchdog timer		• 14 bits × 1 (with prescaler) • Reset start function selectable • Count source protection function selectable • Periodic timer function selectable
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Clock frequency divider circuit integrated
Power control		• Standard operating mode • Wait mode (CPU stopped, peripheral functions in operation) • Stop mode (CPU and peripheral functions stopped)
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 8 ($\overline{\text{INT}}$ × 4, key input × 4) • Priority levels: 2
I/O ports	Programmable I/O ports	• CMOS I/O: 17 (pull-up resistor selectable) • High-current drive ports: 8
Timer	Timer RJ2	16 bits × 1 Timer mode, pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2	8 bits × 1 (with 8-bit prescaler) or 16 bits × 1 (selectable) Timer mode, programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (output compare function, input capture function), PWM mode (3 outputs), PWM2 mode (1 PWM output)
Serial interface	UART0	Clock synchronous serial I/O. Also used for asynchronous serial I/O.
A/D converter		• Resolution: 10 bits × 6 channels • Sample and hold function, sweep mode
Comparator B		2 circuits

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:
1. Specify the D version if it is to be used.

1.2 Product List

Table 1.5 lists the Product List. Figure 1.1 shows the Product Part Number Structure.

Table 1.5 Product List **Current of May 2012**

Group Name	Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
		Program ROM	Data Flash			
R8C/M11A Group	R5F2M110ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	N version
	R5F2M111ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0014AC-A	
	R5F2M111ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	D version
	R5F2M111ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		
R8C/M12A Group	R5F2M120ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	N version
	R5F2M121ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0020AD-A	
	R5F2M121ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	D version
	R5F2M121ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		

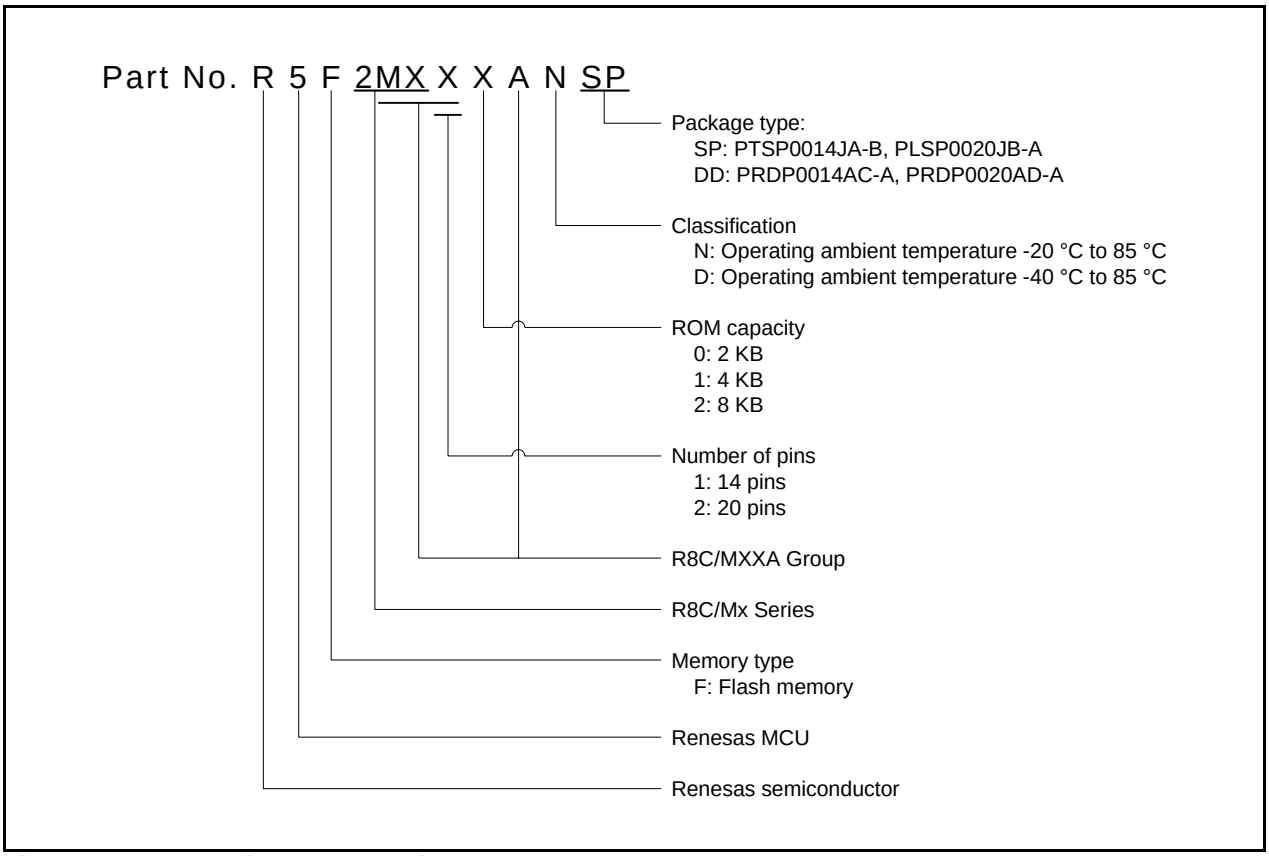


Figure 1.1 Product Part Number Structure

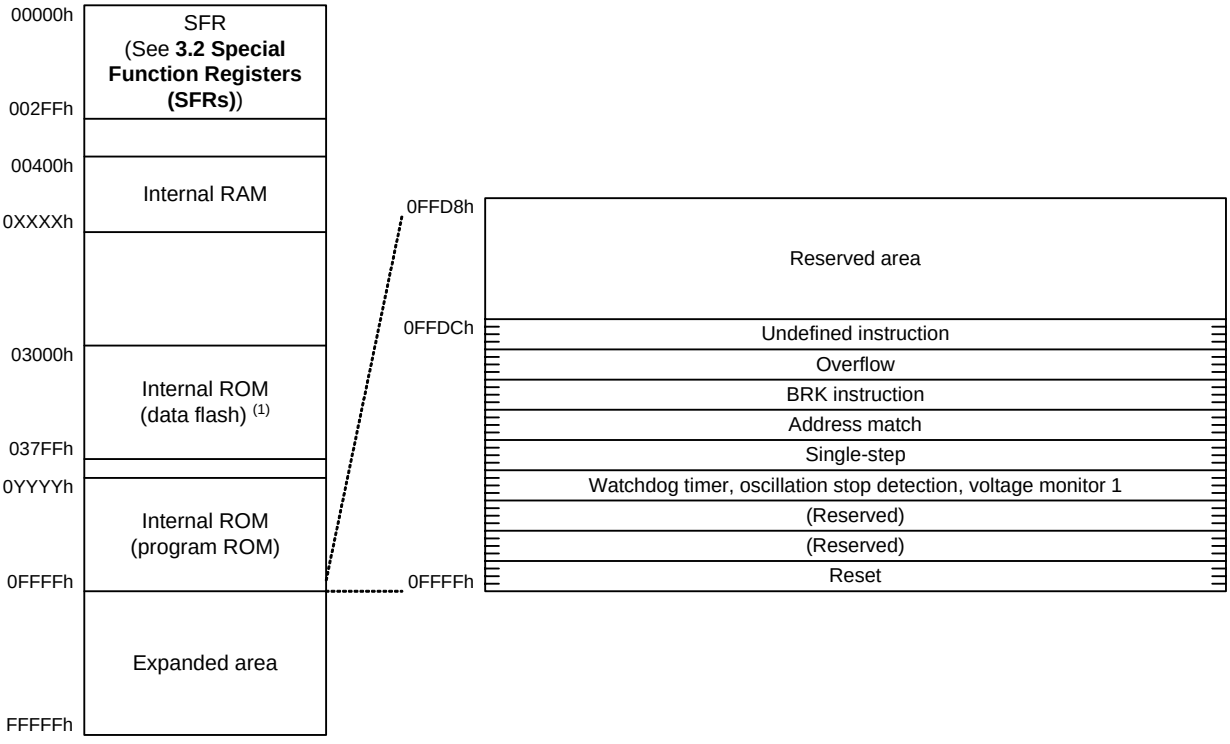
Table 1.6 Pin Name Information by Pin Number

Pin Number		Control Pin	Port	I/O Pins for Peripheral Functions			
R8C/M11A Group	R8C/M12A Group			Interrupt	Timer	Serial Interface	A/D Converter, Comparator B
	1		P4_2	$\overline{KI3}$	TRBO	TXD0	
1	2		P3_7		TRJO/TRCIOD		$\overline{ADTRG}$
2	3	$\overline{RESET}$	PA_0				
3	4	XOUT	P4_7	$\overline{INT2}$			
4	5	VSS/AVSS					
5	6	XIN	P4_6	$\overline{INT1}$	TRJIO	RXD0/TXD0	VCOUT1
6	7	VCC/AVCC					
7	8	MODE					
	9		P3_5	$\overline{KI2}$	TRCIOD		VCOUT3
	10		P3_4	$\overline{INT2}$	TRCIOC		IVREF3
	11		P3_3	$\overline{INT3}$	TRCCLK		IVCMP3
	12		P4_5	$\overline{INT0}$			$\overline{ADTRG}$
8	13		P1_7	$\overline{INT1}$	TRJIO/TRCCLK		AN7/IVCMP1
9	14		P1_6		TRJO/TRCIOB	CLK0	IVREF1
10	15		P1_5	$\overline{INT1}$	TRJIO	RXD0	VCOUT1
11	16		P1_4	$\overline{INT0}$	TRCIOB	RXD0/TXD0	AN4
12	17		P1_3	$\overline{KI3}$	TRBO/TRCIOC		AN3
13	18		P1_2	$\overline{KI2}$	TRCIOB		AN2
14	19		P1_1	$\overline{KI1}$	TRCIOA/TRCTRG		AN1
	20		P1_0	$\overline{KI0}$	TRCIOD		AN0

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte) and block B (1 Kbyte).
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Capacity	Address 0YYYYh	Capacity	Address 0XXXXh
R5F2M110ANSP, R5F2M110ANDD, R5F2M110ADSP, R5F2M120ANSP, R5F2M120ANDD, R5F2M120ADSP	2 Kbytes	0F800h	256 bytes	004FFh
R5F2M111ANSP, R5F2M111ANDD, R5F2M111ADSP, R5F2M121ANSP, R5F2M121ANDD, R5F2M121ADSP	4 Kbytes	0F000h	384 bytes	0057Fh
R5F2M112ANSP, R5F2M112ANDD, R5F2M112ADSP, R5F2M122ANSP, R5F2M122ANDD, R5F2M122ADSP	8 Kbytes	0E000h	512 bytes	005FFh

Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.6 SFR Information (6) (1)

Address	Register Name	Symbol	After Reset
00140h			
00141h			
00142h			
00143h			
00144h			
00145h			
00146h			
00147h			
00148h			
00149h			
0014Ah			
0014Bh			
0014Ch			
0014Dh			
0014Eh			
0014Fh			
00150h			
00151h			
00152h			
00153h			
00154h			
00155h			
00156h			
00157h			
00158h			
00159h			
0015Ah			
0015Bh			
0015Ch			
0015Dh			
0015Eh			
0015Fh			
00160h			
00161h			
00162h			
00163h			
00164h			
00165h			
00166h			
00167h			
00168h			
00169h			
0016Ah			
0016Bh			
0016Ch			
0016Dh			
0016Eh			
0016Fh			
00170h			
00171h			
00172h			
00173h			
00174h			
00175h			
00176h			
00177h			
00178h			
00179h			
0017Ah			
0017Bh			
0017Ch			
0017Dh			
0017Eh			
0017Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time (program/erase endurance ≤ 1,000 times)		—	80	—	µs
—	Byte programming time (program/erase endurance > 1,000 times)		—	160	—	µs
—	Block erase time		—	0.12	—	s
$t_{d(SR-SUS)}$	Transition time to suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = 0 °C to 60 °C, unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple programming operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

Table 4.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

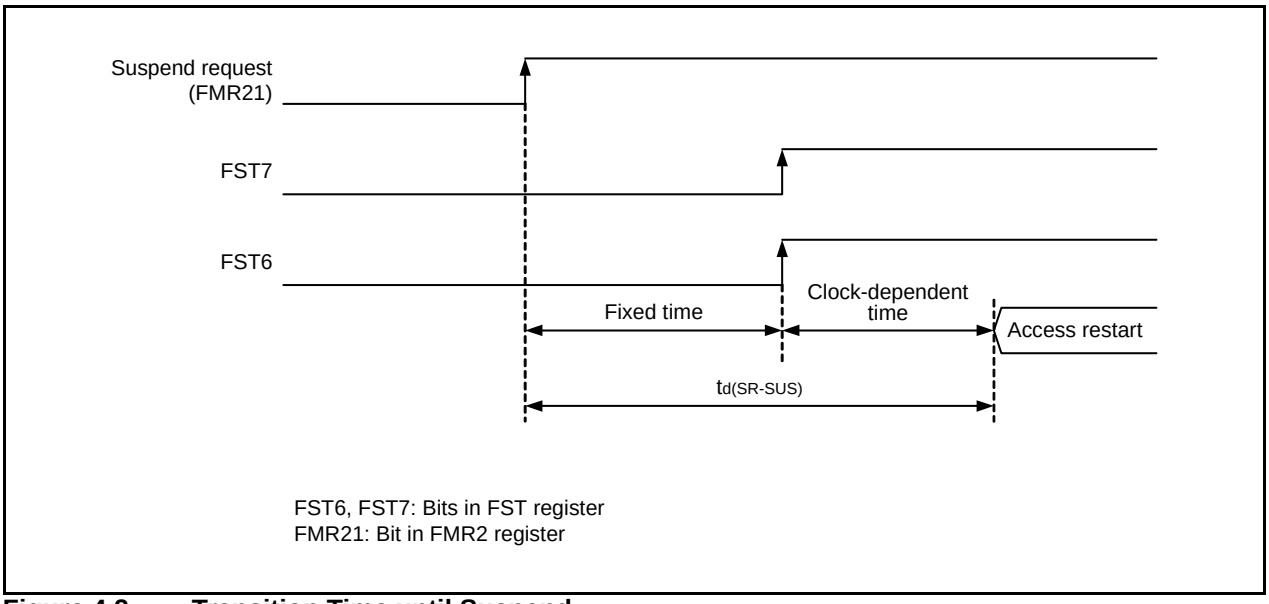


Figure 4.2 Transition Time until Suspend

Table 4.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	µs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 4.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_1 (2)	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 (2)	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 (2)	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 (2)	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 (2)	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B (2)	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D (2)	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F (2)	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	µs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 4.13 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -20 mA	Vcc - 2.0	—	Vcc	V
			When drive capacity is low	I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 5 mA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 5 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 4.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{W(CKH)}$	CLK0 input high width	100	—	ns
$t_{W(CKL)}$	CLK0 input low width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

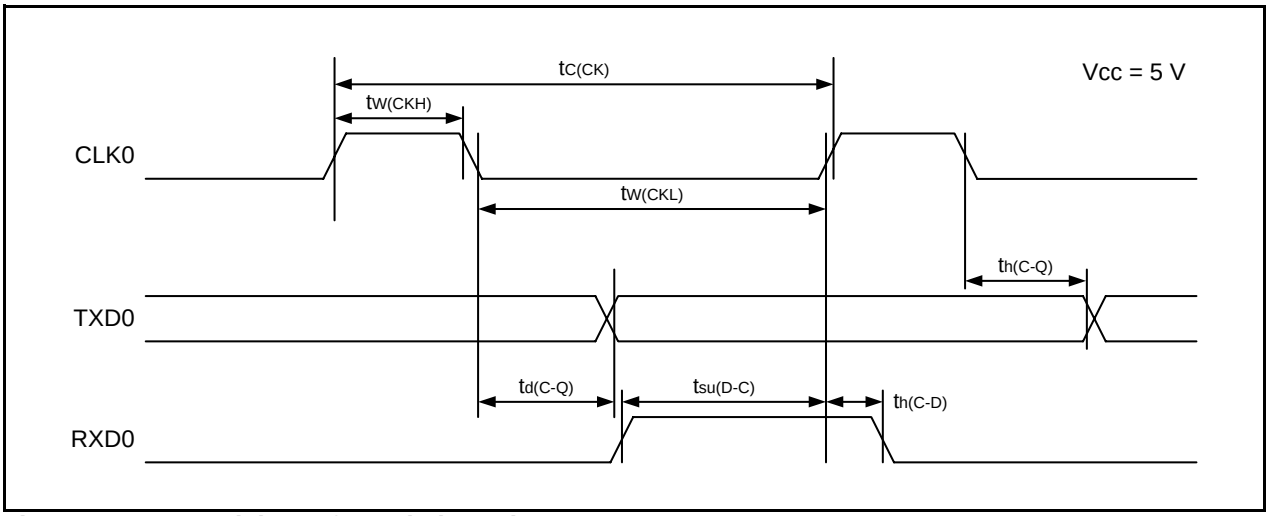


Figure 4.6 Serial Interface Timing When Vcc = 5 V

Table 4.18 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	250 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

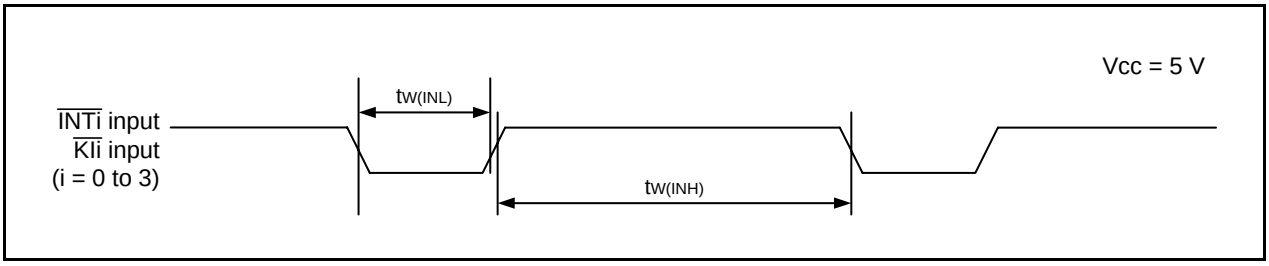


Figure 4.7 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 5 V

Table 4.19 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -5 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 3 V		0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3 V, Vcc = 3.0 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 3.0 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 2.7 V ≤ Vcc < 4.0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 4.20 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3.0	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.6	5.0	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	0.9	4.5	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	10 MHz (4)	125 kHz	No division			—	2.2	—	mA
			Off	10 MHz (4)	125 kHz	Division by 8			—	1.4	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	260	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 4.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

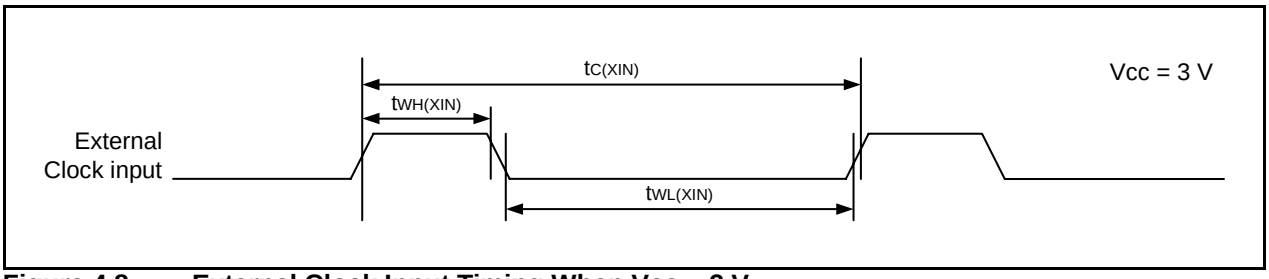


Figure 4.8 External Clock Input Timing When Vcc = 3 V

Table 4.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

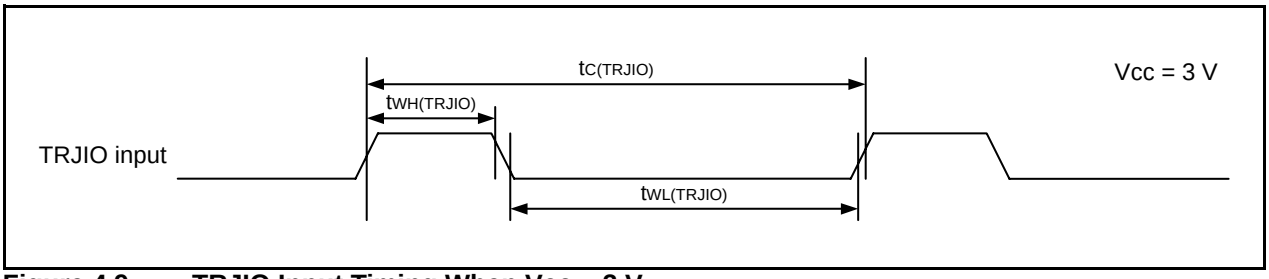


Figure 4.9 TRJIO Input Timing When Vcc = 3 V

Table 4.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{W(CKH)}$	CLK0 input high width	150	—	ns
$t_{W(CKL)}$	CLK0 input low width	150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	70	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

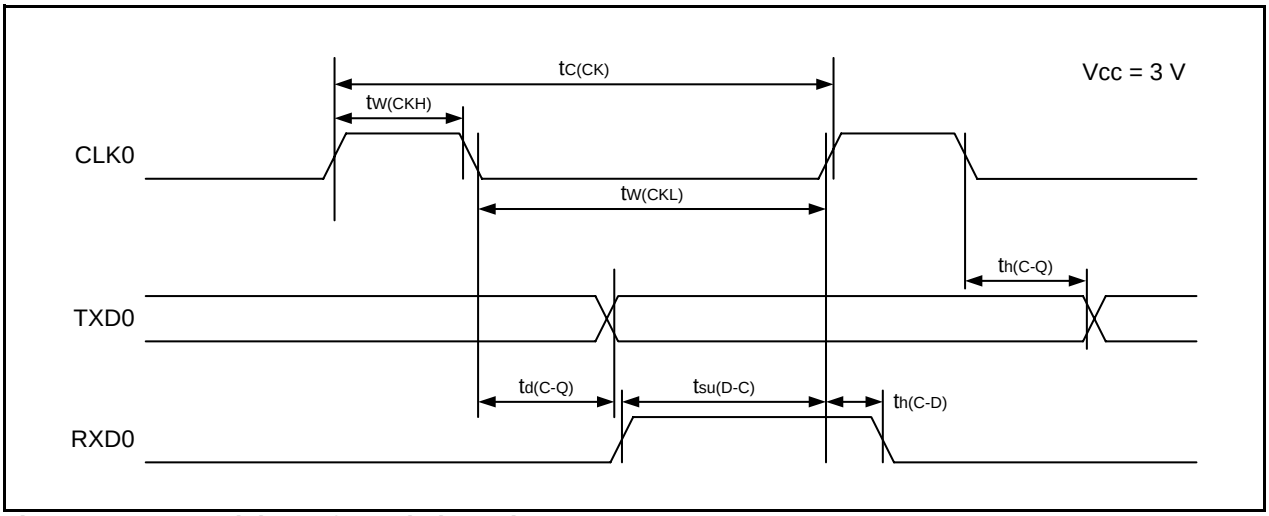


Figure 4.10 Serial Interface Timing When Vcc = 3 V

Table 4.24 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	380 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

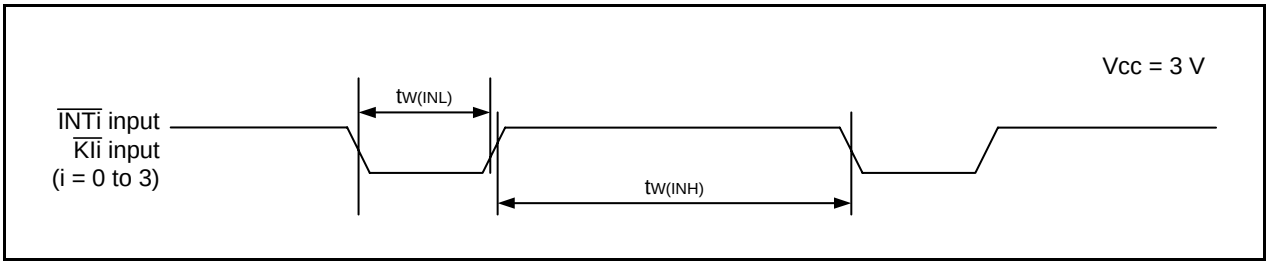


Figure 4.11 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 3 V

Table 4.25 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -2 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 2.2 V		0.05	0.20	—	V
		$\overline{RESET}$	Vcc = 2.2 V		0.05	0.20	—	V
I_{IH}	Input high current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 2.2 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 4.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	—	ns
$t_{W(CKH)}$	CLK0 input high width	400	—	ns
$t_{W(CKL)}$	CLK0 input low width	400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	200	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	150	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

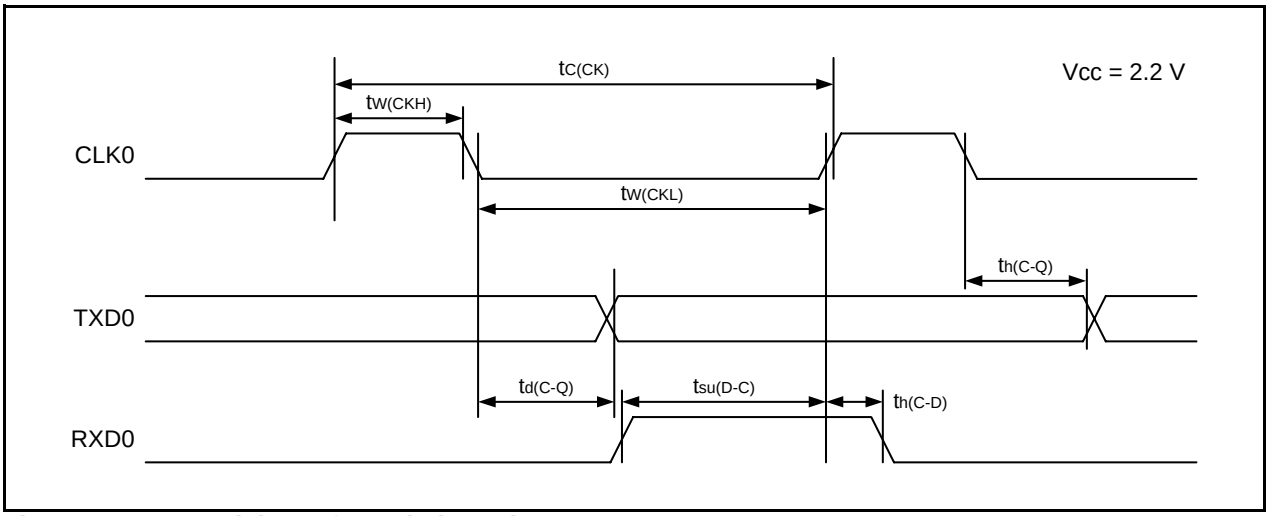


Figure 4.14 Serial Interface Timing When Vcc = 2.2 V

Table 4.30 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	1,000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	1,000 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

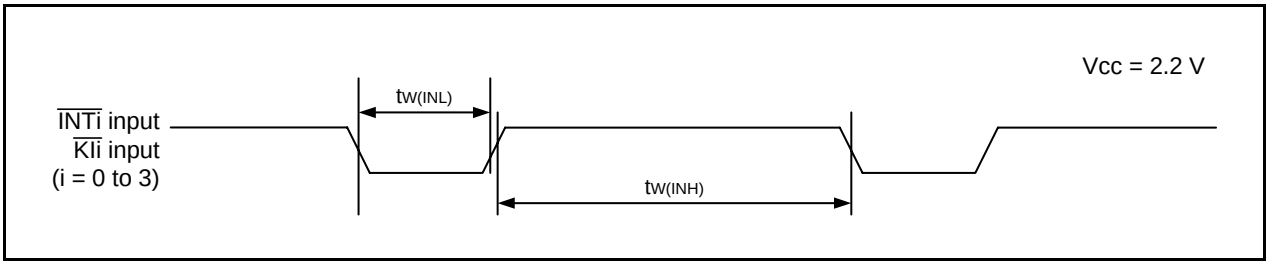
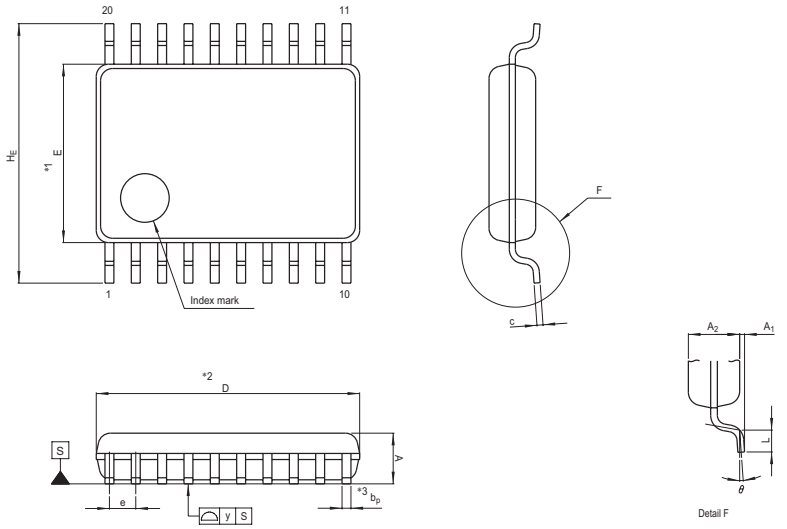


Figure 4.15 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 2.2 V

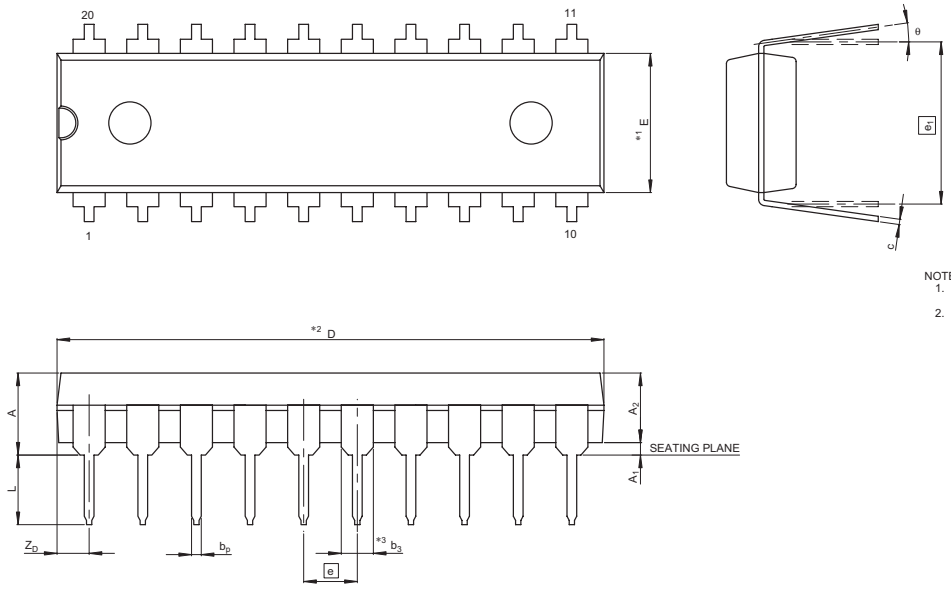
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.6x25.9-2.54	PRDP0020AD-A	20P4X-A	1.39g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.69	—
D	24.9	25.9	26.9
E	6.1	6.6	7.1
A	—	—	5.33
A_1	0.38	—	—
A_2	3.1	3.3	3.5
b_p	0.36	0.46	0.56
b_3	1.32	1.52	1.72
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	1.52	—
L	2.9	—	—