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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	3.6MHz
Connectivity	Serial Port
Peripherals	POR, WDT
Number of I/O	40
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-QFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w925e240fg

1. GENERAL DESCRIPTION

The W925E/C240 is an all in one single 8-bit micro-controller with widely used Calling Identity Delivery (CID) function. The 8-bit CPU core is based on the 8051 family; therefore, all the instructions are compatible to the Turbo 8051 series. The CID part consisted of FSK decoder, DTMF receiver, CPE* Alert Signal (CAS) detector and Ring detector. Also built-in DTMF generator and FSK generator with baud rate 1200 bps (bits/sec). Using W925E/C240 can easily implement the CID adjunct box and the feature phone or Short Message Service (SMS) phone with CID function. The main features are listed in the next section.

2. FEATURES

- **APPLICATION**: The ***SMS*** phone with CID function and CID adjunct box.
- **CPU**: 8-bit micro-controller is similar to the 8051 family.
  - – EEPROM type(E version) operating voltage:
    μC: Depend on the operating vol. option. Either 2.4 to 3.6V or 3.0 to 5.5V for operating. If 2.4 to 3.6V be selected, the μC operating range is from 2.4 to 3.6V, else if 3.0 to 5.5V be selected, the μC operating range is from 3.0 to 5.5V.

    CID: 3.0 to 5.5V.
  - – MASK type(C version) operating voltage:
    μC: 2.2 to 5.5V.

    CID: 3.0 to 5.5V.
- **Dual-clock operation:**
  - – Main oscillator: 3.58MHz crystal for CID and DTMF function. And built-in RC oscillator.
  - – Sub oscillator: 32768Hz crystal.
  - – Main and sub oscillators are enable/disable by bit control individually.
- **ROM**: 256K bytes internal flash EEPROM/MASK ROM type.
  - – Up 128K bytes for program ROM.
  - – Total 256K bytes for look-up table ROM.
  - – Separate 256K into 4 pages, each page is 64K addressable.
- **RAM**:
  - – 256 bytes on chip scratch-pad RAM.
  - – 8K bytes on chip RAM for MOVX instruction.
- **CID**
  - – Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476, British Telecom(BT) SIN227, U.K. Cable Communication Association(CCA) specification.
  - – FSK modulator/demodulator: for Bell 202 and ITU-T V.23 FSK with 1200-baud rate.
  - – CAS detector: for dual tones of Bellcore CAS and BT Idle State and Loop State Dual Tone Alert Signal (DTAS).
  - – DTMF generator/receiver;
  - – Ring detector: for line reversal for BT, ring burst for CCA or ring signal for Bellcore.
  - – Two independent OP amps with adjustable gain for Tip/Ring and Telephone Hybrid connections.

- **I/O**: 40 I/O pins.
  - P0: Bit and byte addressable. I/O mode can be bit controlled. Open drain type.
  - P1~P3: Bit and byte addressable. Pull high and I/O mode can be bit controlled.
  - P4: Byte addressable. Pull high and I/O mode can be bit controlled.

    Note: "CPE*" Customer Premises Equipment
- **Power mode**:
  - **Dual-clock slow operation mode**: System is operated by the sub-oscillator (Fosc=Fs and Fm is stopped)
  - **Idle mode**: CPU hold. The clock to the CPU is halted, but the interrupt, timer and watchdog timer block work normally but CID function is disabled.
  - **Power down mode**: All activity is completely stopped and power consumption is less than 1 μA.
- **Timer**: 2 13/16-bit timers, or 8-bit auto-reload timers, that are Timer0 and Timer1.
- **Watchdog timer**: WDT can be programmed by the user to serve as a system monitor.
- **Interrupt:** 11 interrupt sources with two levels of priority.
  - 4 interrupts from INT0, INT1, INT2 and INT3.
  - 2 interrupts from Timer0, Timer1.
  - 1 interrupt from Serial port.
  - 1 interrupt from CID.
  - 1 interrupt from 13/14-bit Divider.
  - 1 interrupt from Comparator.
  - 1 interrupt from Watch Dog Timer.
- **Divider:** 13/14 bit divider, clock source from sub-oscillator, therefore, DIVF set every 0.25/0.5 second.
- **Comparator:**
  - Comparator: 1 analog inputs from VNEG pin, 2 reference input pins, one is from VPOS pin and another is from internal regulator output.
- **Serial port:**
  - An 8-bit serial transceiver with SCLK and SDATA.
- **Package:**
  - 100pin LQFP: The part numbers are W925E240 & W925C240
  - Lead free 100pin LQFP: The part numbers are W925E240FG & W925G240

4. PIN DESCRIPTION

NAME	I/O	DESCRIPTION
TEST/MODE	I/O	TEST pin. In E version (EEPROM type), it works as a Mode pin to select programming mode. In C version (Mask type), this pin with internal pull-low resistor.
$\overline{EA}$ /DATA	I, I/O	Set high for normal function. In E version, it works as a Data pin. In C version, this pin with internal pull-high resistor.
$\overline{RESET}$ /VPP	I	RESET pin. A low pulse causes the whole chip reset. In E version, this pin works as a VPP pin, which is a supply programming voltage. In C version, this pin with internal pull-high resistor.
RNGDI	I	Ring Detect Input (Schmitt trigger input). Used for ring detection and line reversal detection. Must maintain a voltage between VAD and VAS.
RNGRC	O	Ring RC (Open drain output and Schmitt trigger input). Used to set the time interval from the end of RNGDI pin to the inactive condition of the RNGON pin. An external resistor must connected to VAD and a capacitor connected to V_{SS}, the time interval is the RC time constant.
CAP	O	Must be connected 0.1μF capacitor to V_{SS}.
VREF	O	Reference Voltage. Nominally, VDD/2 is used to bias the input of the gain control op-amp.
GCFB1	O	Op-amp1 Feed-back Gain Control signal. Select the input gain by connecting this pin and the INN1 pin with feedback resistor. It is recommended that the op-amp1 be set to unity gain.
INN1	I	Inverting Input of the gain control op-amp1.
INP1	I	Non-inverting Input of the gain control op-amp1.
GCFB2	O	Op-amp2 Feed-back Gain Control signal. Select the input gain by connecting this pin and the INN2 pin with feedback resistor. It is recommended that the op-amp2 be set to unity gain.
INN2	I	Inverting Input of the gain control op-amp2.
INP2	I	Non-inverting Input of the gain control op-amp2.
VAD	I	Analog voltage supply.
VAS	I	Analog ground.
V_{DD}	I	Digital voltage supply.
V_{SS}	I	Digital ground.
XOUT1	O	Output pin for main-oscillator. Connected to 3.58MHz crystal for CID function.
XIN1	I	Input pin for main-oscillator. Connected to 3.58MHz crystal for CID function.

STACK POINTER (initial=07H)

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

SP: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

DPL: This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

DPH: This is the high byte of the standard 8052 16-bit data pointer.

DATA POINTER LOW1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

DPL1: This is the low byte of the new additional 16-bit data pointer. That has been added to the W925E/C240. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS.0 = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

DATA POINTER HIGH1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

DPH1: This is the high byte of the new additional 16-bit data pointer. That has been added to the W925E/C240. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

IE0: Interrupt 0 edge detects: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT0: Interrupt 0 type control. Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

Bit7~4 control timer 1, bit3~0 control timer0

GATE: Gating control. When this bit is set, Timer x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C/$\overline{T}$: Timer or Counter Select. When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.

Note: X is either 0 or 1.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 13-bits timer
0	1	Mode 1: 16-bits timer
1	0	Mode 2: 8-bits with auto-reload from Thx
1	1	Reserved

TIMER 0 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 low byte register.

TIMER 1 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 low byte register.

P1H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P2 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P2.7H	P2.6H	P2.5H	P2.4H	P2.3H	P2.2H	P2.1H	P2.0H

Mnemonic: P2H Address: 9Eh

P2H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P3 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P3.7H	P3.6H	P3.5H	P3.4H	P3.3H	P3.2H	P3.1H	P3.0H

Mnemonic: P3H Address: 9Fh

P3H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 2 (initial = FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is an I/O port with internal pull-high resistor. P2 can be selected as input or output mode by the P2IO register. At initial reset, P2 is used as input mode. When P2IO is set to 0, P2 is used as CMOS output mode.

HIGH BYTE REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	HB.7	HB.6	HB.5	HB.4	HB.3	HB.2	HB.1	HB.0

Mnemonic: HB Address: A1h

This register contains the high byte address during execution of " MOVX @Ri, " instructions.

P4 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P4.7H	P4.6H	P4.5H	P4.4H	P4.3H	P4.2H	P4.1H	P4.0H

Mnemonic: P4H Address: A2h

PORT 3 (initial = FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: P3 can be selected as input or output mode by the P3IO register, at initial reset, P3IO is set to 0FFH, P3 is used as input mode. When P3IO is set to 00h, the P3 is used as CMOS output mode. Special function of P3 is described below.

P3.5	T1	Timer/Counter 1 external count input
P3.4	T0	Timer/Counter 0 external count input
P3.3	$\overline{INT1}$	External interrupt 1
P3.2	$\overline{INT0}$	External interrupt 0

CID REGISTER (initial = 00H,**read only**)

Bit:	7	6	5	4	3	2	1	0
	-	FCLK	FDATA	FCD	DTMFD	FDR	ALGO	RNG

Mnemonic: CIDR Address: B1h

This SFR indicates the CID signal immediately. Register data is set or cleared by hardware only.

FCLK: FSK serial clock with the baud rate of 1200Hz.

FDATA: FSK serial bit data.

FCD: Set when FSK carrier is detected. Cleared when FSK carrier is disappeared.

DTMFD: Set when DTMF decoded data is ready. Cleared when DTMF signal ends.

FDR: Set when FSK 8 bits data is ready. Cleared before next FSK start bit comes

ALGO: Dual tone Alert signal Guard time detect signal. Set when a guard time qualified dual tone alert signal has been detected. Cleared when the guard time qualified dual tone alert signal is absent.

RNG: Ring detection bit. High to indicate the detection of line reversal and/or ringing.

CID FLAG GENERATOR (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	FSF	DTMFDF	FDRF	ALGOF	RNGF

Mnemonic: CIDFG Address: B2h

FSF: Set when FSK Latch clock low to high. Cleared by software

DTMFDF: Set when DTMFD low to high. Cleared by software

FDRF: Set when FDR low to high. Cleared by software.

ALGOF: Set when ALGO low to high. Cleared by software.

RNGF: Set when RNG low to high. Cleared by software.

CID POWER CONTROL REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	CIDE	-	FSKE	CASE	DTMFE

Mnemonic: CIDPCR Address: B3h

CIDE: Global enable CID function. Low to disable all functions of CID parts.

FSKE: Enable FSK demodulation circuit.

CASE: Enable Dual Tone Alert Signal detection circuit.

DTMFE: Enable DTMF demodulation circuit.

FSK DATA REGISTER (initial = XXH)

Bit:	7	6	5	4	3	2	1	0
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Mnemonic: FSKDR Address: B4h

FD7-0: 8 bits FSK demodulated data.

DTMF DATA REGISTER (initial = XXH)

Bit:	7	6	5	4	3	2	1	0
	CASH	CASL	DTMFH	DTMFL	DD3	DD2	DD1	DD0

Mnemonic: DTMFDR Address: B5h

CASH: Set when Dual Tone Alert Signal high tone is detected.

CASL: Set when Dual Tone Alert Signal low tone is detected.

DTMFH: Set when DTMF high tone is detected.

DTMFL: Set when DTMF low tone is detected.

DD3-0: 4 bits DTMF demodulated data.

DTMF PRESENT TIME REGISTER (initial = 19H)

Bit:	7	6	5	4	3	2	1	0
	DPT7	DPT6	DPT5	DPT4	DPT3	DPT2	DPT1	DPT0

Mnemonic: DTMFPT Address: B6h

The clock period of guard-time timer is 0.8582mS. The default DTMF present time is 21.45mS.

DPT7-0: The pre-set data register for counting DTMF present time. When DTMF is detected(Est, low to high), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of DTMFPT, the exist of the DTMF is accepted. Est changes to low state to stop and reset the counter.

SERIAL DATA BUFFER (initial = 00H) **Read Only**

Bit:	7	6	5	4	3	2	1	0
	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

Mnemonic: SBUF1 Address: C1h

SBUF1.7-0: Serial data on the serial port 1 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive register, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

REGULATOR VOLTAGE CONTROL REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	REGVC.3	REGVC.2	REGVC.1	REGVC.0

Mnemonic: REGVC Address: C2h

REGVC.3-0: 4 bits to tune the regulator output voltage.

POWER MANAGEMENT REGISTER (initial = XXX00001B)

Bit:	7	6	5	4	3	2	1	0
	XT/$\overline{RG}$	RGMD	RGSL	X2OFF	X1OFF	-	-	-

Mnemonic: PMR Address: C4h

XT/$\overline{RG}$:Crystal/RC Oscillator Select. Setting this bit selects crystal or external clock as system clock source. Clearing this bit selects the on-chip RC oscillator as clock source. X1UP (STATUS.4) must be set to 1 and X1OFF (PMR.3) must be cleared before this bit can be set. Attempts to set this bit without obeying these conditions will be ignored.

RGMD: RC Mode Status. This bit indicates the current clock source of micro-controller. When cleared, CPU is operating from the external crystal or oscillator. When set, CPU is operating from the on-chip RC oscillator.

RGSL: RC Oscillator Select. This bit selects the clock source following a resume from Power Down Mode. Setting this bit allows device operating from RC oscillator when a resume from Power Down Mode. When this bit is cleared, the device will hold operation until the crystal oscillator has warmed-up following a resume from Power Down Mode.

X2OFF: Set to disable sub-oscillator (32KHz oscillator)

X1OFF:Crystal Oscillator Disable. Setting this bit disables the external crystal oscillator. This bit can only be set to 1 while the micro-controller is operating from the RC oscillator. Clearing this bit restarts the crystal oscillator, the X1UP (STATUS.4) bit will be set after crystal oscillator warmed-up has completed.

※Please insert at least 5 instructions NOP after X2UP = ”1”& Fsys = Fs (CKCON1.0 = “1”, M/S).

DIVIDER CONTROL (initial = 01H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DIVA

Mnemonic: DIVC Address: C8h

DIVA: Divider available control bit. This bit is set or cleared by software to enable/disable divider. DIVA = 1 to enable the divider. DIVA = 0 to disable the divider. DIVA is reset after reset.

PROGRAM STATUS WORD (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

CY: Carry flag. Set for an arithmetic operation, which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

AC: Auxiliary carry. Set when the previous operation resulted in a carry from the high order nibble.

F0: User flag 0. General-purpose flag that can be set or cleared by the user.

RS.1-0: Register bank select bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

OV: Overflow flag. Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.

F1: User Flag 1. General-purpose flag that can be set or cleared by the user by software.

P: Parity flag. Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

WATCHDOG CONTROL (initial: note)

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	WFS	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

POR: Power-on reset flag. Hardware will set this flag when system is powered on and this flag is cleared only by software.

WFS: Watchdog Timer Frequency Select. Set to select F_S as WDT clock input. Clear to select F_{OSC} as WDT clock input.

WDIF: Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the watchdog timer. If the Watchdog interrupt is enabled (EIE.5), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

EXTENDED INTERRUPT PRIORITY (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	PWDI	PCOMP	PDIV	PCID	PX3	PX2

Mnemonic: EIP Address: F8h

PWDI: Watchdog timer interrupt priority. 0 = Low priority, 1 = High priority.

PCOMP: Comparator interrupt priority. 0 = Low priority, 1 = High priority.

PDIV: Divider Interrupt Priority. 0 = Low priority, 1 = High priority.

PCID: CID Interrupt Priority. 0 = Low priority, 1 = High priority.

PX3: External Interrupt 3 Priority. 0 = Low priority, 1 = High priority.

PX2: External Interrupt 2 Priority. 0 = Low priority, 1 = High priority.

CID GAIN CONTROL DATA (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Mnemonic: CIDGD Address: F9h

CIDGD.7-0: The data value of programmable CID input filter gain and hysteresis.

CID GAIN CONTROL ADDRESS (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	BIT3	BIT2	BIT1	BIT0

Mnemonic: CIDGA Address: FAh

CIDGA.3: The CIDGD latch control signal. Rising high pulse to latch CIDGD into CID gain control register.

CIDGA.2-0: The address to indicate CID input gain control registers.

service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts INT2 to INT3 are edge triggered only.

The TF0, TF1 flags generate the Timer 0, 1 Interrupts. These flags are set by the overflow in the Timer 0, Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the enable bit EIE.5 enables the interrupt, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are one interrupt sources from the Serial block, which are obtained by SF1 in the SCON1. SF1 is cleared automatically when the serial port interrupt is serviced.

The divider interrupt is generated by DIVF that is set when divider overflows. DIVF is set by hardware and cleared when divider interrupt is serviced. The divider interrupt is enable/disable if the bit EDIV is high/low.

The comparator interrupt is produced by COMPF, which is set when the RESC bit is changed from low to high. RESC, which is the real-time result of comparator, set when the voltage of reference input is higher than the voltage of analog input.

The CID interrupt is generated by CIDF. The CIDF is a logic OR output of all CID flags which are set by hardware and cleared by software. The structure of the CID flags is shown in Figure 6-4.

Each of the individual interrupts can be enabled or disabled by setting or clearing the corresponding bits in the IE and EIE SFR. A bit EA, which is located in IE.7, is a global control bit to enable/disable the all interrupt. When bit EA is zero all interrupts are disabling and when bit EA is high, each interrupt is enable individually by the corresponding bit.

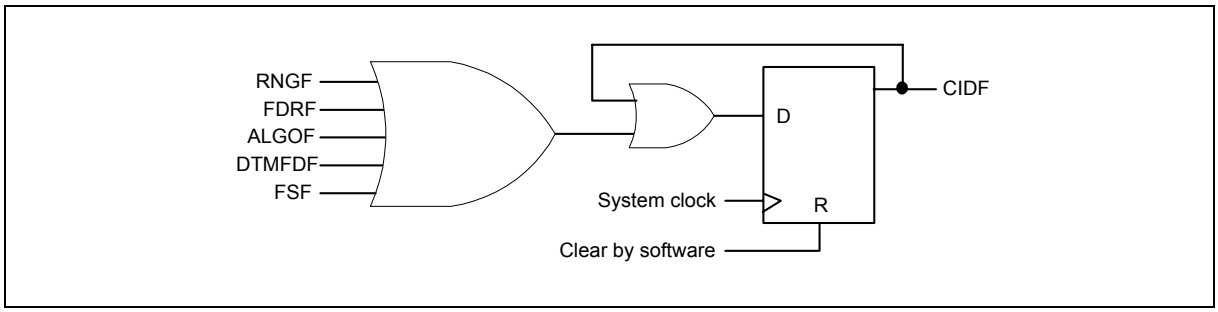


Figure 6-4 The Structure of CID Flags

Priority Level Structure

There are two priority levels for the interrupts, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Table 5 The relation between the tone frequency and the preset value of TM0

		3rd octave			4th octave			5th octave		
		Tone frequency	TM0 preset value & BUZ frequency		Tone frequency	TM0 preset value & BUZ frequency		Tone frequency	TM0 preset value & BUZ frequency	
TONE	C	130.81	83H	131.07	261.63	C1H	260.06	523.25	E1H	528.51
	C #	138.59	8AH	138.84	277.18	C5H	277.69	554.37	E3H	564.96
	D	146.83	90H	146.28	293.66	C8H	292.57	587.33	E4H	585.14
	D #	155.56	97H	156.03	311.13	CBH	309.13	622.25	E6H	630.15
	E	164.81	9DH	165.49	329.63	CEH	327.68	659.26	E7H	655.36
	F	174.61	A2H	174.30	349.23	D1H	348.58	698.46	E9H	712.34
	F #	185.00	A7H	184.09	369.99	D4H	372.35	739.99	EAH	744.72
	G	196.00	ACH	195.04	392.00	D6H	390.08	783.99	EBH	780.19
	G #	207.65	B1H	207.39	415.30	D9H	420.10	830.61	ECH	819.20
	A	220.00	B6H	221.40	**440.00**	**DBH**	**442.81**	880.00	EDH	862.84
	A #	233.08	BAH	234.05	466.16	DDH	468.11	932.23	EEH	910.22
	B	246.94	BEH	248.24	493.88	DF	496.48	987.77	EFH	963.76

Note: Central tone is DB (440 Hz).

WATCHDOG TIMER

The Watchdog timer is a free-running timer that can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is a set of dividers that divides the system clock. The divider output is selectable and determines the time-out interval. In the condition of the timer-out expiring, the WDT interrupt and WDT reset may be executed if the corresponding enables control bits are set. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.

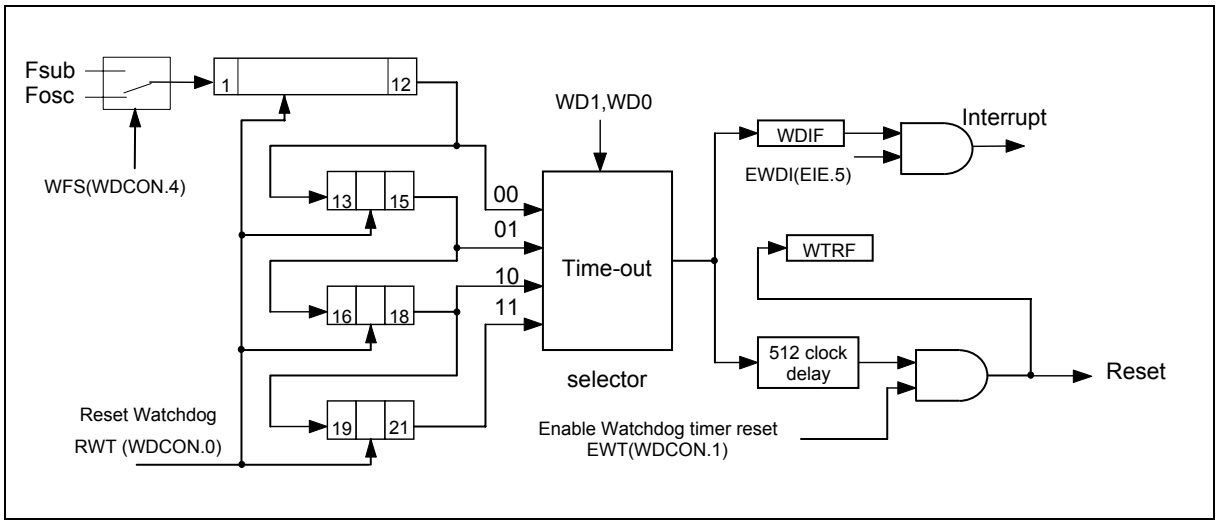


Figure 6-7 Watchdog Timer

When FTE enable will set the FDS to high to enable the internal latch clock in 1200Hz. When FDS is in high state, FSKTB bit0 will be sent out by FSK modulator at the rising edge of latch clock. FDS could be cleared by software to inform no more data will be sent out after the last bit is sent completely. If the FDS is cleared then FTE will become low at next rising latch clock to disable FSK modulator and clear FDS by hardware automatically.

When FTE is set, FSK modulation flag (FSF) will be set at every rising edge of latch clock to produce an interrupt shared with CID interrupt routine. If a CID interrupt occurs, user can check FSF to know if this interrupt is caused by FSK modulator. The only way to stop FSK signal immediately is to disable FTE by software.

6.13 I/O Ports

There are five 8-bits ports named from P0 to P4 in W925E/C240. All ports can be configured as input or output mode. Except P0, every port has pull high resistor enable/disable by PxH register. After reset the initial state of each port is in input mode and the value of the registers from P0 to P3 are FFh. The I/O port is described as below:

P0: I/O mode is controlled by P0IO. Only **P0 output as open drain mode** and without pull high resistor.

P1: I/O mode is controlled by P1IO. Pull high is controlled by P1H. **P1.0~P1.3 work as INT2**, **P1.4~P1.7 work as INT3**. **Falling edge** on P1 pins to produce INT2 and INT3 flag. P1 is configured as INT2/INT3 by P1EF register.

P2: I/O mode is controlled by P2IO. Pull high is controlled by P2H.

P3: I/O mode is controlled by P3IO. Pull high is controlled by P3H.

P3.5	T1	Timer/counter 1 external count input
P3.4	T0	Timer/counter 0 external count input
P3.3	$\overline{\text{INT1}}$	External interrupt 1
P3.2	$\overline{\text{INT0}}$	External interrupt 0

P4: I/O mode is controlled by P4IO. Pull high is controlled by P4H.

Special function of P4 is described below.

P4.7-5	I/O	Normal I/O
P4.4	VPOS	Positive input of the comparator
P4.2	VNEG	Negative input of the comparator
P4.1	SDATA	Serial port output
P4.0	SCLK	Serial port input

6.14 Divider

A built-in 13/14-bit binary up counter designed to generate periodic interrupt. The clock source is from sub-oscillator. When the frequency of sub-crystal is 32768Hz, it provides the divider interrupt in the period of 0.25/0.5 second. Bit DIVS controls the degree of divider. When DIVA is high to enable the divided counter, when DIVA is low to reset divider and stop counting. As the divider overflows, the divider interrupt flag DIVF is set. DIVF is clear by software or serving divider interrupt routine.

Ring Detector

The application circuit in Figure 6-15 illustrates the relationship between the RNGDI, RNGRC and RNG signals. The combination of RNGDI and RNGRC is used to detect an increase of the RNGDI voltage from ground to a level above the Schmitt trigger high going threshold voltage V_{T+}.

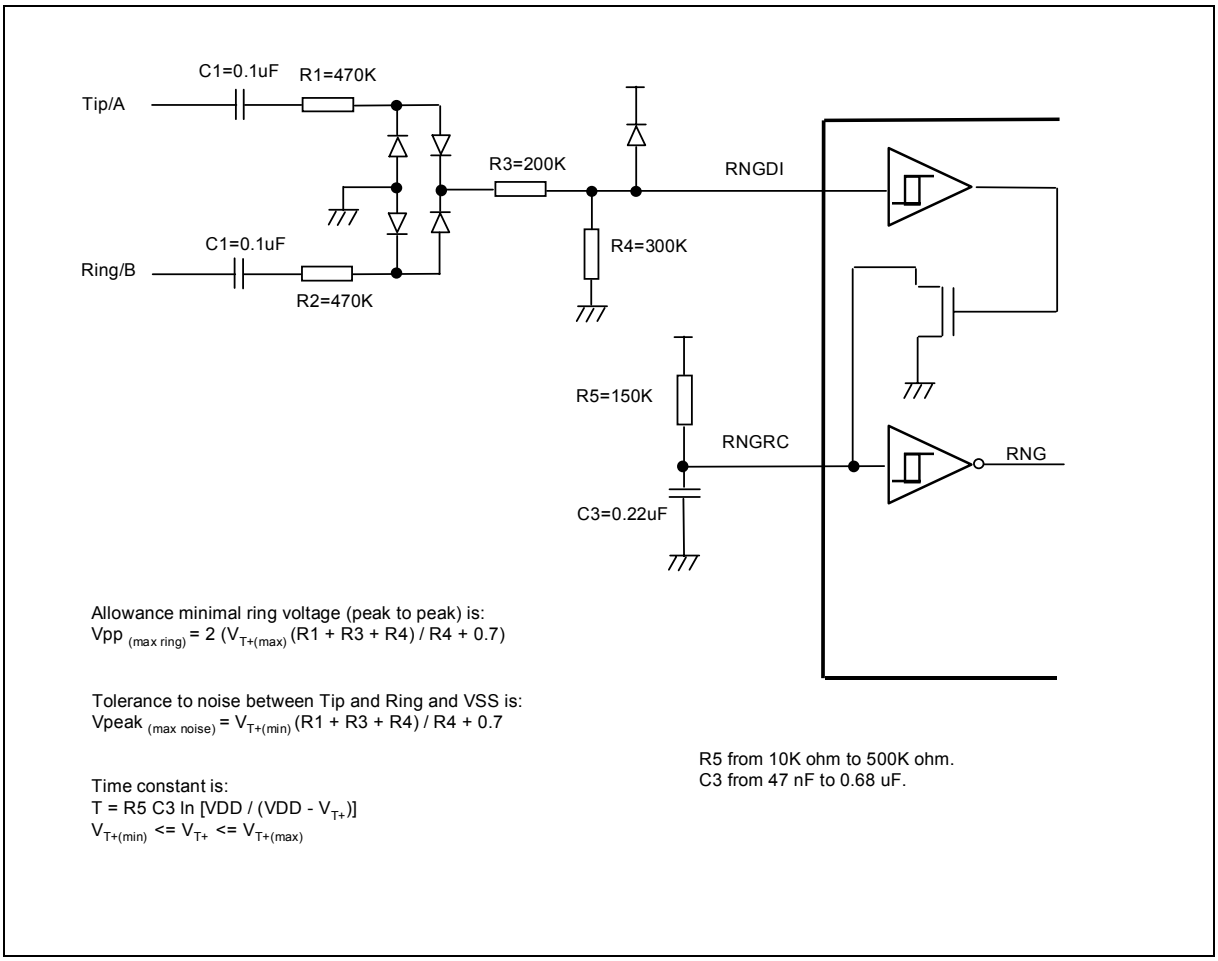


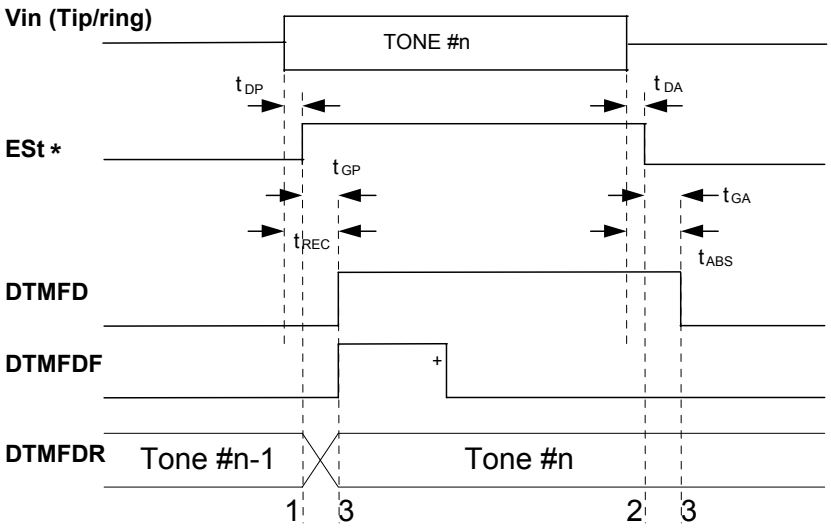
Figure 6-15 Application Circuit of the Ring Detector

The RC time constant of the RNGRC pin is used to delayed the output pulse of the RNG flag for a low going edge on RNGDI. This edge goes from above the V_{T+} voltage to the Schmitt trigger low going threshold voltage V_{T-}. The RC time constant must be greater than the maximum period of the ring signal, to ensure a minimum RNG high interval and to filter the ring signal to get an envelope output. The rising signal of RNG will set the bit RNGF(CIDFG.0) high to cause the CID flag(CIDF) high.

The diode bridge shown in Figure 6-15 works for both single ended ring signal and balanced ringing. The R1 and R2 are used to set the maximum loading and must be of equal value to achieve balanced loading at both the tip and ring line. R1, R3 and R4 form a resistor divider to supply a reduced voltage to the RNGDI input. The attenuation value is determined by the detection of minimal ring voltage and maximum noise tolerance between tip/ring and ground.

DTMF Decoder

The DTMF decoder shares the same input pre-processor with FSK decoder. The dual tone is separated into low group and high group by two SCFs (switched capacitor filter. The method of DTMF detection is the same as alert tone detection. The present/absent guard time is adjusted by registers DTMFPT/DTMFAT. As the DTMF signal is recognized and decoded, the bit DTMFD will be set and the decoded DTMF data is stored in bit0 to bit3 of register DTMFDR. The rising edge of DTMFD produces the flag DTMFDF. The bit DTMFD is controlled by hardware only. The flag DTMFDF is set by rising edge of DTMFD and cleared by software.



1: Guard time timer is reset and starts to up count from 00H.
2: Guard time timer is reset and starts to up count from 00H.
3: The content of the up counting timer reaches the register DTMFPT/DTMFAT.

* ESt is an internal signal in the circuit.
\+ Clear by software.

Figure 6-19 The Waveform of DTMF Detection

Tone Detector

In off-hook state, said type II system, detecting tone alert signal(CAS) is easily interfered by human's voice or other noise in voice band. Sometimes the interference makes falsely recognizing a noise as a CAS(talk-off), or lost detecting a real CAS(talk-down). The DTMF can be programmed as a tone detector by setting bit 4 of DTMFR2. The frequency band of the tone detector is DTMF frequency from 697Hz to 1633Hz. Once the tone detector gets signals in the band, the bit of DTMFH or DTMFL in register DTMFDR will become high immediately. User can poll these 2 bits to check if the tone exists on the tip/ring. The input gain of tone detector is the same as DTMF receiver.

FSK Decoder

The FSK carrier detector provides an indication of the present of a signal within the FSK frequency band. If the output amplitude of the FSK band-pass filter is sufficient to be detected continuously for 8 mS, the FSK carrier detected bit FCD will go high and it will be released if the FSK band-pass filter output amplitude is not able to be detected for greater than 8 mS. The 8 mS is the hysteresis of the FSK carrier detector. Figure 6-20 shows the timing of FSK carrier detection.

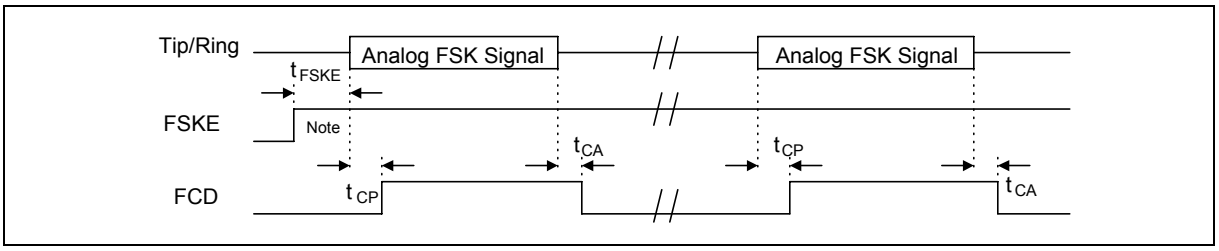


Figure 6-20 FSK Detection Enable and FSK Carrier Present and Absent Timing

The FSK demodulation function can demodulate Bell 202 and ITU-T V.23 Frequency Shift keying (FSK) with 1200-baud rate. When the decoder receives the FSK serial data, the serial data will be demodulated into bit FDATA with 1200-baud rate in the mean time the synchronous clock signal is output to the bit FCLK. As the decoder receives one byte, the internal serial-to-parallel circuit sets the bit FDR and converts the 8-bit serial data into the byte register FSKDR. The rising edge of bit FDR will set the flag FDRF to produce CID interrupt but FDRF is cleared by software. User can get the FSK data by reading register FSKDR or sampling the bit FDATA. The timing of FSK demodulation is shown in Figure 6-21.

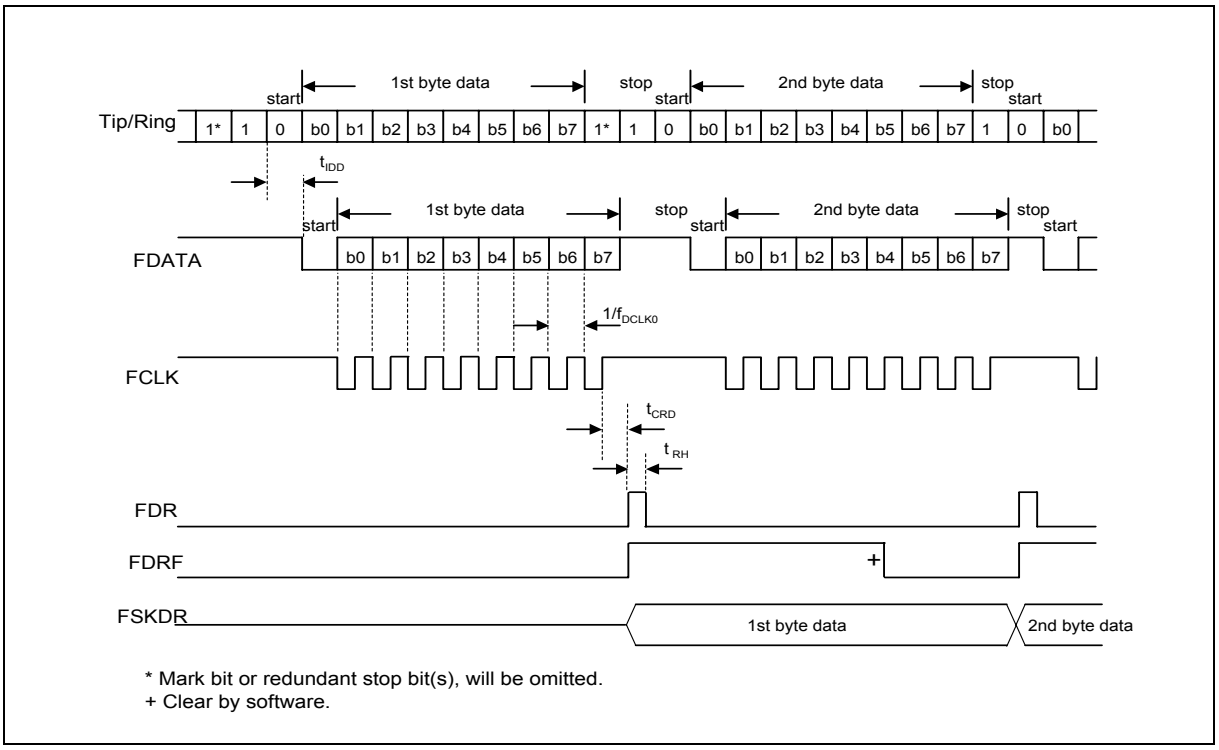


Figure 6-21 Serial Data Interface Timing of FSK Demodulation

8.3 DC Characteristics

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Operating Current	I_{OP1}	FSK On, dual clock, normal run		2.8		mA	
	I_{OP2}	FSK Off, dual clock, normal run		1.3		mA	
	I_{OP3}	FSK off, slow run, main osc stopped		50		uA	
	I_{OP4}	Idle mode, dual clock		500		uA	
	I_{OP5}	Idle mode, main osc stopped		50		uA	
	I_{OP6}	Power down mode			1	uA	
I/O Ports Input High Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}	V	
I/O Ports Input Low Voltage	V_{IL}		V_{SS}		$0.3V_{DD}$	V	
I/O Ports Output High Voltage	V_{OH}	I_{OH} = 2.0 mA	2.4	-	-	V	
I/O Ports Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	-	-	0.4	V	
BUZ Pin Output High Voltage	V_{BOH}	I_{OH} = 3.5 mA	2.4	-	-	V	
BUZ Pin Output High Voltage	V_{BOL}	I_{OL} = 3.5mA	0.4	-	-	V	
DTMF Output DC Level	V_{TDC}	R_L = 5KΩ, V_{DD} = 2.5-3.8	1.1	-	2.8	V	
DTMF Distortion	DTHD	R_L = 5KΩ, V_{DD} = 2.5-3.8	-	-30	-23	dB	
DTMF Output Voltage	V_{TO}	Low group, R_L = 5KΩ	130	150	170	mV rms	
Pre-emphasis		Col/Row	1	2	3	dB	
FSK Output DC Level	V_{FDC}	R_L = 5KΩ, V_{DD} = 2.5-3.8	1.1	-	2.8	V	
FSK Distortion	FTHD	R_L = 5KΩ, V_{DD} = 2.5-3.8	-	-	-30	dB	
FSK Output Voltage	VFD	RL = 5KΩ	75	150	170	mV rms	

DTMF Decoder

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Sensitivity per tone		-29		1	dBm	1, 2
Positive and negative twist accept		7			dB	1, 2
Frequency Deviation accept		1.5			%	1, 2
Frequency Deviation reject		3.5			%	1, 2
3rd Tone Tolerance				-16	dB	1, 2, 3
Noise Tolerance				-12	dB	1, 2, 3
Dial tone Tolerance			22		dB	1, 2, 4

Notes :

1. signal consists of all DTMF tones.
2. Tone duration is 40 mS at least, tone pause duration is 40 mS at least.
3. Referenced to the lowest level frequency component in DTMF signal.
4. Referenced to the minimum valid accept level.

DTMF Detection Interface

PARAMETER	CONDITION	SYM.	MIN.	TYP‡	MAX.	UNITS	NOTES
DTMF present detect time	Est	t_{FP}	0.5		8	mS	
DTMF absent detect time		t_{FA}	0.1		8	mS	
DTMF Detected Duration	DTMFD = 1	t_{DD}	40			mS	
DTMF Signal Ignore Time	DTMFD = 0	t_{DI}			20	mS	
DTMF Pause Accept Time	DTMFD = 1	t_{DPA}	20			mS	

"‡" Typical figure are at V_{DD} = 5V and temperature = 25 °C are design aids only, not guaranteed and not subject to production testing.

10. REVISION HISTORY

REVISION	DATE	MODIFICATION
A6	–	1. Add initial state of registers 2. Modify description of WDCON.0
A7	–	1. Modify the µC's operating volt in Features and Operating Conditions. 2. Modify the PMR initial data.
A8	May 16, 2003	1. Add Fsys Low-speed-clock switch as High-speed-clock application note.
A9	Mar 1, 2005	1. Modify MOVX instruction machine cycles data.
A10	July 12, 2005	1. Add lead free package part number. 2. Modify EIF to EXIF.

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