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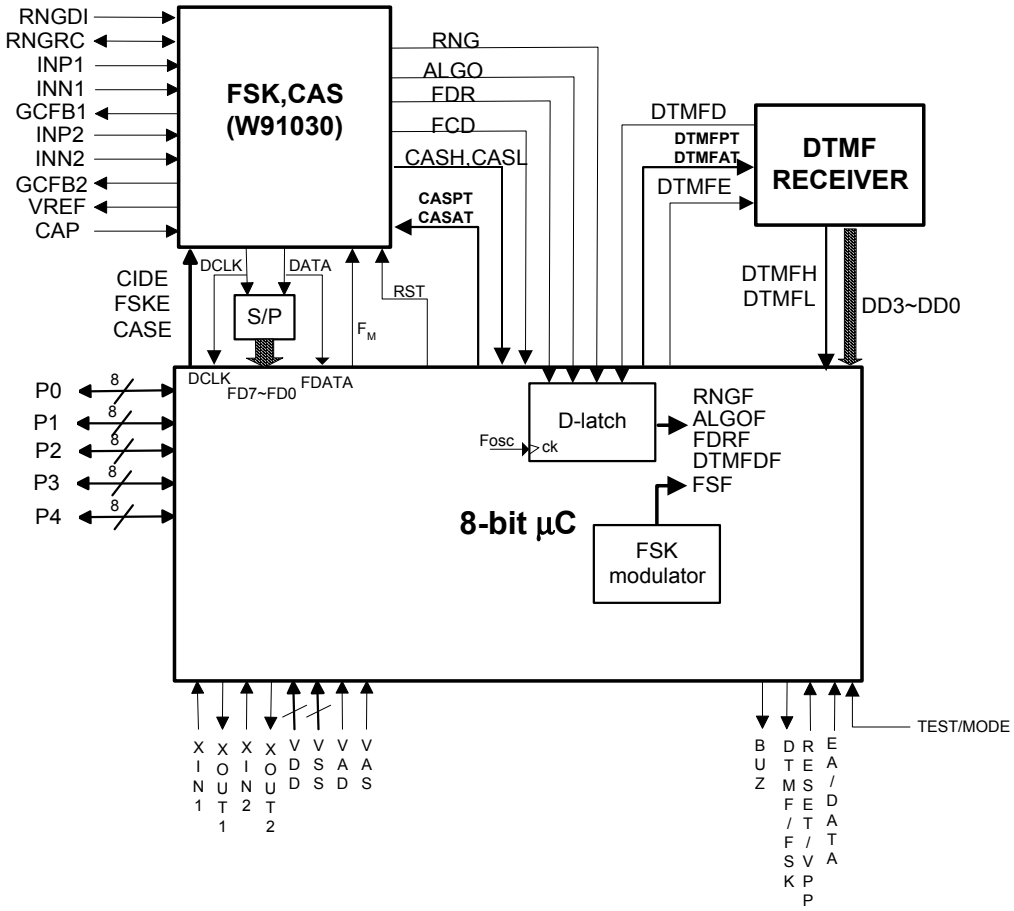
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	3.6MHz
Connectivity	Serial Port
Peripherals	POR, WDT
Number of I/O	40
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w925g240

5. BLOCK DIAGRAM



IE0: Interrupt 0 edge detects: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT0: Interrupt 0 type control. Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

Bit7~4 control timer 1, bit3~0 control timer0

GATE: Gating control. When this bit is set, Timer x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C/$\overline{T}$: Timer or Counter Select. When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.

Note: X is either 0 or 1.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 13-bits timer
0	1	Mode 1: 16-bits timer
1	0	Mode 2: 8-bits with auto-reload from Thx
1	1	Reserved

TIMER 0 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 low byte register.

TIMER 1 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 low byte register.

SERIAL DATA BUFFER (initial = 00H) **Read Only**

Bit:	7	6	5	4	3	2	1	0
	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

Mnemonic: SBUF1 Address: C1h

SBUF1.7-0: Serial data on the serial port 1 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive register, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

REGULATOR VOLTAGE CONTROL REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	REGVC.3	REGVC.2	REGVC.1	REGVC.0

Mnemonic: REGVC Address: C2h

REGVC.3-0: 4 bits to tune the regulator output voltage.

POWER MANAGEMENT REGISTER (initial = XXX00001B)

Bit:	7	6	5	4	3	2	1	0
	XT/$\overline{RG}$	RGMD	RGSL	X2OFF	X1OFF	-	-	-

Mnemonic: PMR Address: C4h

XT/$\overline{RG}$:Crystal/RC Oscillator Select. Setting this bit selects crystal or external clock as system clock source. Clearing this bit selects the on-chip RC oscillator as clock source. X1UP (STATUS.4) must be set to 1 and X1OFF (PMR.3) must be cleared before this bit can be set. Attempts to set this bit without obeying these conditions will be ignored.

RGMD: RC Mode Status. This bit indicates the current clock source of micro-controller. When cleared, CPU is operating from the external crystal or oscillator. When set, CPU is operating from the on-chip RC oscillator.

RGSL: RC Oscillator Select. This bit selects the clock source following a resume from Power Down Mode. Setting this bit allows device operating from RC oscillator when a resume from Power Down Mode. When this bit is cleared, the device will hold operation until the crystal oscillator has warmed-up following a resume from Power Down Mode.

X2OFF: Set to disable sub-oscillator (32KHz oscillator)

X1OFF:Crystal Oscillator Disable. Setting this bit disables the external crystal oscillator. This bit can only be set to 1 while the micro-controller is operating from the RC oscillator. Clearing this bit restarts the crystal oscillator, the X1UP (STATUS.4) bit will be set after crystal oscillator warmed-up has completed.

※Please insert at least 5 instructions NOP after X2UP = ”1”& Fsys = Fs (CKCON1.0 = “1”, M/S).

6.3 Initial State of Registers

The following table lists the initial state of registers after different reset functions.

SFR ITEM	RESET INITIAL VALUE	POR	WDT RESET
ACC, B, STATUS, PSW,	00h	00h	00h
SP,	07h	07h	07h
PAGE	00h	00h	00h
P0, P1, P2, P3, P4, P0IO, P1IO, P2IO, P3IO, P4IO	ffh	ffh	ffh
DPL, DPH, DPL1, DPH1, DPS	00h	00h	00h
PCON, TCON, TMOD,	00h	00h	00h
TL0, TL1, TH0, TH1,	00h	00h	00h
CKCON1, CKCON2, SCON1, SBUF1, REGVC,	00h	00h	00h
EXIF, IE, HB, IP, EIE, EIP	00h	00h	00h
P1SR, P1EF, P1H, P2H, P3H, P4H,	00h	00h	00h
CIDR, CIDFG, CIDPCR, CIDGD, CIDGA,	00h	00h	00h
FSKDR, DTMFDR,	******** B	******** B	******** B
DTMFPT, DTMFAT,	19h	19h	19h
DTMFG, COMPR, IRC1, IRC2, FSKTC, FSKTB,	00h	00h	00h
CASPT, CASAT,	0fh	0fh	0fh
PMR	10000xx1B	10000xx1B	uuu00xx1B
DIVC,	01h	01h	01h
WDCON	0u000uu0B	01000000B	0u0001u0B

Notes:

x: Un-used

u: unchanged

*: Depend on circuit detection

Table 3. Instruction Timing for W925E/C240, continued

INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES	INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES
ADDC A, R2	3A	1	1	ANL C, /bit	B0	2	2
ADDC A, R3	3B	1	1	CJNE A, direct, rel	B5	3	4
ADDC A, R4	3C	1	1	CJNE A, #data, rel	B4	3	4
ADDC A, R5	3D	1	1	CJNE @R0, #data, rel	B6	3	4
ADDC A, R6	3E	1	1	CJNE @R1, #data, rel	B7	3	4
ADDC A, R7	3F	1	1	CJNE R0, #data, rel	B8	3	4
ADDC A, @R0	36	1	1	CJNE R1, #data, rel	B9	3	4
ADDC A, @R1	37	1	1	CJNE R2, #data, rel	BA	3	4
ADDC A, direct	35	2	2	CJNE R3, #data, rel	BB	3	4
ADDC A, #data	34	2	2	CJNE R4, #data, rel	BC	3	4
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	CJNE R5, #data, rel	BD	3	4
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	CJNE R6, #data, rel	BE	3	4
CJNE R7, #data, rel	BF	3	4	JC rel	40	2	3
CLR A	E4	1	1	JNC rel	50	2	3
CPL A	F4	1	1	JB bit, rel	20	3	4
CLR C	C3	1	1	JNB bit, rel	30	3	4
CLR bit	C2	2	2	JBC bit, rel	10	3	4
CPL C	B3	1	1	LCALL addr16	12	3	4
CPL bit	B2	2	2	LJMP addr16	02	3	4
DEC A	14	1	1	MUL AB	A4	1	5
DEC R0	18	1	1	MOV A, R0	E8	1	1
DEC R1	19	1	1	MOV A, R1	E9	1	1
DEC R2	1A	1	1	MOV A, R2	EA	1	1
DEC R3	1B	1	1	MOV A, R3	EB	1	1
DEC R4	1C	1	1	MOV A, R4	EC	1	1
DEC R5	1D	1	1	MOV A, R5	ED	1	1
DEC R6	1E	1	1	MOV A, R6	EE	1	1
DEC R7	1F	1	1	MOV A, R7	EF	1	1
DEC @R0	16	1	1	MOV A, @R0	E6	1	1
DEC @R1	17	1	1	MOV A, @R1	E7	1	1
DEC direct	15	2	2	MOV A, direct	E5	2	2
DEC DPTR	A5	1	2	MOV A, #data	74	2	2
DIV AB	84	1	5	MOV R0, A	F8	1	1
DA A	D4	1	1	MOV R1, A	F9	1	1

Table 3. Instruction Timing for W925E/C240, continued

INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES	INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES
DJNZ R0, rel	D8	2	3	MOV R2, A	FA	1	1
DJNZ R1, rel	D9	2	3	MOV R3, A	FB	1	1
DJNZ R2, rel	DA	2	3	MOV R4, A	FC	1	1
DJNZ R3, rel	DB	2	3	MOV R5, A	FD	1	1
DJNZ R4, rel	DC	2	3	MOV R6, A	FE	1	1
DJNZ R5, rel	DD	2	3	MOV R7, A	FF	1	1
DJNZ R6, rel	DE	2	3	MOV R0, direct	A8	2	2
DJNZ R7, rel	DF	2	3	MOV R1, direct	A9	2	2
DJNZ direct, rel	D5	3	4	MOV R2, direct	AA	2	2
INC A	04	1	1	MOV R3, direct	AB	2	2
INC R0	08	1	1	MOV R4, direct	AC	2	2
INC R1	09	1	1	MOV R5, direct	AD	2	2
INC R2	0A	1	1	MOV R6, direct	AE	2	2
INC R3	0B	1	1	MOV R7, direct	AF	2	2
INC R4	0C	1	1	MOV R0, #data	78	2	2
INC R5	0D	1	1	MOV R1, #data	79	2	2
INC R6	0E	1	1	MOV R2, #data	7A	2	2
INC R7	0F	1	1	MOV R3, #data	7B	2	2
INC @R0	06	1	1	MOV R4, #data	7C	2	2
INC @R1	07	1	1	MOV R5, #data	7D	2	2
INC direct	05	2	2	MOV R6, #data	7E	2	2
INC DPTR	A3	1	2	MOV R7, #data	7F	2	2
JMP @A+DPTR	73	1	2	MOV @R0, A	F6	1	1
JZ rel	60	2	3	MOV @R1, A	F7	1	1
JNZ rel	70	2	3	MOV @R0, direct	A6	2	2
MOV @R1, direct	A7	2	2	RL A	23	1	1
MOV @R0, #data	76	2	2	RLC A	33	1	1
MOV @R1, #data	77	2	2	RR A	03	1	1
MOV direct, A	F5	2	2	RRC A	13	1	1
MOV direct, R0	88	2	2	SETB C	D3	1	1
MOV direct, R1	89	2	2	SETB bit	D2	2	2
MOV direct, R2	8A	2	2	SWAP A	C4	1	1
MOV direct, R3	8B	2	2	SJMP rel	80	2	3
MOV direct, R4	8C	2	2	SUBB A, R0	98	1	1
MOV direct, R5	8D	2	2	SUBB A, R1	99	1	1
MOV direct, R6	8E	2	2	SUBB A, R2	9A	1	1
MOV direct, R7	8F	2	2	SUBB A, R3	9B	1	1
MOV direct, @R0	86	2	2	SUBB A, R4	9C	1	1
MOV direct, @R1	87	2	2	SUBB A, R5	9D	1	1

Table 3. Instruction Timing for W925E/C240, continued

INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES	INSTRUCTION	HEX OP-CODE	BYTES	MACHINE CYCLES
MOV direct, direct	85	3	3	SUBB A, R6	9E	1	1
MOV direct, #data	75	3	3	SUBB A, R7	9F	1	1
MOV DPTR, #data 16	90	3	3	SUBB A, @R0	96	1	1
MOVC A, @A+DPTR	93	1	2	SUBB A, @R1	97	1	1
MOVC A, @A+PC	83	1	2	SUBB A, direct	95	2	2
MOVX A, @R0	E2	1	2	SUBB A, #data	94	2	2
MOVX A, @R1	E3	1	2	XCH A, R0	C8	1	1
MOVX A, @DPTR	E0	1	2	XCH A, R1	C9	1	1
MOVX @R0, A	F2	1	2	XCH A, R2	CA	1	1
MOVX @R1, A	F3	1	2	XCH A, R3	CB	1	1
MOVX @DPTR, A	F0	1	2	XCH A, R4	CC	1	1
MOV C, bit	A2	2	2	XCH A, R5	CD	1	1
MOV bit, C	92	2	2	XCH A, R6	CE	1	1
ORL A, R0	48	1	1	XCH A, R7	CF	1	1
ORL A, R1	49	1	1	XCH A, @R0	C6	1	1
ORL A, R2	4A	1	1	XCH A, @R1	C7	1	1
ORL A, R3	4B	1	1	XCHD A, @R0	D6	1	1
ORL A, R4	4C	1	1	XCHD A, @R1	D7	1	1
ORL A, R5	4D	1	1	XCH A, direct	C5	2	2
ORL A, R6	4E	1	1	XRL A, R0	68	1	1
ORL A, R7	4F	1	1	XRL A, R1	69	1	1
ORL A, @R0	46	1	1	XRL A, R2	6A	1	1
ORL A, @R1	47	1	1	XRL A, R3	6B	1	1
ORL A, direct	45	2	2	XRL A, R4	6C	1	1
ORL A, #data	44	2	2	XRL A, R5	6D	1	1
ORL direct, A	42	2	2	XRL A, R6	6E	1	1
ORL direct, #data	43	3	3	XRL A, R7	6F	1	1
ORL C, bit	72	2	2	XRL A, @R0	66	1	1
ORL C, /bit	A0	2	2	XRL A, @R1	67	1	1
PUSH direct	C0	2	2	XRL A, direct	65	2	2
POP direct	D0	2	2	XRL A, #data	64	2	2
RET	22	1	2	XRL direct, A	62	2	2
RETI	32	1	2	XRL direct, #data	63	3	3

6.5 Power Management

The W925E/C240 has 3 operation mode, normal mode, idle mode and power down mode to manage the power consumption.

Normal Mode

Normal mode is used in the normal operation status. All functions can be worked in the normal mode.

Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer, Divider, Comparator and CID blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically terminate the Idle mode and clear the Idle bit. And if bit IDLT(PCON.4) is cleared the Interrupt Service Routine(ISR) will be executed, else the idle mode is released directly without any execution of ISR. After the ISR, execution of the program will continue from the instruction, which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a low on the external RESET pin or a power on/fail reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset, condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is still running in the period of external reset therefore the instruction is executed immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt, which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset, which will occur after 512 clock periods of the time-out.

Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W925E/C240 will exit the Power Down mode by reset or external interrupts or ring detected. An external reset can be used to exit the Power down state. The low on RESET pin terminates the Power Down mode, and restarts the clock. The on-chip hardware will now provide a delay of 65536 clock, which is used to provide time for the oscillator to restart and stabilize. Once this delay is complete, an internal reset is activated and the program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W925E/C240 can be woken from the Power Down mode by forcing an external interrupt pin activated and ring detected, provided the corresponding interrupt is enabled**,** while the global enable(EA) bit is set. While the power down is released, the device will experience a warm-up delay of 65536 clock cycles to ensure the stabilization of oscillation. Then device executes the interrupt service routine for the corresponding external interrupt or CID interrupt. After the interrupt service routine is completed, the program returns to the instruction after the one, which put the device into Power Down

mode and continues from there. When RGSL (PMR.5) bit is set to 1, the CPU will use the internal RC oscillator instead of crystal to exit Power Down mode. The micro-controller will automatically switch from RC oscillator to crystal after a warm-up delay of 65536 crystal clocks. The RC oscillator runs at approximately 2–4 MHz. Using RC oscillator to exit from Power Down mode saves the time for waiting crystal start-up. It is useful in the low power system which usually be awakened from a short operation then returns to Power Down mode.

6.6 Reset

The user has several hardware related options for placing the W925E/C240 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are few flags that initial states are dependant on the source of reset. User can recognize the cause of reset by reading the flags. There are three ways of putting the device into reset state. They are External reset, Power on reset and Watchdog reset.

External Reset

The device continuously samples the RESET pin at state C4 of every machine cycle. Therefore, the RESET pin must be held for at least 2 machine cycles to ensure detection of a valid RESET low. The reset circuitry then synchronously applies the internal reset signal. Thus, the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RESET is 0. Even after RESET is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However, since some flags indicate the cause of other two reset, the external reset can be considered as the default reset if those two flags are cleared.

Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can reset the watchdog timer at any time to avoid producing the flag WDIF. If the Watchdog reset is enabled and the flag WDIF is set high, the watchdog timer reset is performed after the additional 512 clocks come. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed, the device will begin execution from 0000h.

6.7 Interrupt

The W925E/C240 has a two priority levels interrupt structure with 11 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags, which are checked to generate the interrupt. In the edge triggered mode of the $\overline{INT0}$ and the $\overline{INT1}$ inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low until the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the

service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts INT2 to INT3 are edge triggered only.

The TF0, TF1 flags generate the Timer 0, 1 Interrupts. These flags are set by the overflow in the Timer 0, Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the enable bit EIE.5 enables the interrupt, then an interrupt will occur.

The Serial block can generate interrupts on reception or transmission. There are one interrupt sources from the Serial block, which are obtained by SF1 in the SCON1. SF1 is cleared automatically when the serial port interrupt is serviced.

The divider interrupt is generated by DIVF that is set when divider overflows. DIVF is set by hardware and cleared when divider interrupt is serviced. The divider interrupt is enable/disable if the bit EDIV is high/low.

The comparator interrupt is produced by COMPF, which is set when the RESC bit is changed from low to high. RESC, which is the real-time result of comparator, set when the voltage of reference input is higher than the voltage of analog input.

The CID interrupt is generated by CIDF. The CIDF is a logic OR output of all CID flags which are set by hardware and cleared by software. The structure of the CID flags is shown in Figure 6-4.

Each of the individual interrupts can be enabled or disabled by setting or clearing the corresponding bits in the IE and EIE SFR. A bit EA, which is located in IE.7, is a global control bit to enable/disable the all interrupt. When bit EA is zero all interrupts are disabling and when bit EA is high, each interrupt is enable individually by the corresponding bit.

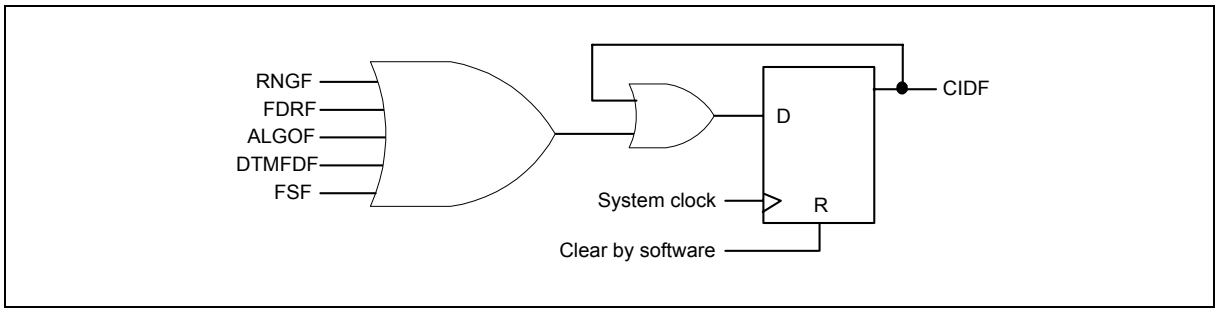


Figure 6-4 The Structure of CID Flags

Priority Level Structure

There are two priority levels for the interrupts, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Table 4 Interrupt table.

INTERRUPT	FLAG NAME	FLAG LOCATION	EN BIT	EN BIT LOCATION	PRIORITY	FLAG CLEARED BY	INTERRUPT VECTOR
External interrupt 0	IE0	TCON.1	EX0	IE.0	1 (higest)	hardware + software	03h
Timer0 overflow	TF0	TCON.5	ET0	IE.1	2	hardware + software	0Bh
External interrupt 1	IE1	TCON.3	EX1	IE.2	3	hardware + software	13h
Timer1 overflow	TF1	TCON.7	ET1	IE.3	4	hardware + software	1Bh
Serial port	SF1	SCON1.7	ES1	IE.6	5	hardware + software	3Bh
External interrupt 2	*IE2*	EXIF.0	EX2	EIE.0	6	hardware + software	43h
External interrupt 3	*IE3*	EXIF.1	EX3	EIE.1	7	hardware + software	4Bh
CID	*CIDF*	EXIF.2	ECID	EIE.2	8	software	53h
Divider overflow	*DIVF*	EXIF.3	EDIV	EIE.3	9	hardware + software	5Bh
Compare difference	*COMPF*	EXIF.4	ECOMP	EIE.4	10	hardware + software	63h
Watchdog timer	*WDIF*	WDCON.3	EWDI	EIE.5	11 (lowest)	software	6Bh

Ps: The flags marked as the italic font are not bit-addressable.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are

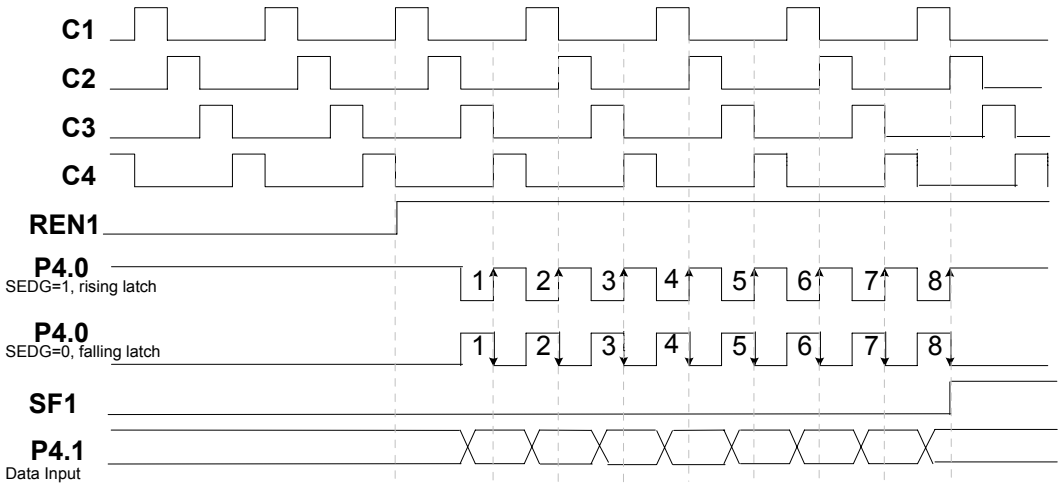
1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being executed.

3. The current instruction does not involve a write to IP, IE, EIP or EIE registers and is not a RETI.

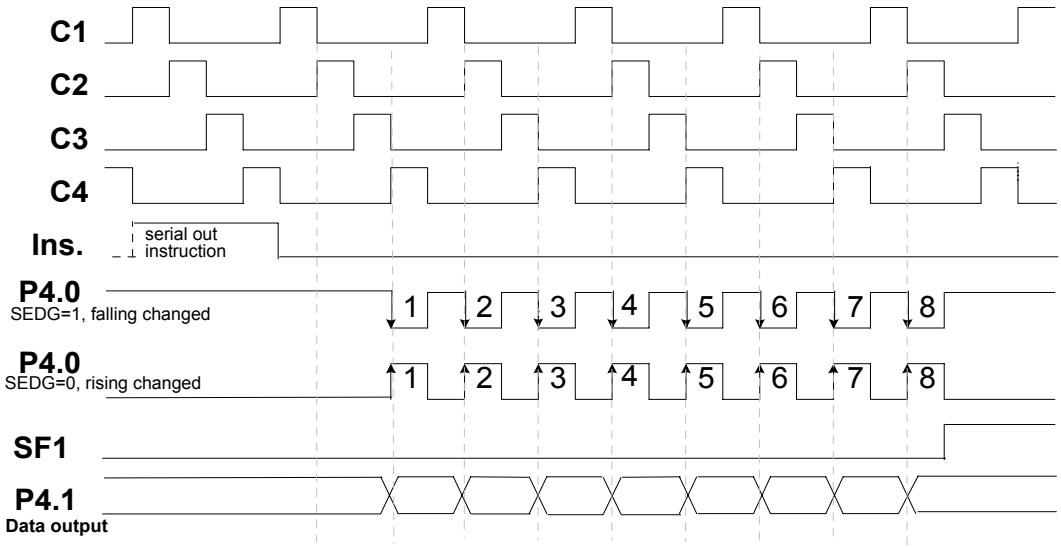
If any of these conditions is not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts being sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered. Note that every polling cycle is new.

Execution continues from the vectored address until an RETI instruction is executed. On execution of the RETI instruction, the processor pops out the top content of Stack to the PC. The processor is not notified anything if the content of stack was changed. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.



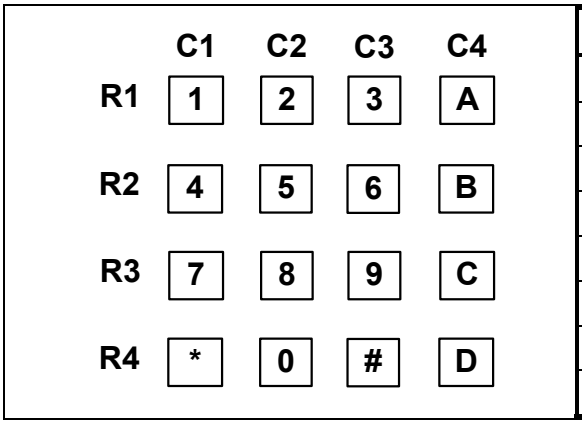
NOTE: The serial clock frequency is fosc/2

Figure 6-8 Timing of the Serial Port 1 Input Function



NOTE: The serial clock frequency is fosc/2

Figure 6-9 Timing of the Serial Port 1 Output Function



Row/Col	Frequency
R1	697 Hz
R2	770 Hz
R3	852 Hz
R4	941 Hz
C1	1209 Hz
C2	1336 Hz
C3	1477 Hz
C4	1633 Hz

Figure 6-11 The Relation Between DTMF and Keypad

Bit: 7 6 5 4 3 2 1 0

-	DTGE	HE	LE	L1	L0	H1	H0

Mnemonic: DTMFG Address: BAh

L1	L0	H1	H0	SELECTED TONE
x	x	0	0	1209Hz
x	x	0	1	1336Hz
x	x	1	0	1477Hz
x	x	1	1	1633Hz
0	0	x	x	697Hz
0	1	x	x	770Hz
1	0	x	x	852Hz
1	1	x	x	941Hz

LE: Enable low group frequency output.

HE: Enable high group frequency output.

DTGE: Enable dual tone output to DTMF pin.

6.12 FSK Generator

W925E/C240 provides a FSK generator, which outputs the FSK signal to the DTMF pin. The FSK output share with DTMF output pin. It can out FSK signal with 1200Hz baud rate of ITU-T V.23 or Bellcore 202 signal. A FSK transmit data register (FSKTB) specifies the desired output data. The FSK Transmit Control Register (FSKTC) can control whether the FSK signal will be output or not. The relation timing is shown in Figure 6-12

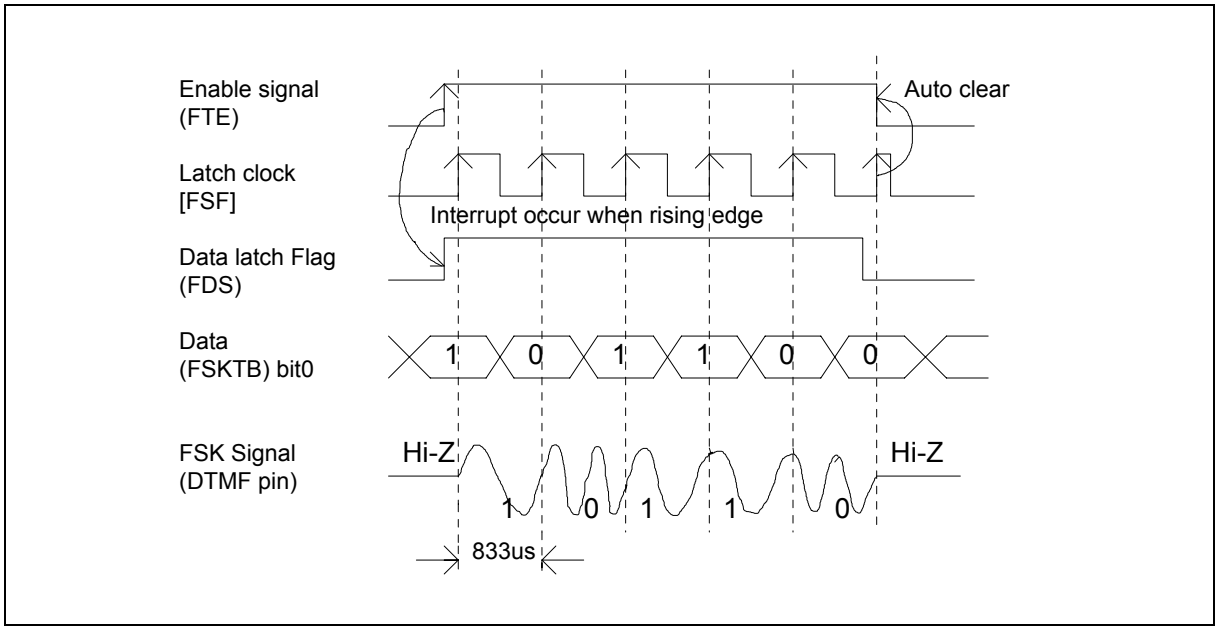


Figure 6-12 FSK Modulator

FSK TRANSIMT CONTROL REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	FTE	FTM	FDS	-	-	-	LO1	LO0

Mnemonic: FSKTC Address: C6h

FTE: FSK transmit Enable. Enable = 1, Disable = 0

FTM: FSK signal Standard. Bellcore 202 = 1, V.23 = 0

FDS: FSK data sending status

LO0, LO1: FSK transmit level option

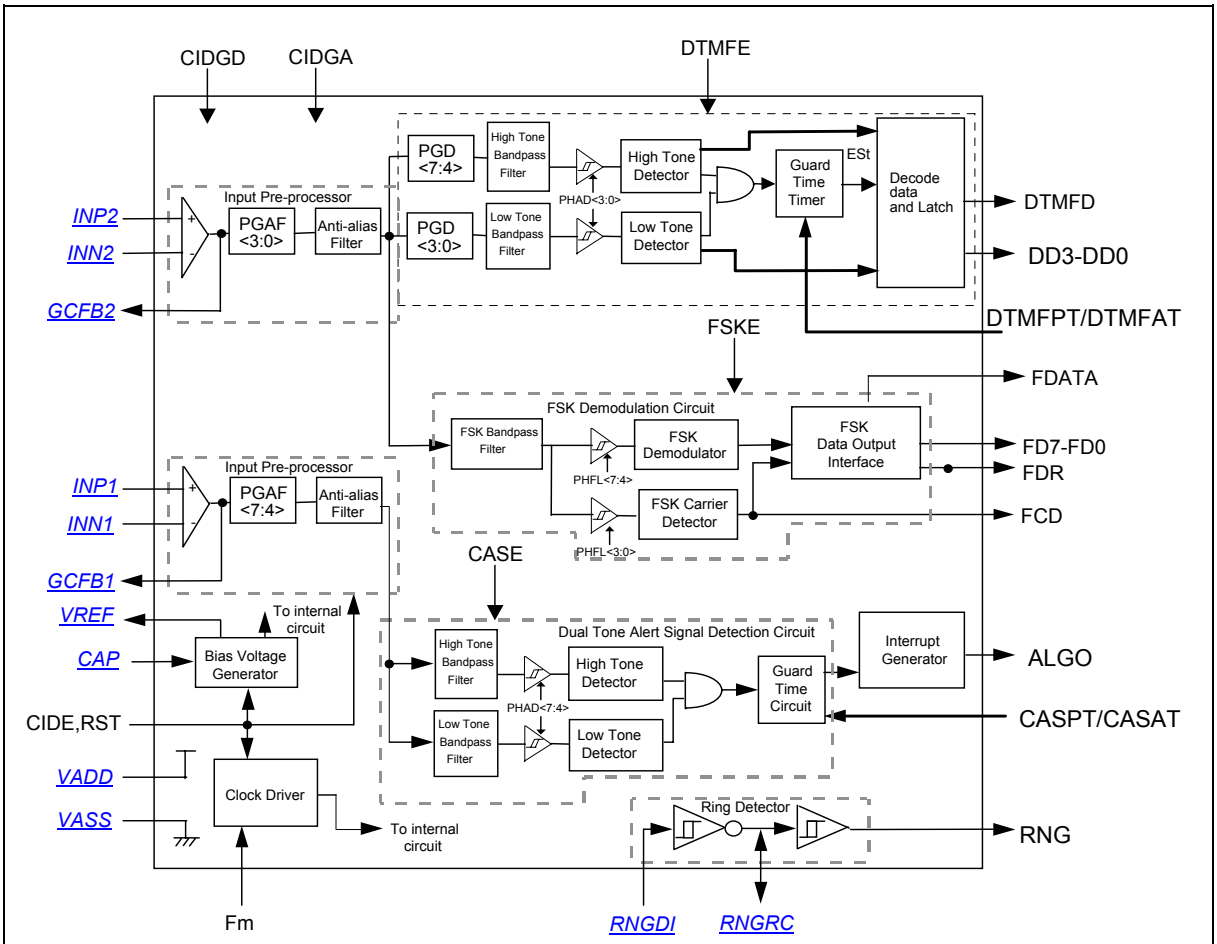
FSK output level	LO1	LO0
150mV	0	0
120mV	0	1
95mV	1	0
75mV	1	1

FSK TRANSMIT DATA BUFFER (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	FSKTB.7	FSKTB.6	FSKTB.5	FSKTB.4	FSKTB.3	FSKTB.2	FSKTB.1	FSKTB.0

Mnemonic: FSKTB Address: C7h

FSKTB.0:Only this bit will be latched and send out as FSK signal



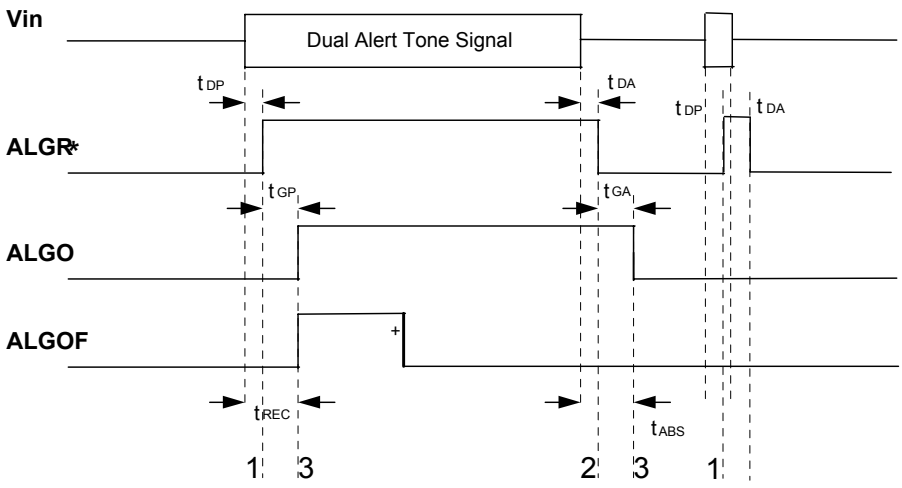
PS: The signals noted in italic and underline type are CID pins on the chip.

Figure 6-14 The CID Block Diagram

CAS/DTAS Detection

In off-hook services (type II), the detection of CAS/DTAS will affect the quality of the call waiting service. When the CAS/DTAS is sent from far end, sometimes the near end user maybe still talking. The CPE must be able to detect the CAS/DTAS successfully in the presence of near end speech. To detect CAS/DTAS from telephone hybrid receiver pair improves the detection. However, in BT's on-hook CID system the CAS/DTAS detection is from Tip/Ring pair.

The dual tone alert signal is separated into high and low tones and detected by a high/low tone detector. When the alert tone is recognized by the detector, the bit ALGO will go high and the rising signal will set the bit ALGOF in CIDFG to produce the CID flag(CIDF). Figure 6-18 shows the guard time waveform of detecting alert tone. The total recognition time is $t_{REC}=t_{DP}+t_{GP}$, where t_{DP} is the tone present detect time and t_{GP} is the tone present guard time. The total absent guard time is $t_{ABS}=t_{DA}+t_{GA}$ where t_{DA} is the tone absent detect time and t_{GA} is the tone absent guard time. The tone present/absent guard time is determined by guard-time timer, which the input clock period is 0.858mS. When the alert tone is detected, the internal signal ALGR will be set and the rising edge of ALGR resets the guard-time timer and the timer starts up counting from 00H. As the content of the timer is the same as the register CASPT, the timer stops counting and the bit ALGO will be set and the rising edge of ALGO triggers the flag ALGOF to become high. The counting of tone absent time is similar to the counting of tone present time but the falling edge of ALGR/ ALGO replaces the rising edge and the CASAT replaces the CASPT. The bit ALGO is controlled by hardware only. The flag ALGOF is set by rising edge of ALGO and cleared by software.



1: Guard time timer is reset and starts to up count from 00H.
2: Guard time timer is reset and starts to up count from 00H.
3: The content of the guard-time timer reaches the content of ASPT/ASAT.

*ALGR is an internal signal in the uC.
+ Clear by software.

Figure 6-18 Guard Time Waveform of Alert Tone Signal Detection

FSK Decoder

The FSK carrier detector provides an indication of the present of a signal within the FSK frequency band. If the output amplitude of the FSK band-pass filter is sufficient to be detected continuously for 8 mS, the FSK carrier detected bit FCD will go high and it will be released if the FSK band-pass filter output amplitude is not able to be detected for greater than 8 mS. The 8 mS is the hysteresis of the FSK carrier detector. Figure 6-20 shows the timing of FSK carrier detection.

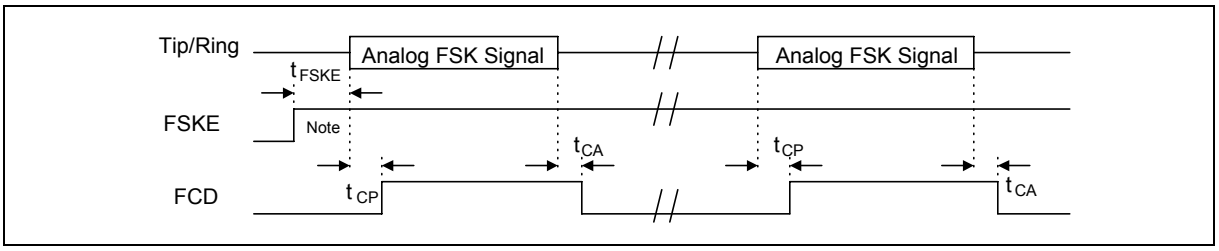


Figure 6-20 FSK Detection Enable and FSK Carrier Present and Absent Timing

The FSK demodulation function can demodulate Bell 202 and ITU-T V.23 Frequency Shift keying (FSK) with 1200-baud rate. When the decoder receives the FSK serial data, the serial data will be demodulated into bit FDATA with 1200-baud rate in the mean time the synchronous clock signal is output to the bit FCLK. As the decoder receives one byte, the internal serial-to-parallel circuit sets the bit FDR and converts the 8-bit serial data into the byte register FSKDR. The rising edge of bit FDR will set the flag FDRF to produce CID interrupt but FDRF is cleared by software. User can get the FSK data by reading register FSKDR or sampling the bit FDATA. The timing of FSK demodulation is shown in Figure 6-21.

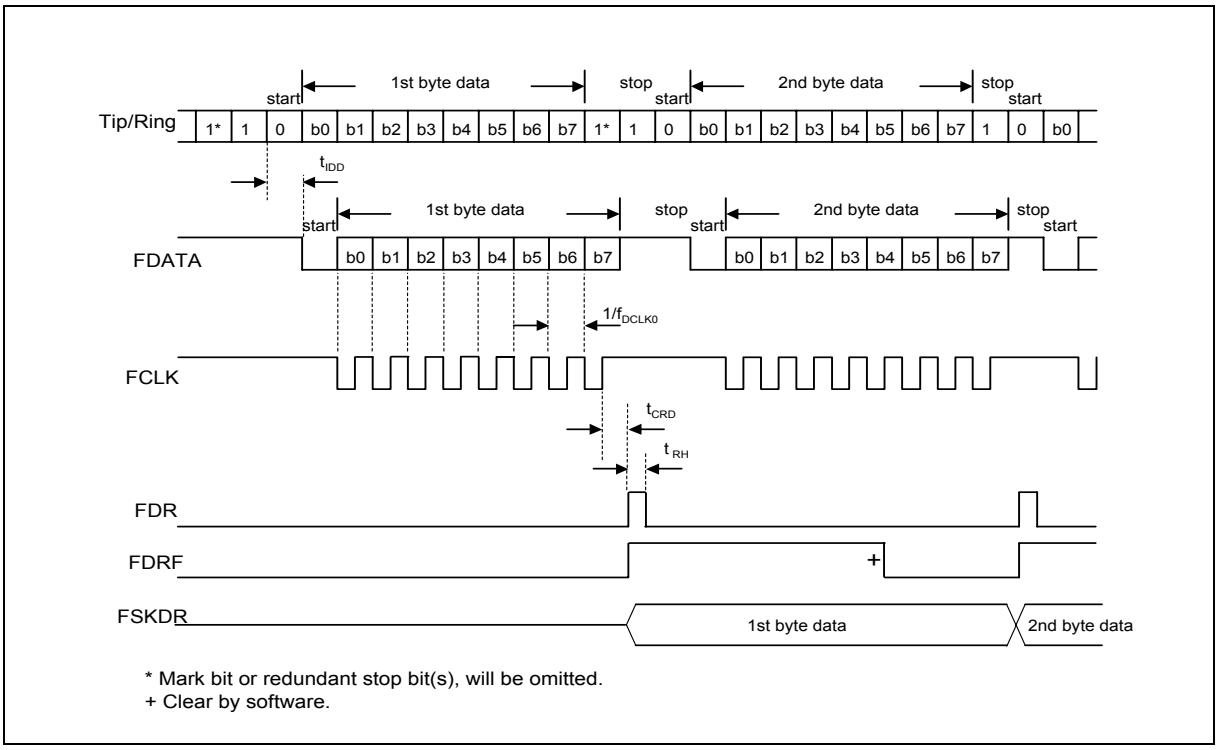


Figure 6-21 Serial Data Interface Timing of FSK Demodulation

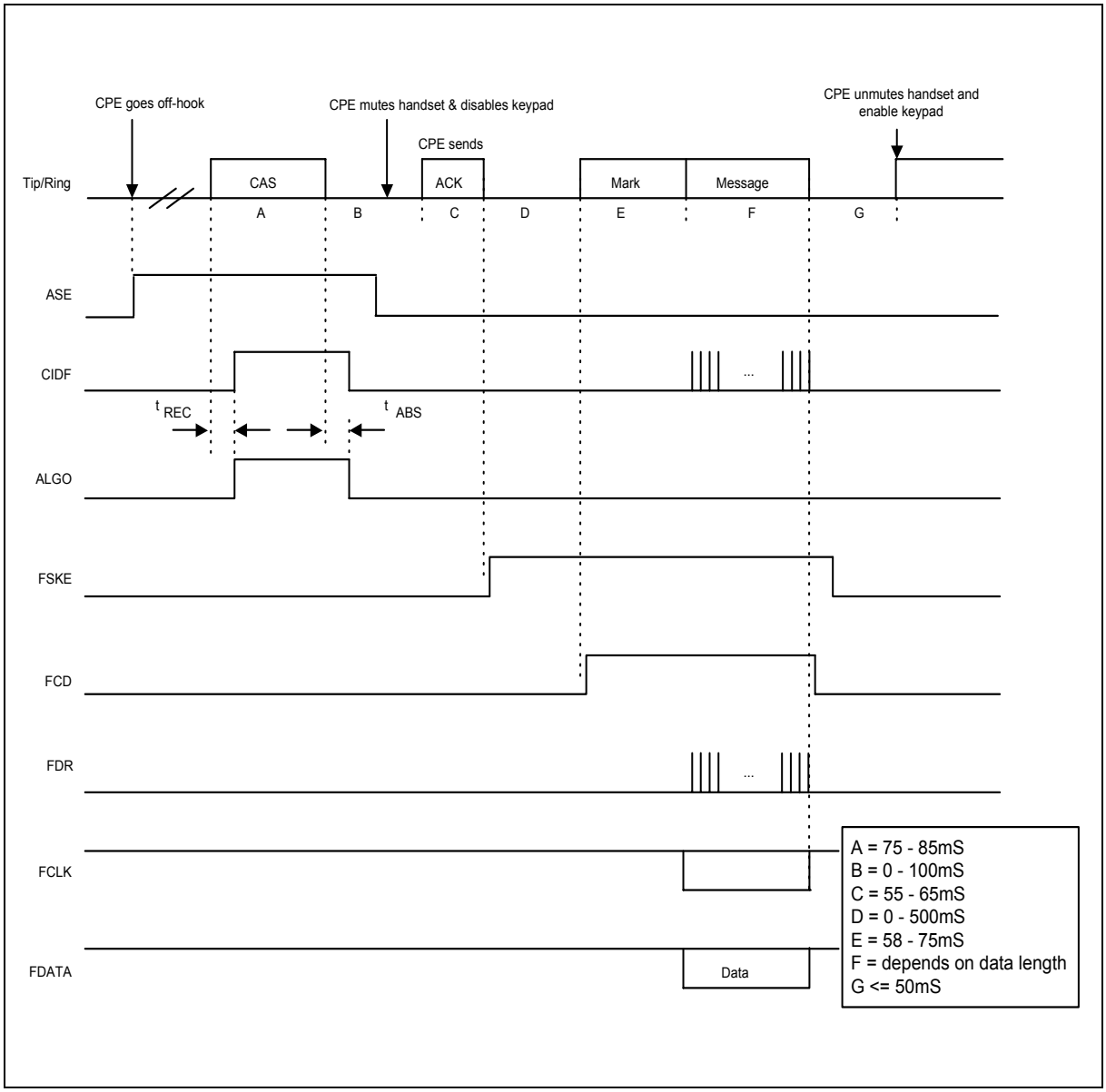


Figure 7-3 Input and Output Timing of Bellcore Off-hook Data Transmission

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings*

(Voltage referenced to V_{SS} pin)

PARAMETER	SYMBOL	RATING	UNITS
Supply Voltage with respect to V_{SS}	V_{DD}	-0.3 to 6	V
Voltage on any pin other than supplies (note 1)		-0.7 to V_{DD} + 0.7	V
Current at any pin other than supplies		0 to 10	MA
Storage Temperature	Tst	-65 to 150	°C

Note:

*. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the lift and reliability of the device.

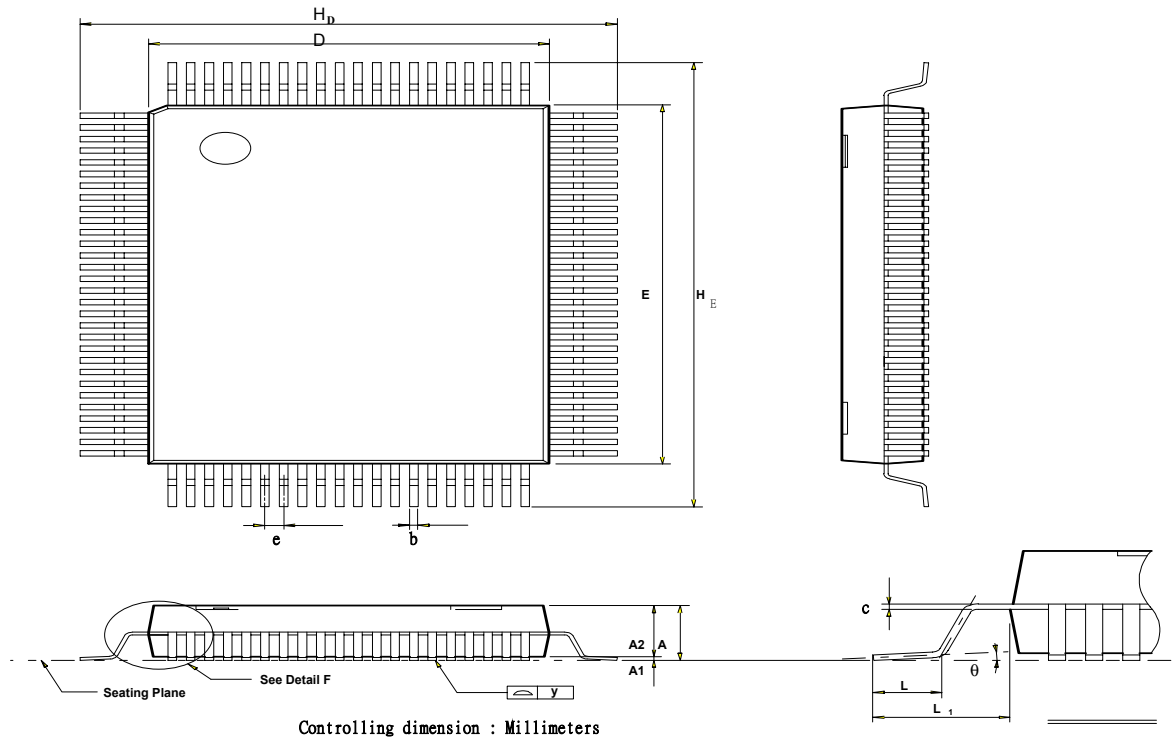
1. V_{DD} +0.7 should not excess maximum rating of supply voltage.

8.2 Recommended Operating Conditions

CHARACTERISTICS	SYMBOL	RATING	UNIT
Power Supplies (Analog)	V_{AD}	3.0 to 6.0	V
Power Supplies (Digital) EEPROM(E) type(Depend on option) MASK(C) type	V_{DD}	2.4 to 3.6 or 3.0 to 5.5 2.2 to 6.0	V
Main Clock Frequency	f_{OSC}	3.579545	MHz
Sub Clock Frequency	f_{SUB}	32768	Hz
Tolerance on Clock Frequency	Δf_C	-0.1 to +0.1	%
Operation Temperature	T_{op}	0 to 75	°C

9. PACKAGE DIMENSION

100L QFP (14 x 20 x 2.75mm footprint 4.8mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A 1	0.010	0.014	0.018	0.25	0.35	0.45
A 2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H D	0.746	0.740	0.756	18.40	18.80	19.20
H E	0.960	0.976	0.992	24.40	24.80	25.20
L	0.039	0.047	0.055	1.00	1.20	1.40
L 1	—	0.064	—	—	2.40	—
y	—	—	0.003	—	—	0.08
θ	0 °	—	7 °	0 °	—	7 °