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Organization

The μPD789167, 789177, 789167Y, 789177Y Subseries manual is divided into two parts: this manual and the instruction manual (common to the 78K/0S Series).

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual (This manual)	78K/0S Series Instruction User's Manual
• Pin functions • Internal block functions • Interrupts • Other internal peripheral functions • Electrical specifications	• CPU function • Instruction set • Instruction description

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electric engineering, logic circuits, and microcontrollers.

◊ For users who use this document as the manual for the μPD789166(A), 789167(A), 789176(A), 789177(A), 789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A), 789166(A1), 789167(A1), 789176(A1), 789177(A1), 789166(A2), 789167(A2), 789176(A2), 789177(A2), 78F9177A(A), 78F9177AY(A), and 78F9177A(A1)

→ The only differences between standard products and (A) products, (A1) products, and (A2) products are quality grades, power supply voltage, operating ambient temperature, minimum instruction execution time, and electrical specifications. (Refer to 1.10 Differences Between Standard Quality Grade Products and (A) Products, (A1) Products, and (A2) Products, and 2.10 Differences Between Standard Quality Grade Products and (A) Products.) For (A) products, (A1) products, and (A2) products, read the part numbers indicated in Chapters 3 to 22 in the following manner.

μPD789166 → μPD789166(A), 789166(A1), 789166(A2)
μPD789167 → μPD789167(A), 789167(A1), 789167(A2)
μPD789176 → μPD789176(A), 789176(A1), 789176(A2)
μPD789177 → μPD789177(A), 789177(A1), 789177(A2)
μPD789166Y → μPD789166Y(A)
μPD789167Y → μPD789167Y(A)
μPD789176Y → μPD789176Y(A)
μPD789177Y → μPD789177Y(A)
μPD78F9177A → μPD789177A(A), 78F9177A(A1)
μPD78F9177AY → μPD78F9177AY(A)

◊ To understand the overall functions of the μPD789167, 789177, 789167Y, and 789177Y Subseries

→ Read this manual in the order of the **CONTENTS**.

◊ How to read register formats

→ The name of a bit whose number is enclosed with < > is reserved in the assembler and is defined as an sfr variable by the #pragma sfr directive in the C compiler.

◊ To learn the detailed functions of a register whose register name is known

→ See **APPENDIX C REGISTER INDEX**.

4.2 Description of Pin Functions

4.2.1 P00 to P05 (Port 0)

These pins constitute a 6-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 0 (PM0). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

4.2.2 P10, P11 (Port 1)

These pins constitute a 2-bit I/O port and can be set to input or output port mode in 1-bit units by using port mode register 1 (PM1). When these pins are used as an input port, an on-chip pull-up resistor can be used by setting pull-up resistor option register 0 (PU0).

4.2.3 P20 to P26 (Port 2)

These pins constitute a 7-bit I/O port. In addition, these pins provide a function to perform I/O to/from the timer and to I/O the data and clock of the serial interface.

Port 2 can be set to the following operation modes in 1-bit units.

(1) Port mode

In port mode, P20 to P26 function as a 7-bit I/O port. Port 2 can be set to input or output mode in 1-bit units by using port mode register 2 (PM2). For P20 to P22, P25, and P26, whether to use on-chip pull-up resistors can be specified in 1-bit units by using pull-up resistor option register B2 (PUB2), regardless of the setting of port mode register 2 (PM2). P23 and P24 are N-ch open-drain I/O ports.

(2) Control mode

In this mode, P20 to P26 function as the timer I/O, the data I/O and the clock I/O of the serial interface.

(a) TI80

This is the external clock input pin for 8-bit timer/event counter 80.

(b) TO80

This is the timer output pin of 8-bit timer/event counter 80.

(c) SI20, SO20

These are the serial data I/O pins of the serial interface.

(d) $\overline{\text{SCK20}}$

This is the serial clock I/O pin of the serial interface.

(e) $\overline{\text{SS20}}$

This is the chip select input pin of the serial interface.

(f) RxD20, TxD20

These are the serial data I/O pins of the asynchronous serial interface.

4.2.6 P60 to P67 (Port 6)

These pins constitute an 8-bit input-only port. They can function as A/D converter input pins as well as a general-purpose input port.

(1) Port mode

In port mode, P60 to P67 function as an 8-bit input-only port.

(2) Control mode

In control mode, P60 to P67 function as A/D converter analog inputs (ANI0 to ANI7).

4.2.7 $\overline{\text{RESET}}$

A low-level active system reset signal is input to this pin.

4.2.8 X1, X2

These pins are used to connect a crystal resonator for main system clock oscillation.

To supply an external clock, input the clock to X1 and input the inverted signal to X2.

4.2.9 XT1, XT2

These pins are used to connect a crystal resonator for subsystem clock oscillation.

To supply an external clock, input the clock to XT1 and input the inverted signal to XT2.

4.2.10 AV_{DD}

Analog power supply pin of the A/D converter. Always use the same potential as that of the V_{DD0} pin even when the A/D converter is not used.

4.2.11 AV_{SS}

This is a ground potential pin of the A/D converter. Always use the same potential as that of the V_{SS0} pin even when the A/D converter is not used.

4.2.12 AV_{REF}

This is the A/D converter reference voltage input pin. When the A/D converter is not used, connect this pin to V_{DD0} or V_{SS0}.

4.2.13 V_{DD0}, V_{DD1}

V_{DD0} is a positive power supply pin for ports.

V_{DD1} is a positive power supply pin for other than ports.

4.2.14 V_{SS0}, V_{SS1}

V_{SS0} is a ground potential pin for ports.

V_{SS1} is a ground potential pin for other than ports.

4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 4-1.
For the I/O circuit configuration of each type, refer to **Figure 4-1**.

Table 4-1. Types of I/O Circuits for Each Pin and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/SCL0	13-X		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24/SDA0			
P25/TI80/$\overline{SS20}$	8-C		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
P30/INTP0/TI81/CPT90			Input: Independently connect to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P31/INTP1/TO81			
P32/INTP2/TO90			
P33/INTP3/TO82/BZO90			
P50 to P53 (mask ROM version)	13-U		Input: Connect to V_{SS0} or V_{SS1}. Output: Leave open.
P50 to P53 (flash memory version)	13-T		
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
XT1	–	Input	Connect directly to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC0 (mask ROM version)	–	–	Connect directly to V_{SS0} or V_{SS1}.
IC2			Leave open.
V_{PP} (flash memory version)			Independently connect via a 10 kΩ pull-down resistor, or connect directly to V_{SS0} or V_{SS1}.

Figure 5-2. Memory Map (μPD789167, μPD789177, μPD789167Y, and μPD789177Y)

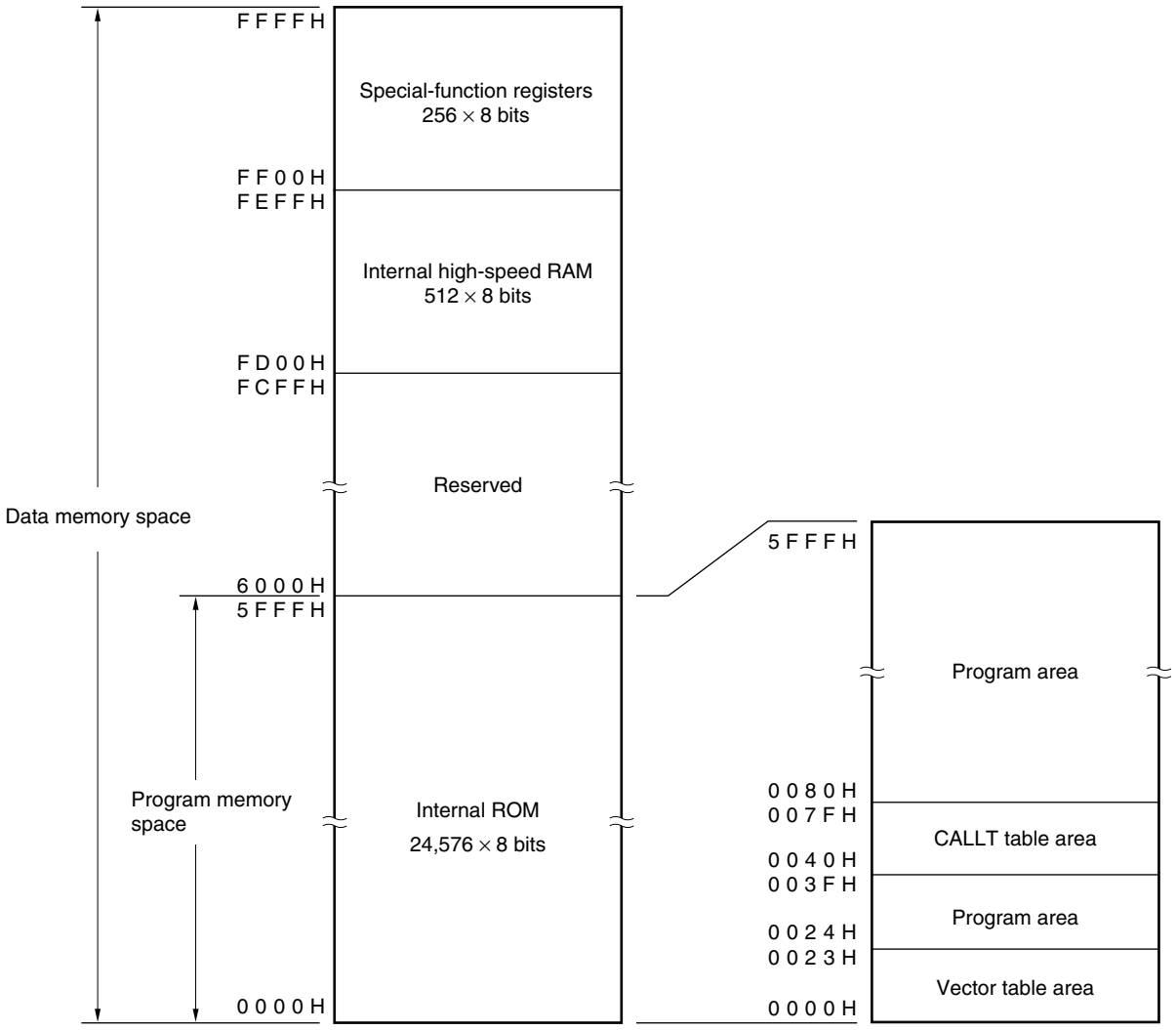


Table 5-3. Special-Function Registers (1/2)

Address	Special-Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1			√	√	–	
FF02H	Port 2	P2			√	√	–	
FF03H	Port 3	P3			√	√	–	
FF05H	Port 5	P5			√	√	–	
FF06H	Port 6	P6		R	√	√	–	
FF10H	16-bit multiplication result storage register 0	MUL0L	MUL0		–	–	√ Notes 2, 3	Undefined
FF11H		MUL0H						
FF14H	A/D conversion result register 0	ADCR0			–	√ Note 1	√ Note 2	
FF15H								
FF16H	16-bit compare register 90	CR90L	CR90	W	–	–	√ Notes 2, 3	FFFFH
FF17H		CR90H						
FF18H	16-bit timer counter 90	TM90L	TM90	R	–	–	√ Notes 2, 3	0000H
FF19H		TM90H						
FF1AH	16-bit capture register 90	TCP90L	TCP90		–	–	√ Notes 2, 3	Undefined
FF1BH		TCP90H						
FF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1			√	√	–	
FF22H	Port mode register 2	PM2			√	√	–	
FF23H	Port mode register 3	PM3			√	√	–	
FF25H	Port mode register 5	PM5			√	√	–	
FF32H	Pull-up resistor option register B2	PUB2			√	√	–	00H
FF33H	Pull-up resistor option register B3	PUB3			√	√	–	
FF42H	Timer clock selection register 2	TCL2			–	√	–	
FF48H	16-bit timer mode control register 90	TMC90			√	√	–	
FF49H	Buzzer output control register 90	BZC90			√	√	–	
FF4AH	Watch timer mode control register	WTM			√	√	–	
FF50H	8-bit compare register 80	CR80		W	–	√	–	Undefined
FF51H	8-bit timer counter 80	TM80		R	–	√	–	00H
FF53H	8-bit timer mode control register 80	TMC80		R/W	√	√	–	

Notes 1. When using this register with an 8-bit A/D converter (μPD789167 or 789167Y Subseries), the register can be accessed in 8-bit units. At this time, the address is FF15H.
When using this register with a 10-bit A/D converter (μPD789177 or 789177Y Subseries), the register can be accessed only in 16-bit units. When the μPD78F9177 or μPD78F9177A, the flash memory counterpart of the μPD789166 or μPD789167, is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166 or μPD789167 can be used. The same is also true for the μPD78F9177Y or μPD78F9177AY, the flash memory counterpart of the μPD789166Y or μPD789167Y. When the μPD78F9177Y or μPD78F9177AY is used, the register can be accessed in 8-bit units. However, only an object file assembled with the μPD789166Y and μPD789167Y can be used.

2. 16-bit access is allowed only with short direct addressing.

3. MUL0, CR90, TM90, and TCP90 are designed only for 16-bit access. With direct addressing, however, they can also be accessed in 8-bit mode.

5.4.5 Register indirect addressing

[Function]

The memory is addressed with the contents of the register pair specified as an operand. The register pair to be accessed is specified with the register pair specify code in the instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

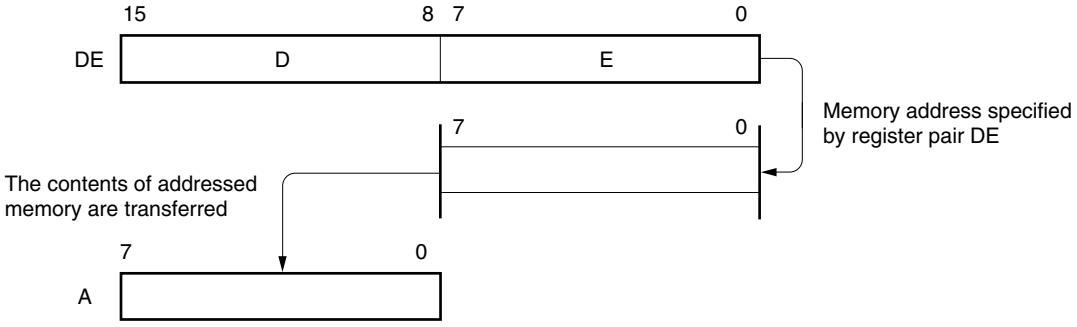
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; When selecting register pair [DE]

Instruction code	0	0	1	0	1	0	1	1

[Illustration]



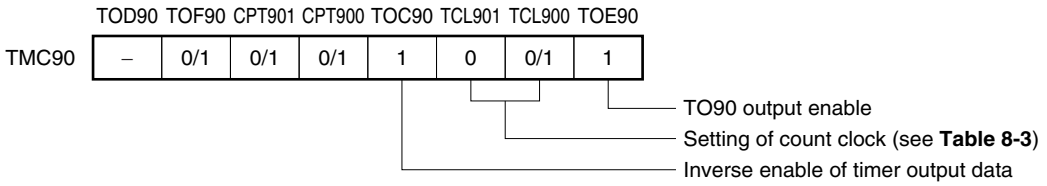
8.4.2 Operation as timer output

16-bit timer 90 can invert the timer output repeatedly each time the free-running counter value reaches the value set to CR90. Since this counter is not cleared and holds the count even after the timer output is inverted, the interval time is equal to one cycle of the count clock set in TCL901 and TCL900.

To operate the 16-bit timer as a timer output, the following settings are required.

- Set P32 to output mode (PM32 = 0).
- Reset the output latch of P32 to 0.
- Set the count value in CR90.
- Set 16-bit timer mode control register 90 (TMC90) as shown in Figure 8-7.

Figure 8-7. Settings of 16-Bit Timer Mode Control Register 90 for Timer Output Operation

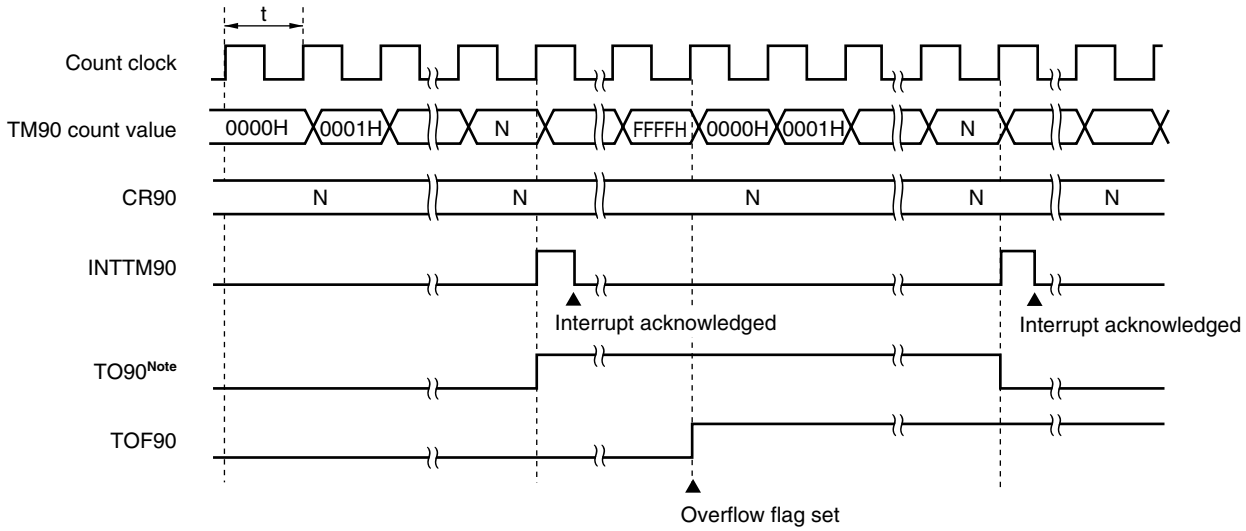


Caution If both the CPT901 flag and CPT900 flag are set to 0, the capture edge is disabled.

When the count value of 16-bit timer counter 90 (TM90) matches the value set in CR90, the output status of the TO90/P32/INTP2 pin is inverted. This enables timer output. At that time, the TM90 count is continued and an interrupt request signal (INTTM90) is generated.

Figure 8-8 shows the timing of timer output (see **Table 8-3** for the interval time of the 16-bit timer).

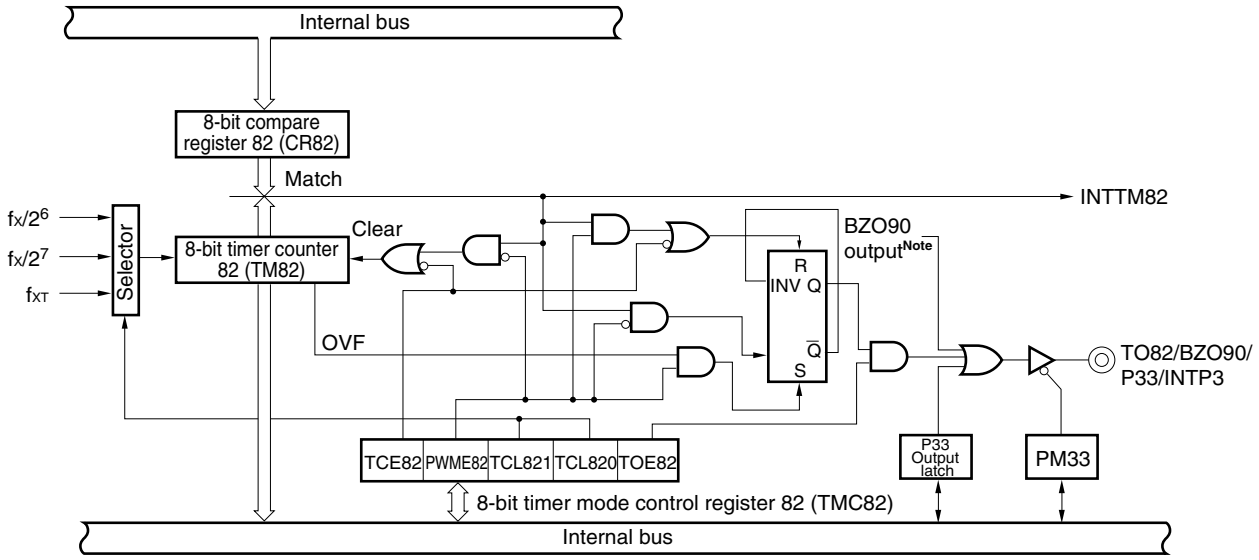
Figure 8-8. Timer Output Timing



Note The TO90 initial value becomes low level during output enable (TOE90 = 1).

Remark N = 0000H to FFFFH

Figure 9-3. Block Diagram of 8-Bit Timer 82



Note See **Figure 8-1 Block Diagram of 16-Bit Time 90**.

(1) 8-bit compare register 8n (CR8n)

A value specified in CR8n is compared with the count in 8-bit timer counter 8n (TM8n). If they match, an interrupt request (INTTM8n) is issued.

CR8n is set with an 8-bit memory manipulation instruction. Any value from 00H to FFH can be set.

$\overline{\text{RESET}}$ input makes CR8n undefined.

Cautions 1. Before rewriting CR8n, stop the timer operation once. If CR8n is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. Do not clear CR8n to 00H in PWM output mode (when PWME8n = 1: bit 6 of 8-bit timer mode control register 8n (TMC8n)); otherwise, PWM output may not be produced normally.

Remark n = 0 to 2

(2) 8-bit timer counter 8n (TM8n)

TM8n is used to count the number of pulses.

Its contents are read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TM8n to 00H.

Remark n = 0 to 2

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stop
1	Transmit operation enable

RXE20	Receive operation control
0	Receive operation stop
1	Receive operation enable

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length specification
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be set to 0.

2. Switch operating modes after halting the serial transmit/receive operation.

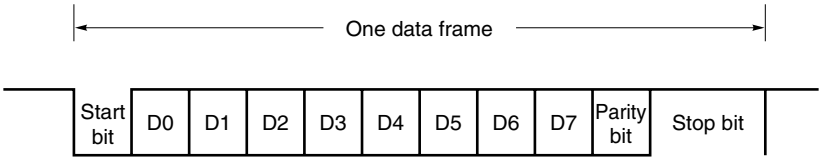
(2) Communication operation

(a) Data format

The transmit/receive data format is as shown in Figure 14-7. One data frame consists of a start bit, character bits, parity bit, and stop bit(s).

The specification of character bit length in one data frame, parity selection, and specification of stop bit length is carried out with asynchronous serial interface mode register 20 (ASIM20).

Figure 14-7. Asynchronous Serial Interface Transmit/Receive Data Format



- Start bits ..... 1 bit
- Character bits..... 7 bits/8 bits
- Parity bits ..... Even parity/odd parity/0 parity/no parity
- Stop bit(s) ..... 1 bit/2 bits

When 7 bits are selected as the number of character bits, only the lower 7 bits (bits 0 to 6) are valid; in transmission the most significant bit (bit 7) is ignored, and in reception the most significant bit (bit 7) is always “0”.

The serial transfer rate is selected by baud rate generator control register 20 (BRGC20).

If a serial data receive error is generated, the receive error contents can be determined by reading the status of asynchronous serial interface status register 20 (ASIS20).

Figure 15-4. Format of SMB Clock Selection Register 0 (2/2)

Symbol	7	6	<5>	<4>	3	2	1	0	Address	After reset	R/W
SMBCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00	FF7AH	00H	R/W[Note]

CL01	CL00	Communication clock	
		SMB/IIC standard mode (SMC0 = 0)	IIC high-speed mode (SMC0 = 1)
0	0	fx/44	fx/24
0	1	fx/86	
1	0	fx/172	fx/48
1	1	Setting prohibited	

Note Bits 4 and 5 are read-only.

Caution To change the communication clock, stop operations (SMBE0 = 0) first before rewriting SMBCL0.

Remark fx: Main system clock oscillation frequency

Table 15-2. SMB0 Communication Clock

SMC0	CL01	CL00	Communication Clock		Digital Filter Input Delay
			At fx = 10.0 MHz operation[Note 1]	At fx = 5.0 MHz operation	
0	0	0	227.2 kHz[Note 2]	113.6 kHz[Note 2]	250 ns
0	0	1	116.2 kHz[Note 2]	58.13 kHz	250 ns
0	1	0	58.13 kHz	29.06 kHz	500 ns
1	0	0	416.6 kHz[Note 3]	208.3 kHz	250 ns
1	0	1	416.6 kHz[Note 3]	208.3 kHz	250 ns
1	1	0	208.3 kHz	104.1 kHz	500 ns
Other than above			Setting prohibited		

Notes 1. Expanded-specification products only.

2. Since the SMB/IIC standard mode standards specify a range of 10 to 100 kHz, this communication clock falls outside the specifications.

3. Since the standards of the IIC high-speed mode specify a range of 0 to 400 kHz, this communication clock falls outside the specifications.

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	!addr16	3	6	$(SP - 1) \leftarrow (PC + 3)_H$, $(SP - 2) \leftarrow (PC + 3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP - 2$			
CALLT	[addr5]	1	8	$(SP - 1) \leftarrow (PC + 1)_H$, $(SP - 2) \leftarrow (PC + 1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP - 2$			
RET		1	6	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
RETI		1	8	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP + 2)$, $SP \leftarrow SP + 3$	R	R	R
PUSH	PSW	1	2	$(SP - 1) \leftarrow PSW$, $SP \leftarrow SP - 1$			
	rp	1	4	$(SP - 1) \leftarrow rp_H$, $(SP - 2) \leftarrow rp_L$, $SP \leftarrow SP - 2$			
POP	PSW	1	4	$PSW \leftarrow (SP)$, $SP \leftarrow SP + 1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP + 1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
MOVW	SP, AX	2	8	$SP \leftarrow AX$			
	AX, SP	2	6	$AX \leftarrow SP$			
BR	!addr16	3	6	$PC \leftarrow$ addr16			
	$addr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8			
	AX	1	6	$PC_H \leftarrow A$, $PC_L \leftarrow X$			
BC	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if CY = 1			
BNC	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if CY = 0			
BZ	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if Z = 1			
BNZ	$saddr16	2	6	$PC \leftarrow PC + 2 +$ jdisp8 if Z = 0			
BT	saddr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if (saddr.bit) = 1			
	sfr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if sfr.bit = 1			
	A.bit, $addr16	3	8	$PC \leftarrow PC + 3 +$ jdisp8 if A.bit = 1			
	PSW.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if PSW.bit = 1			
BF	saddr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if (saddr.bit) = 0			
	sfr.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if sfr.bit = 0			
	A.bit, $addr16	3	8	$PC \leftarrow PC + 3 +$ jdisp8 if A.bit = 0			
	PSW.bit, $addr16	4	10	$PC \leftarrow PC + 4 +$ jdisp8 if PSW.bit = 0			
DBNZ	B, $addr16	2	6	$B \leftarrow B - 1$, then $PC \leftarrow PC + 2 +$ jdisp8 if $B \neq 0$			
	C, $addr16	2	6	$C \leftarrow C - 1$, then $PC \leftarrow PC + 2 +$ jdisp8 if $C \neq 0$			
	saddr, $addr16	3	8	$(saddr) \leftarrow (saddr) - 1$, then $PC \leftarrow PC + 3 +$ jdisp8 if $(saddr) \neq 0$			
NOP		1	2	No Operation			
EI		3	6	$IE \leftarrow 1$ (Enable Interrupt)			
DI		3	6	$IE \leftarrow 0$ (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le AV_{DD} + 0.3\ V$			V
	AV_{REF}	$AV_{REF} \le V_{DD} + 0.3\ V$			V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		−0.3 to +5.5	V
	V_{I3}	P50 to P53	N-ch open drain	−0.3 to +13	V
			On-chip pull-up resistor	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78916x(A1), 78917x(A1)	−4	mA
		Total for all pins		−14	mA
		Per pin	μPD78916x(A2), 78917x(A2)	−2	mA
		Total for all pins		−6	mA
Output current, low	I_{OL}	Per pin	μPD78916x(A1), 78917x(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78916x(A2), 78917x(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78916x(A1), 78917x(A1)		−40 to +110	°C
		μPD78916x(A2), 78917x(A2)		−40 to +125	°C
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

(2) Serial interface 20

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		900			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}				120	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

8-Bit A/D Converter Characteristics (μPD78916x(A1), 78916x(A2))

(T_A = –40 to +110°C (μPD78916x(A1)), –40 to +125°C (μPD78916x(A2))

4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full scale range

10-Bit A/D Converter Characteristics (μPD78917x(A1), 78917x(A2))

(T_A = –40 to +110°C (μPD78917x(A1)), –40 to +125°C (μPD78917x(A2))

4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]				±0.2	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Note]					±0.6	%FSR
Full-scale error[Note]					±0.6	%FSR
Integral linearity error[Note]	INL				±4.5	LSB
Differential linearity error[Note]	DNL				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

(c) AC characteristics

Parameter		Symbol	SMB Mode		Standard Mode I^2C Bus		High-speed Mode I^2C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time Note 1		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	0 Note 2	–	0 Note 2	900 Note 3	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100 Note 4	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in the SMB mode and the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

- If the device extends the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I^2C bus specification).

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11,P60 to P67	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
			V_{DD} = 1.8 to 5.5 V, T_A = 25 to +85°C	0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$,P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
			V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ

Note A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 and P50 to P53 are set to input mode. At times other than this, a –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +105°C) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		7.5	20.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	6.0	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	3000	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	2500	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		1.0	1000	μA
	I_{DD6} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		8.7	22.3	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and port current (including the current flowing through the internal pull-up resistors) is not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) is not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.