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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 6x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkm33z64aclh5

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Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Pre-qualification (Proto)
K	Main family	K = Kinetis
M	Sub family	- M1 = Metering only (No LCD support) - M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	3 = 2 SD ADC with PGA and 1 SD ADC 4 = 2 SD ADC with PGA and 2 SD ADC
A	Key attribute	Z = Cortex-M0+
FFF	Program flash memory size	64 = 64 KB 128 = 128 KB
R	Silicon revision	- Z = Initial (Blank) = Main - A = Second revision
T	Temperature range (°C)	C = -40 to 85
PP	Package identifier	- HH = 44 LGA (5 mm x 5 mm) - LH = 64 LQFP (10 mm x 10 mm) - LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	5 = 50 MHz
N	Packaging type	- R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

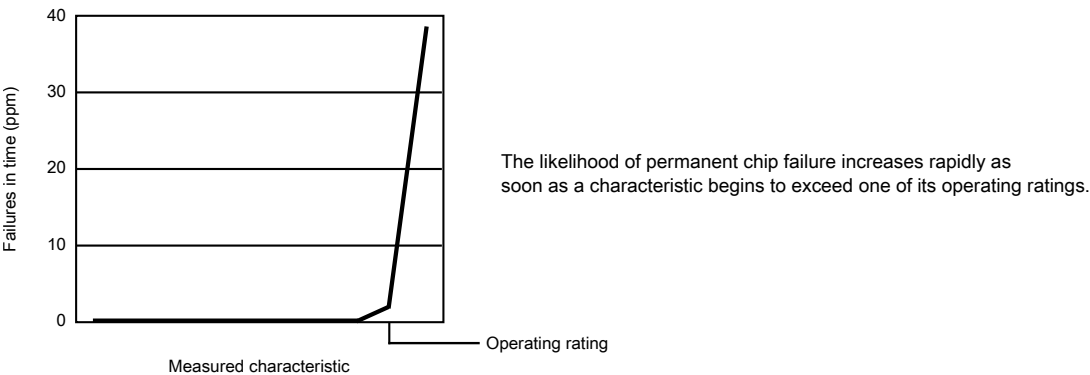
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5 Result of exceeding a rating



4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.6	V
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{DTamper}$	Tamper input voltage	-0.3	$V_{BAT} + 0.3$	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{BAT}	RTC battery supply voltage	-0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

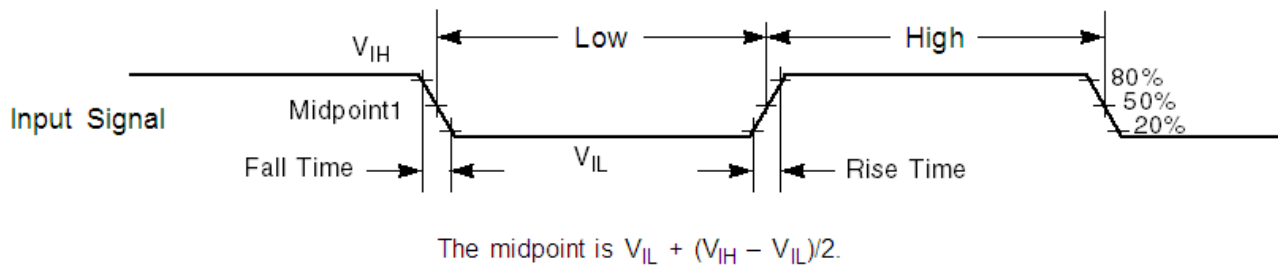


Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — high-drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$	—	0.5	V	
	Output low voltage — low-drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	30	60	$k\Omega$	1,
R_{PD}	Internal pulldown resistors	30	60	$k\Omega$	2

1. Measured at $V_{input} = V_{SS}$

2. Measured at $V_{input} = V_{DD}$

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temp: $-40\text{ }^{\circ}\text{C}$, $25\text{ }^{\circ}\text{C}$, and $85\text{ }^{\circ}\text{C}$
- V_{DD} : 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563	659	μs	1
	• $VLLS0 \rightarrow \text{RUN}$	—	372	μs	
	• $VLLS1 \rightarrow \text{RUN}$	—	372	μs	
	• $VLLS2 \rightarrow \text{RUN}$	—	273	μs	
	• $VLLS3 \rightarrow \text{RUN}$	—	273	μs	
	• $VLPS \rightarrow \text{RUN}$	—	5.0	μs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• STOP → RUN	—	5.0	μs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 3.0 V • 25 °C • -40 °C • 105 °C	— — —	6.17 6.39 6.93	7.1 6.7 8.3	mA mA mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 3.0 V • 25 °C • -40 °C • 105 °C	— — —	8.24 8.26 9.00	10.4 9.8 11.5	mA mA mA	2
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power • 25 °C • -40 °C • 105 °C	— — —	3.95	4.65 4.4 6	mA mA mA	2
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power) • 25 °C • -40 °C • 105 °C	— — —	3.81	4.4 4.2 5.8	mA mA mA	2, 3
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled • 25 °C • -40 °C • 105 °C	— — —	248.8 245.30 535.40	500 470 1800	μA μA μA	4
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled • 25 °C • -40 °C • 105 °C	— — —	343.4 336.62 626.18	530 500 2000	μA μA μA	5

Table continues on the next page...

5.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	44 LGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	63	95	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	50	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	53	79	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	44	45	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	18	28	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{dco_t_DMX32}	DCO output frequency	Low-range (DRS=00) 732 × f _{ints_t}	—	23.99	—	MHz	4, 5, 6
		Mid-range (DRS=01) 1464 × f _{ints_t}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{ints_t}	—	71.99	—	MHz	
		High-range (DRS=11) 2929 × f _{ints_t}	—	95.98	—	MHz	
J _{cyc_fll}	FLL period jitter		—	70	140	ps	7
t _{fll_acquire}	FLL target frequency acquisition time		—	—	1	ms	8
PLL							
f _{vco}	VCO operating frequency		11.71875	12.288	14.6484375	MHz	
I _{pll}	PLL operating current - IO 3.3 V current - Max core voltage current		—	300 100	—	μA	9
f _{pll_ref}	PLL reference frequency range		31.25	32.768	39.0625	kHz	
J _{cyc_pll}	PLL period jitter (RMS) f_{vco} = 12 MHz				700	ps	10
D _{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	11
D _{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time		—	—	150 × 10 ⁻⁶ + 1075(1/f _{pll_ref})	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 5075 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 5075 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.2 Oscillator electrical specifications

6.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) 32 kHz 1 MHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	500	—	nA	1
		—	200	—	μA	
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1) 32 kHz 1 MHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	25	—	μA	1
		—	300	—	μA	
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
Capacitance of EXTAL	247 0.495 - Die level (100 LQFP) - Package level (100 LQFP)	—	—	ff pF		
	Capacitance of XTAL - Die level (100 LQFP) - Package level (100 LQFP)	265 0.495	—	—	ff pF	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

- V_{DD}=3.3 V, Temperature =25 °C
- See crystal or resonator manufacturer's recommendation
- C_x and C_y can be provided by using either integrated capacitors or external components.
- When low-power mode is selected, R_F is integrated and must not be attached externally.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.2.3.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3 Memories and memory interfaces

6.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvp4}	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1

Table continues on the next page...

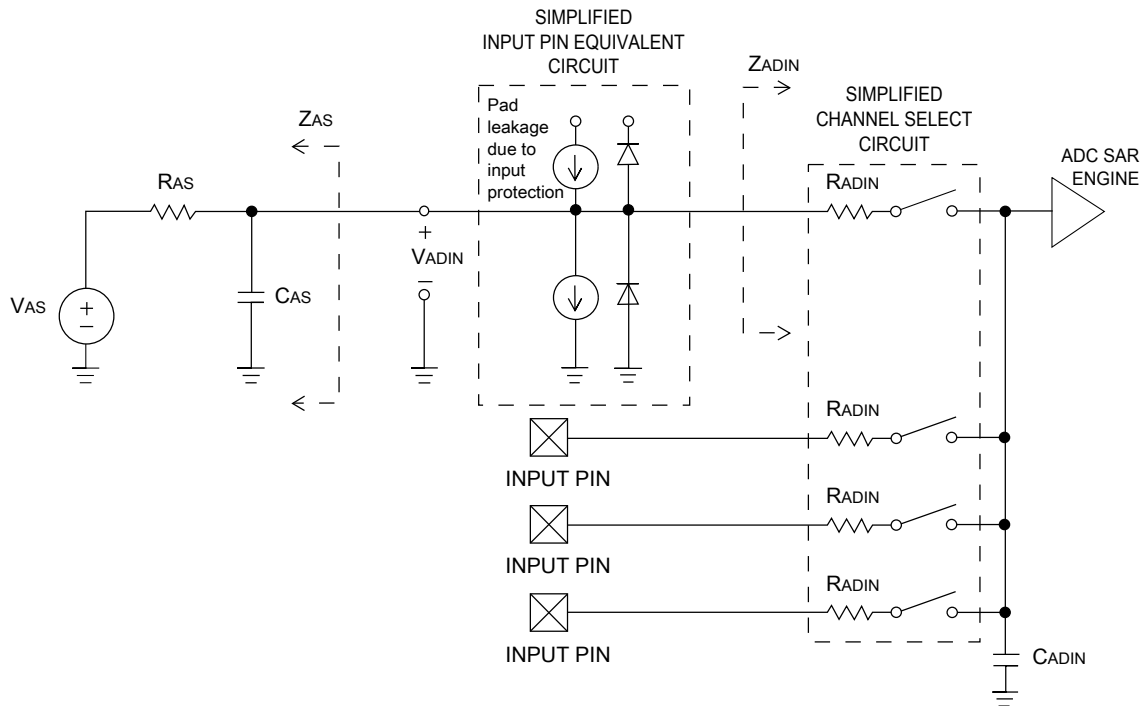


Figure 2. ADC input impedance equivalency diagram

6.4.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f _{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t _{ADACK} = 1/f _{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	−1.1 to +1.9 −0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	−2.7 to +1.9 −0.7 to +0.5	LSB ⁴	5

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_{FS}	Full-scale error	12-bit modes <12-bit modes	—	−4	−5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	16-bit modes 12-bit modes	—	−1 to 0	—	LSB ⁴	
$ENOB$	Effective number of bits	16-bit single-ended mode - Avg = 32 - Avg = 4	12.8	14.5	—	bits	6
			11.9	13.8	—	bits	
			12.2	13.9	—	bits	
			11.4	13.1	—	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times ENOB + 1.76$			dB	
THD	Total harmonic distortion	16-bit single-ended mode Avg = 32	—	−94	—	dB	7
			—	−85	—	dB	
SFDR	Spurious free dynamic range	16-bit single-ended mode Avg = 32	82	95	—	dB	7
			78	90	—	dB	
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

Table 33. VREF limited-range operating behaviours

Symbol	Description	Min.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim	1.173	1.225	V	
VREFL	Voltage reference output	0.38	0.42	V	

6.4.4 AFE electrical specifications

6.4.4.1 $\Sigma\Delta$ ADC + PGA specifications

Table 34. $\Sigma\Delta$ ADC + PGA specifications

Symbol	Description	Conditions	Min	Typ ¹	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
$V_{IN_{diff}}$	Differential input range	Gain = 1 (PGA ON/OFF) ²		+/- 500		mV	
		Gain = 2		+/- 250		mV	
		Gain = 4		+/- 125		mV	
		Gain = 8		+/- 62		mV	
		Gain = 16		+/- 31		mV	
		Gain = 32		+/- 15		mV	

Table continues on the next page...

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25^{\circ}\text{C}$, $f_{\text{MCLK}} = 6.144\text{ MHz}$, $\text{OSR} = 2048$ for Normal mode and $f_{\text{MCLK}} = 768\text{ kHz}$, $\text{OSR} = 256$ for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See [General switching specifications](#).

6.6 Communication interfaces

6.6.1 I2C switching specifications

See [General switching specifications](#).

6.6.2 UART switching specifications

See [General switching specifications](#).

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6) (continued)

Description	Min.	Max.	Unit	Notes
SCK frequency - Master - Slave		9 9	MHz Mhz	
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) - Master - Slave	42 3.5		ns	
Input Data Hold Time (inputs, tHI) - Master - Slave	0 1		ns	
Data hold time (outputs, tHO) - Master - Slave	-3 0		ns	
Data Valid Out Time (tDVO) - Master - Slave	16 44		ns	1
Rise time input - Master - Slave	1 1		ns	
Fall time input - Master - Slave	1 1		ns	
Rise time output - Master - Slave	14.4 14.4		ns	
Fall time output - Master - Slave	12.4 12.4		ns	

1. SCK frequency of 9 Mhz is applicable only in the case that the input setup time of the device outside is not more than 11.5 ns, else the frequency would need to be lowered.

The following table represents SPI Switching specification in OD cells

Table 38. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Data Setup Time (inputs, tSUI) - Master - Slave	51 4		ns	
Input Data Hold Time (inputs, tHI) - Master - Slave	0 1		ns	
Data hold time (outputs, tHO) - Master - Slave	-15 0		ns	
Data Valid Out Time (tDVO) - Master - Slave	61 93		ns	

Table continues on the next page...

8.3.1 100-pin LQFP

Figure below shows the KM 100 LQFP pinouts.

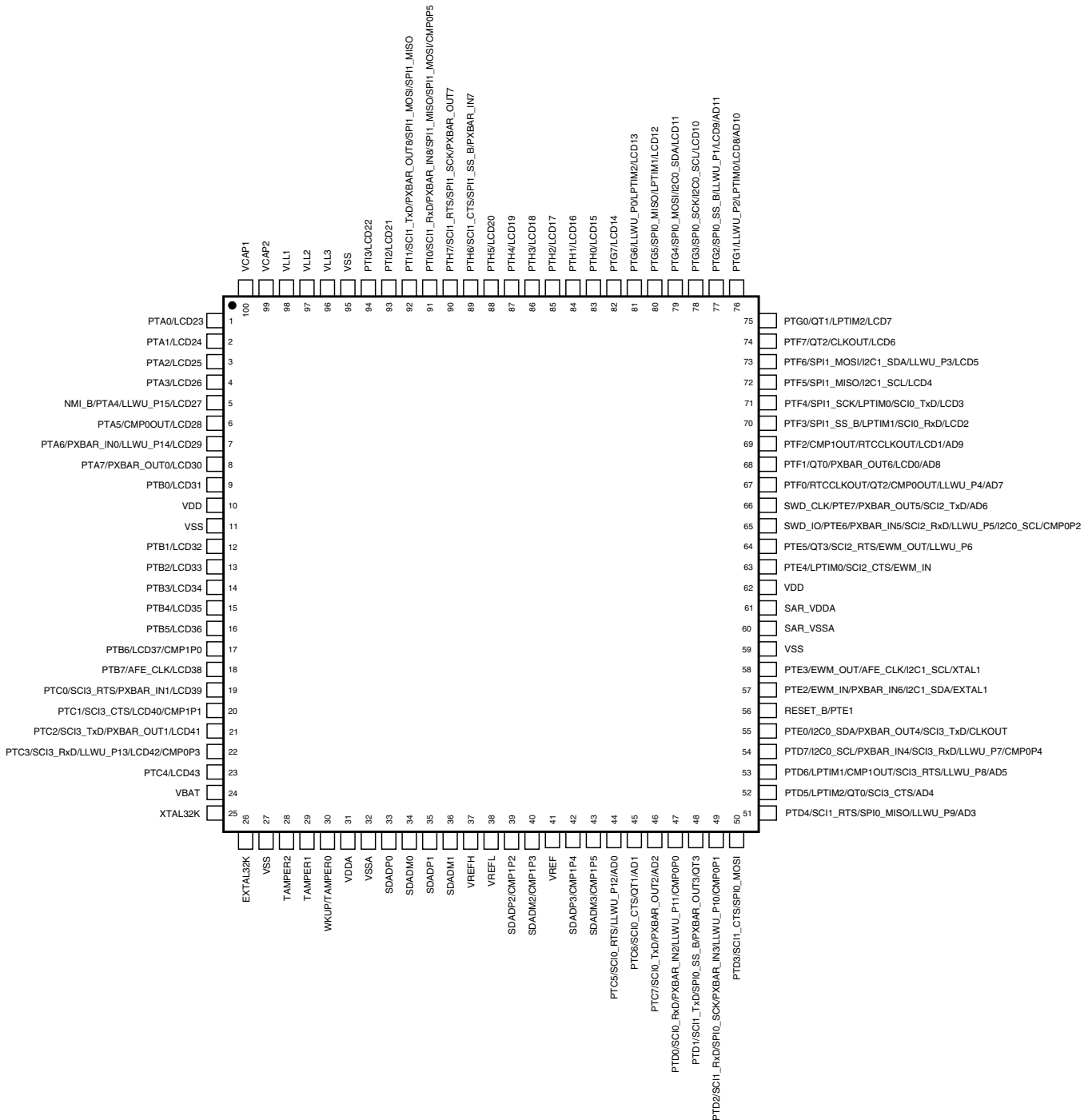


Figure 6. 100-pin LQFP Pinout Diagram

8.3.2 64-pin LQFP

Figure below shows the 64-pin LQFP pinouts.

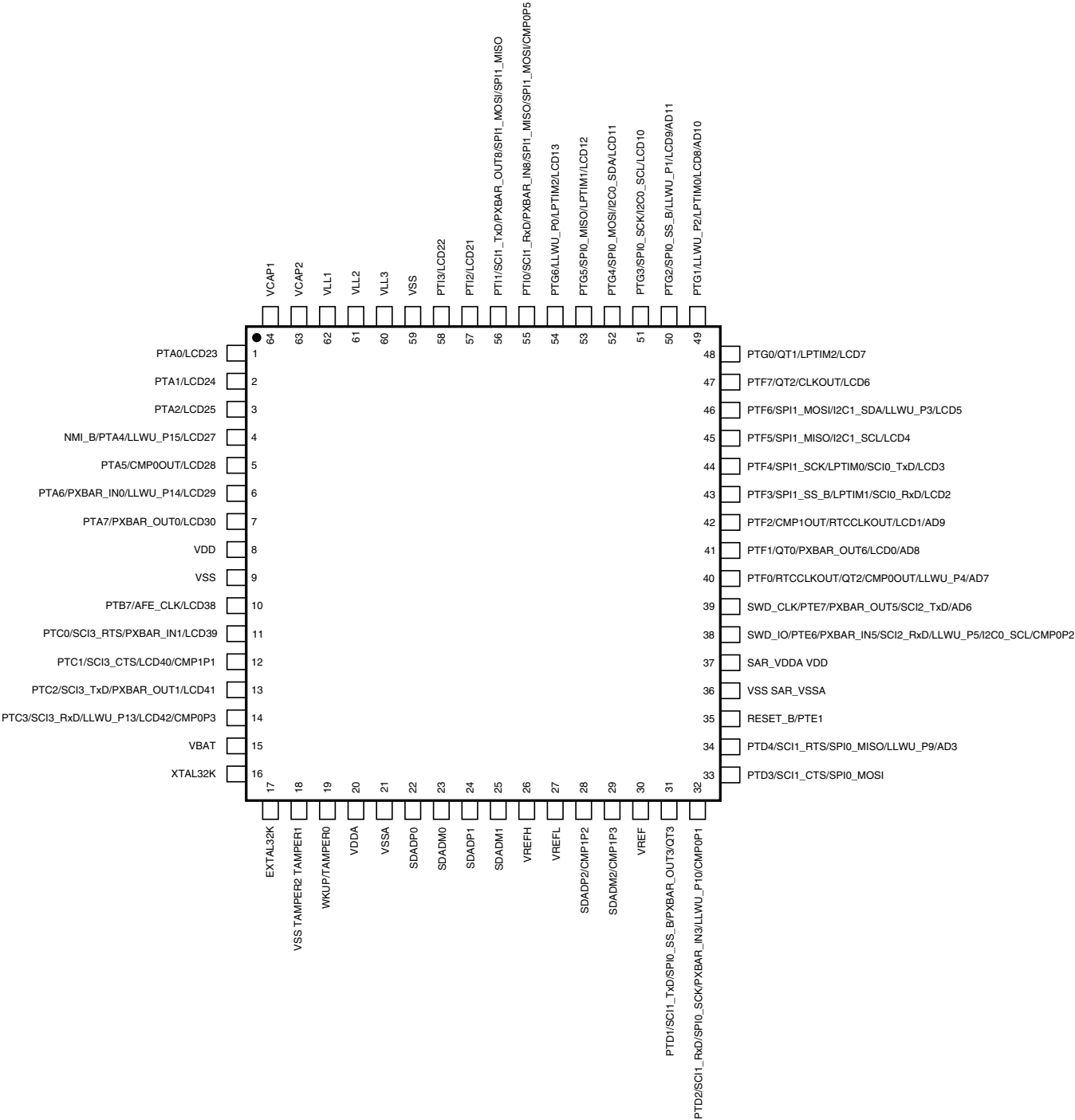


Figure 7. 64-pin LQFP Pinout Diagram

8.3.3 44-pin LGA

Figure below shows the 44-pin LGA pinouts.

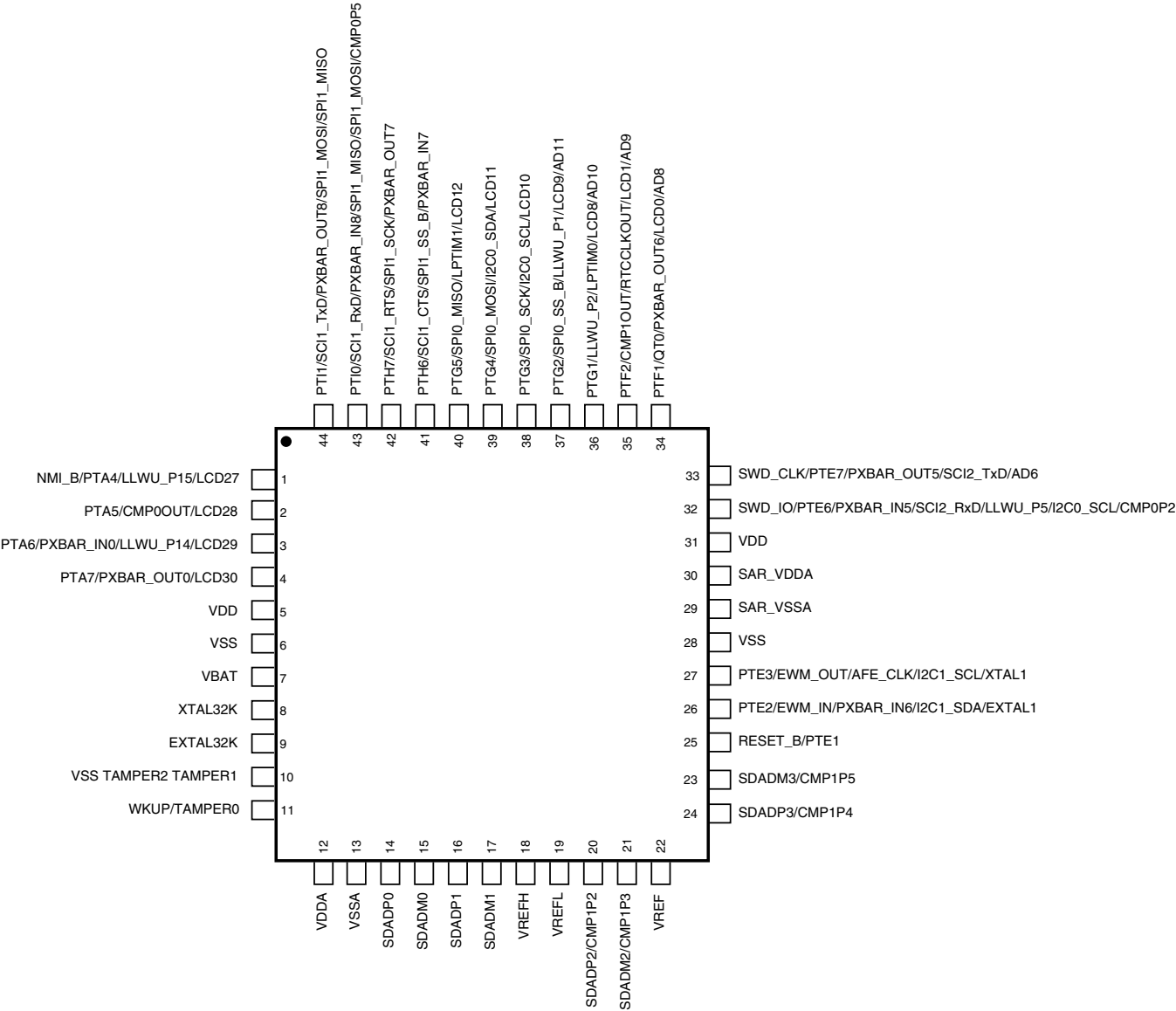


Figure 8. 44-pin LGA Pinout Diagram

NOTE

VSS also connects to flag on 44 LGA.

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