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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details	
Product Status	Active
Core Processor	-
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Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm33z64acll5

1 Ordering parts

1.1 Determining valid order-able parts

Valid order-able part numbers are provided on the web. To determine the order-able part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM14Z64ACHH5
- MKM14Z128ACHH5
- MKM33Z64ACLH5
- MKM33Z128ACLH5
- MKM33Z64ACLL5
- MKM33Z128ACLL5
- MKM34Z128ACLL5

NOTE

It is recommended to order the RevA part numbers for the KM parts.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K M S A FFF R T PP CC N

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification (Proto)
K	Main family	• K = Kinetis
M	Sub family	• M1 = Metering only (No LCD support) • M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	• 3 = 2 SD ADC with PGA and 1 SD ADC • 4 = 2 SD ADC with PGA and 2 SD ADC
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Second revision
T	Temperature range (°C)	• C = –40 to 85
PP	Package identifier	• HH = 44 LGA (5 mm x 5 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
$V_{DTamper}$	Tamper input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{BAT}	RTC battery supply voltage	–0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

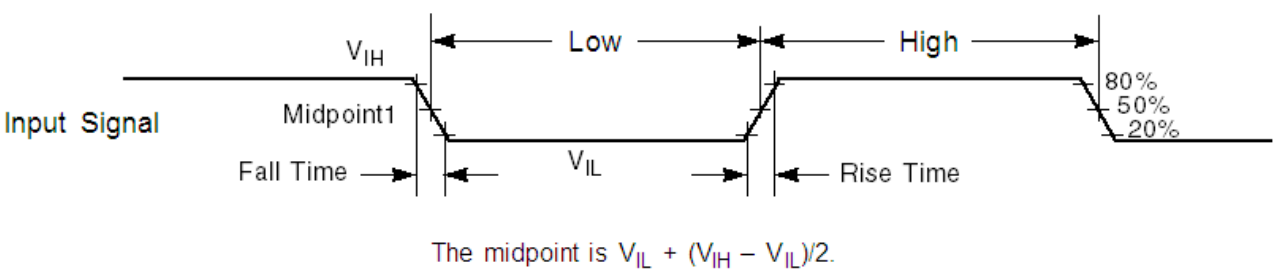

Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 10 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
	Output low voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	30	60	kΩ	1,
R_{PD}	Internal pulldown resistors	30	60	kΩ	2

1. Measured at Vinput = V_{SS}
2. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temp: -40 °C, 25 °C, and 85 °C
- V_{DD}: 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563	659	µs	1
	• VLLS0 → RUN	—	372	µs	
	• VLLS1 → RUN	—	372	µs	
	• VLLS2 → RUN	—	273	µs	
	• VLLS3 → RUN	—	273	µs	
	• VLPS → RUN	—	5.0	µs	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled					6
	• 25 °C	—	162	350	µA	
	• -40 °C	—	158.50	330	µA	
	• 105 °C	—	446.94	1700	µA	
I_{DD_STOP}	Stop mode current at 3.0 V					
	• 25 °C	—	311.90	730	µA	
	• -40 °C	—	364	700	µA	
	• 105 °C	—	645.13	2250	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• 25 °C	—	8.56	46	µA	
	• -40 °C	—		44	µA	
	• 105 °C	—		1500	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• 25 °C	—	1.98	3.5	µA	
	• -40 °C	—		3.3	µA	
	• 105 °C	—		85	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• 25 °C	—	1.24	2.6	µA	
	• -40 °C	—		2.5	µA	
	• 105 °C	—		59.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• 25 °C	—	0.89	1.7	µA	
	• -40 °C	—		1.6	µA	
	• 105 °C	—		38.8	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• 25 °C	—	0.35	0.67	µA	
	• -40 °C	—		0.64	µA	
	• 105 °C	—		38	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• 25 °C	—	0.472	0.76	µA	
	• -40 °C	—		0.72	µA	
	• 105 °C	—		38.4	µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF					
	• 25 °C	—	0.3	1	µA	
	• -40 °C	—		0.95	µA	
	• 105 °C	—		15	µA	

Table continues on the next page...

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock		50	MHz	
f_{BUS}	Bus clock		25	MHz	
f_{FLASH}	Flash clock		25	MHz	
f_{AFE}	AFE Modulator clock		6.5	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock		2	MHz	
f_{BUS}	Bus clock		1	MHz	
f_{FLASH}	Flash clock		1	MHz	
f_{AFE}	AFE Modulator clock[2]		1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

6.2.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.2.3 32 kHz oscillator electrical characteristics

6.2.3.1 32 kHz oscillator DC electrical specifications

Table 21. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

6.4.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

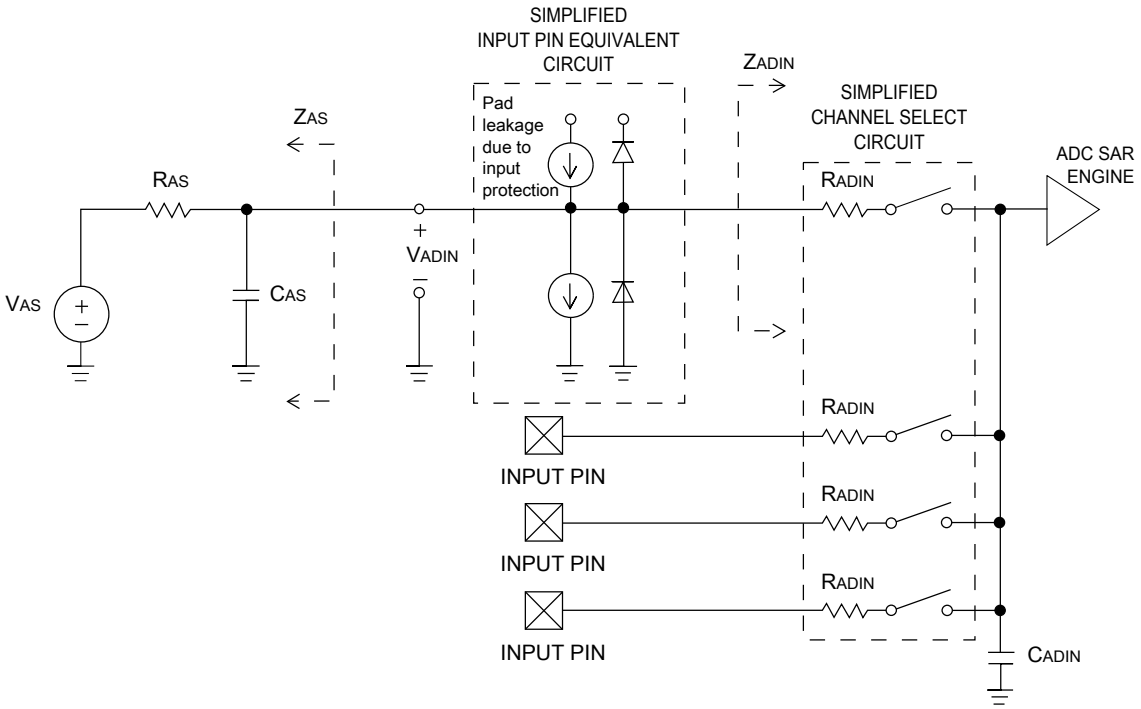

Figure 2. ADC input impedance equivalency diagram

6.4.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.5	–0.7 to +0.5		

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

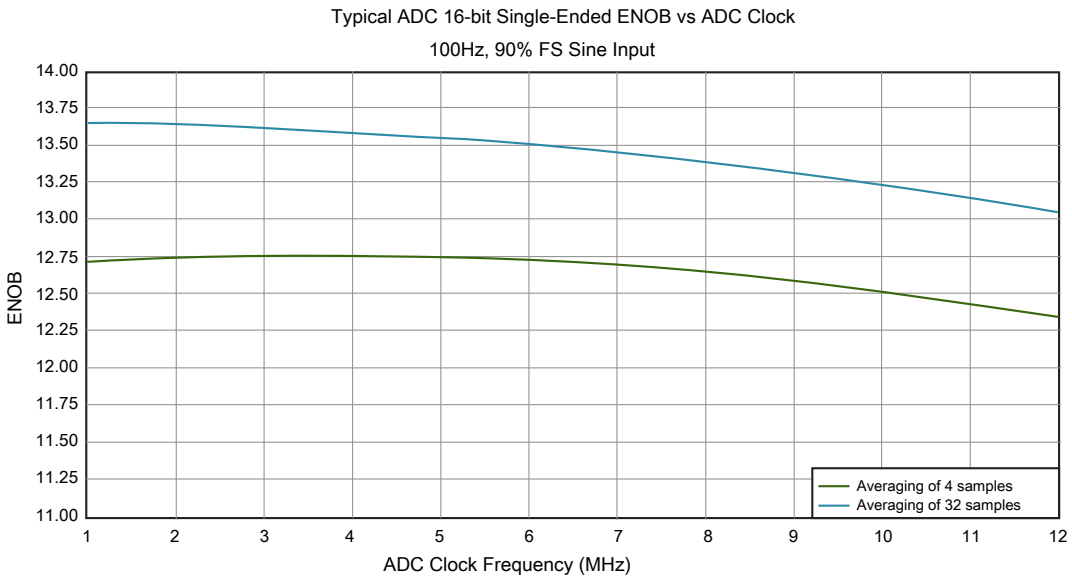

Figure 3. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.4.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1] • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	— — — —	5 10 20 30	— — — —	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

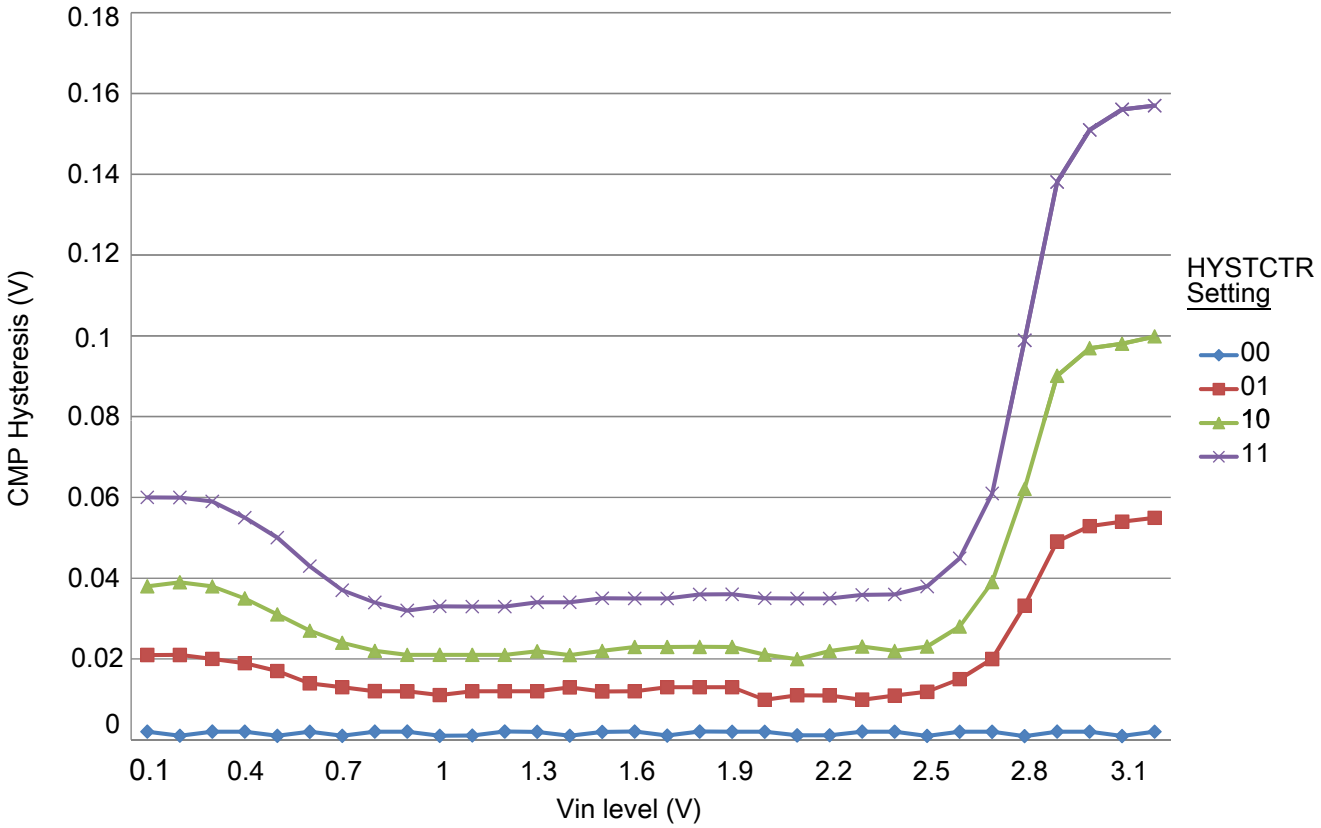

Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71[1]	3.6	V	
T_A	Temperature	–40	85	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed ±25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.195	1.2027	V	

Table continues on the next page...

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	90 88 82 76 70 64	92 90 86 82 78 74		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	82 76 70 64 58 52	82 78 74 70 66 62		dB	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	

Table continues on the next page...

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder	—	15	—	µA	
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	3	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)					
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

NOTE

- For devices other than MKMx4, the SDADP3 and SDADM3 functions on the corresponding pins are disabled.
- All input pins including TAMPER pins must be pulled up or down to avoid extra power consumption.

8.2 KM Signal Multiplexing and Pin Assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	Disabled	LCD23	PTA0						
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	PXBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	PXBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						
18	10	—	Disabled	LCD38	PTB7	AFE_CLK					
19	11	—	Disabled	LCD39	PTC0	SCI3_RTS	PXBAR_IN1				
20	12	—	Disabled	LCD40/ CMP1P1	PTC1	SCI3_CTS					
21	13	—	Disabled	LCD41	PTC2	SCI3_TxD	PXBAR_OUT1				
22	14	—	Disabled	LCD42/ CMP0P3	PTC3	SCI3_RxD	LLWU_P13				
23	—	—	Disabled	LCD43	PTC4						
24	15	7	VBAT	VBAT							
25	16	8	XTAL32K	XTAL32K							
26	17	9	EXTAL32K	EXTAL32K							
27	18	10	VSS	VSS							
28	18	10	TAMPER2	TAMPER2							
29	18	10	TAMPER1	TAMPER1							
30	19	11	WKUP	TAMPER0							

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
68	41	34	Disabled	LCD0/ AD8	PTF1	QT0	PXBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTIM1	SCI0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTIM0	SCI0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL				
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	QT2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	QT1	LPTIM2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTIM0				
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTIM1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTIM2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	SCI1_CTS	SPI1_SS_B	PXBAR_IN7			
90	—	42	Disabled		PTH7	SCI1_RTS	SPI1_SCK	PXBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	SCI1_RxD	PXBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	SCI1_TxD	PXBAR_OUT8	SPI1_MOSI	SPI1_MISO		
93	57	—	Disabled	LCD21	PTI2						
94	58	—	Disabled	LCD22	PTI3						
95	59	—	VSS	VSS							
96	60	—	VLL3	VLL3							
97	61	—	VLL2	VLL2							
98	62	—	VLL1	VLL1							
99	63	—	VCAP2	VCAP2							
100	64	—	VCAP1	VCAP1							

8.3 KM Family Pinouts

8.3.1 100-pin LQFP

Figure below shows the KM 100 LQFP pinouts.

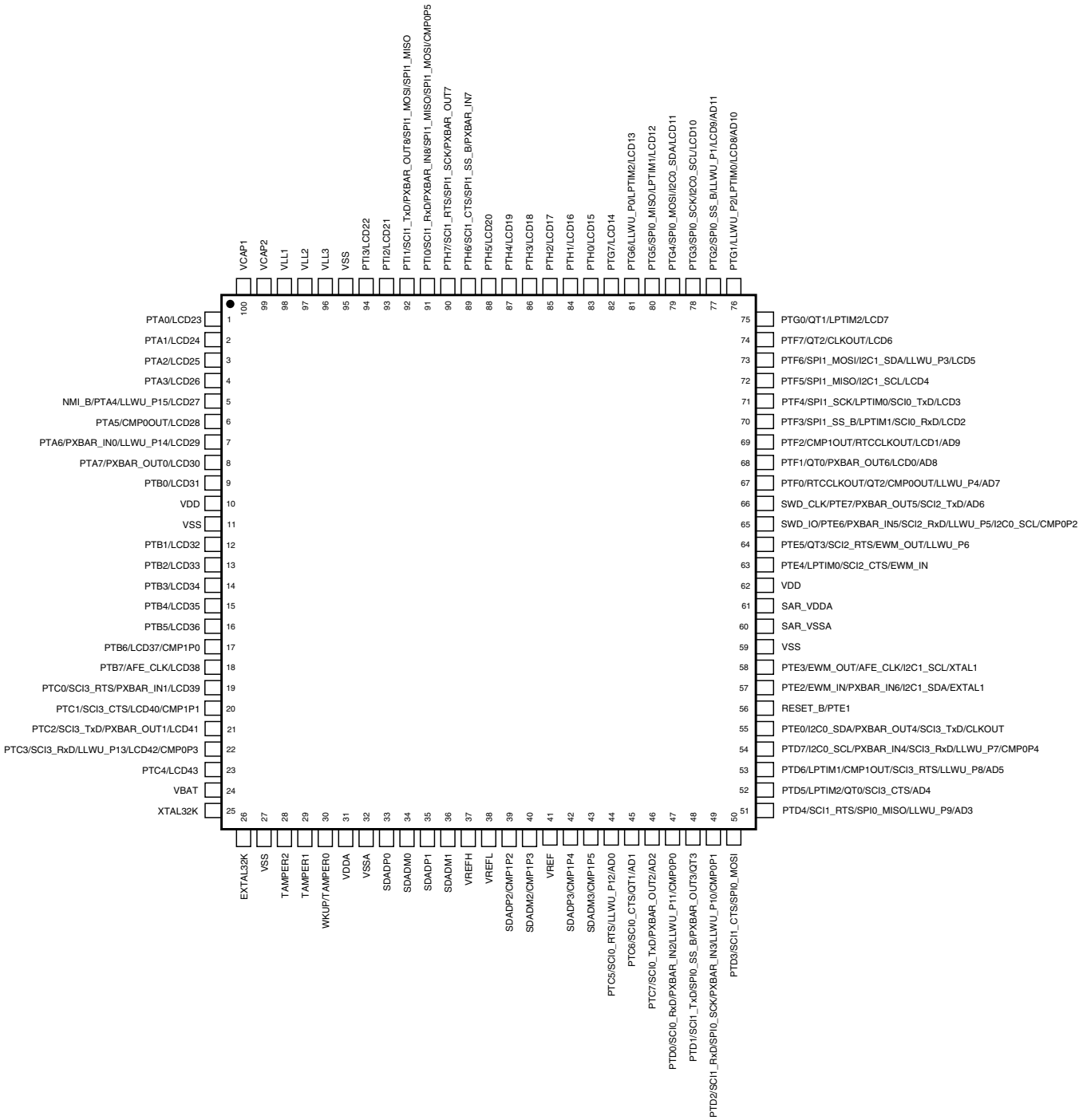

Figure 6. 100-pin LQFP Pinout Diagram

8.3.2 64-pin LQFP

Figure below shows the 64-pin LQFP pinouts.

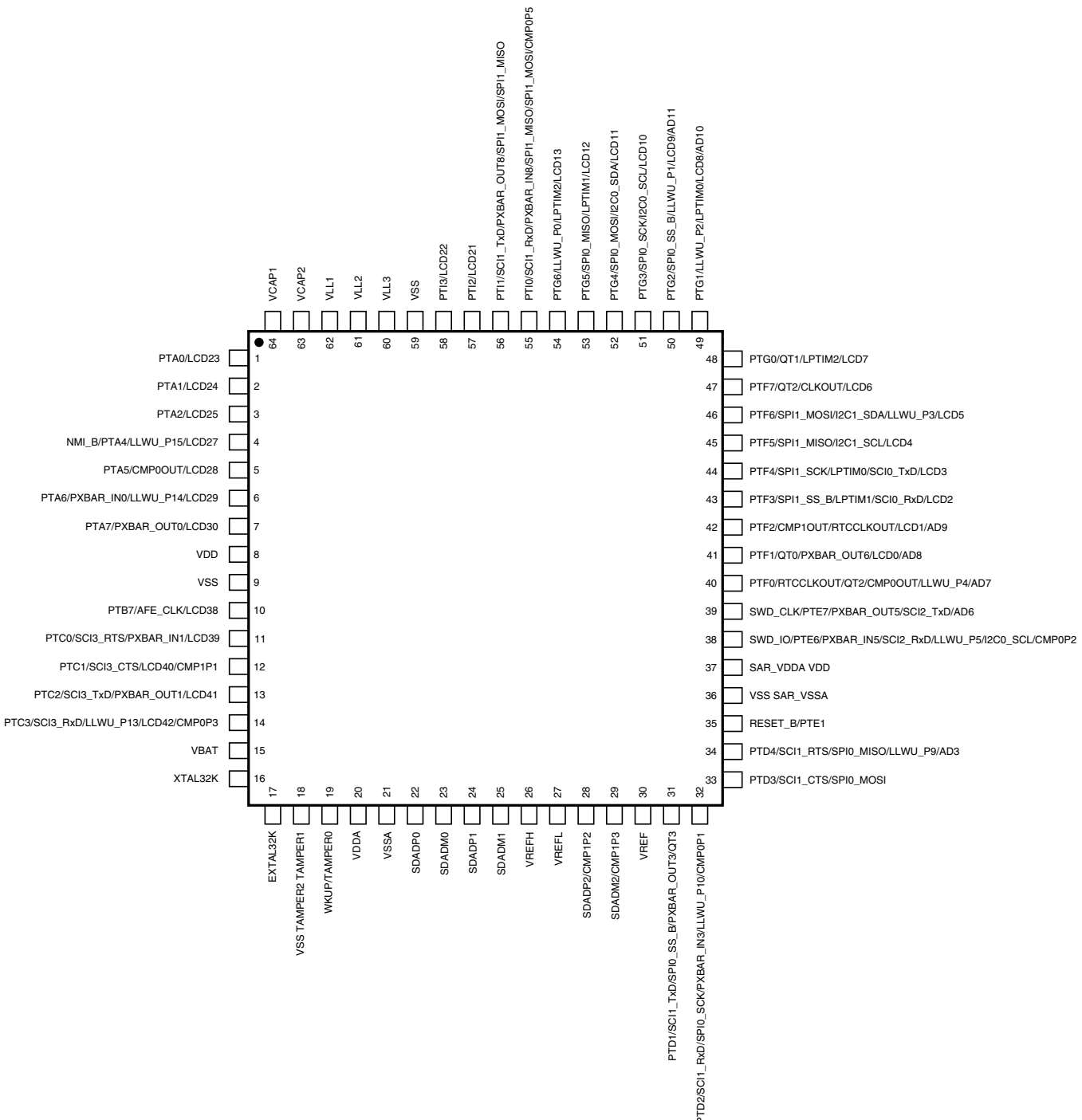

Figure 7. 64-pin LQFP Pinout Diagram