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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm34z128acll5

1 Ordering parts

1.1 Determining valid order-able parts

Valid order-able part numbers are provided on the web. To determine the order-able part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM14Z64ACHH5
- MKM14Z128ACHH5
- MKM33Z64ACLH5
- MKM33Z128ACLH5
- MKM33Z64ACLL5
- MKM33Z128ACLL5
- MKM34Z128ACLL5

NOTE

It is recommended to order the RevA part numbers for the KM parts.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K M S A FFF R T PP CC N

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

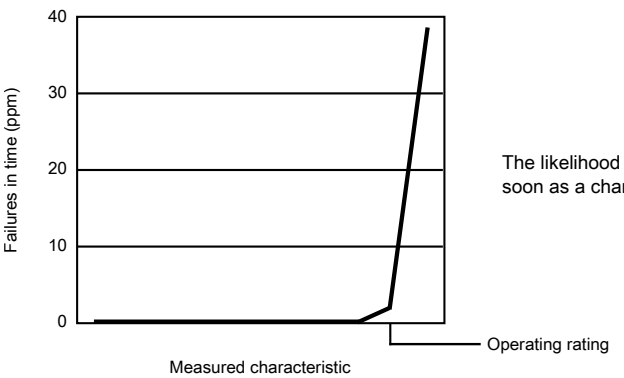
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	-4000	+4000	V	1
	Electrostatic discharge voltage, human body model (RESET pin only)	-2500	+2500	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	-750	+750	V	2
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	3
V_{PESD}	Powered ESD voltage	-6000	+6000	V	
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V_{DDA}	Analog supply voltage	2.7	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -3 —	 — +3	mA	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes

I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.
	• @ 3.0 V
	  • 25 °C
	  • -40 °C
	  • 105 °C
		—	1.3 [7]	3
				2.5
				16
					µA
					µA
					µA
						8, 9

1. See AFE specification for IDDA.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 µA.
4. 2 MHz core, system, bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core, system and bus clock, and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core, system and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Current consumption will vary with number of CPU accesses done and is dependent on the frequency of the accesses and frequency of bus clock. Number of CPU accesses should be optimized to get optimal current value.
8. Includes 32 kHz oscillator current and RTC operation.
9. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	16	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 50 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock		50	MHz	
f_{BUS}	Bus clock		25	MHz	
f_{FLASH}	Flash clock		25	MHz	
f_{AFE}	AFE Modulator clock		6.5	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock		2	MHz	
f_{BUS}	Bus clock		1	MHz	
f_{FLASH}	Flash clock		1	MHz	
f_{AFE}	AFE Modulator clock[2]		1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

5.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	44 LGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	63	95	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	50	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	53	79	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	44	45	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	18	28	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	—	%	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over fixed voltage and full operating temperature range		-2	—	+2	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7		$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.4	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
Δf_{intf_t}	Total deviation of internal reference frequency (fast clock) over voltage and temperature — factory trimmed at nominal VDD and 25°C		—	+1/-2	—	%	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{dco}	DCO output frequency range	Low-range (DRS=00) 640 × f_{ints_t}	20	20.97	22	MHz	2, 3
		Mid-range (DRS=01) 1280 × f_{ints_t}	40	41.94	45	MHz	
		Mid-high range (DRS=10) 1920 × f_{ints_t}	60	62.91	67	MHz	
		High-range (DRS=11) 2560 × f_{ints_t}	80	83.89	90	MHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$f_{dco\_t\_DMX32}$	DCO output frequency	Low-range (DRS=00) $732 \times f_{ints\_t}$	—	23.99	—	MHz	4, 5, 6
		Mid-range (DRS=01) $1464 \times f_{ints\_t}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{ints\_t}$	—	71.99	—	MHz	
		High-range (DRS=11) $2929 \times f_{ints\_t}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	70	140	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8
PLL							
f_{vco}	VCO operating frequency		11.71875	12.288	14.6484375	MHz	
I_{pll}	PLL operating current • IO 3.3 V current • Max core voltage current		—	300 100	—	µA	9
f_{pll_ref}	PLL reference frequency range		31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 12 MHz				700	ps	10
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	11
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 5075 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 5075 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.3.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2 , 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3 Memories and memory interfaces

6.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1

Table continues on the next page...

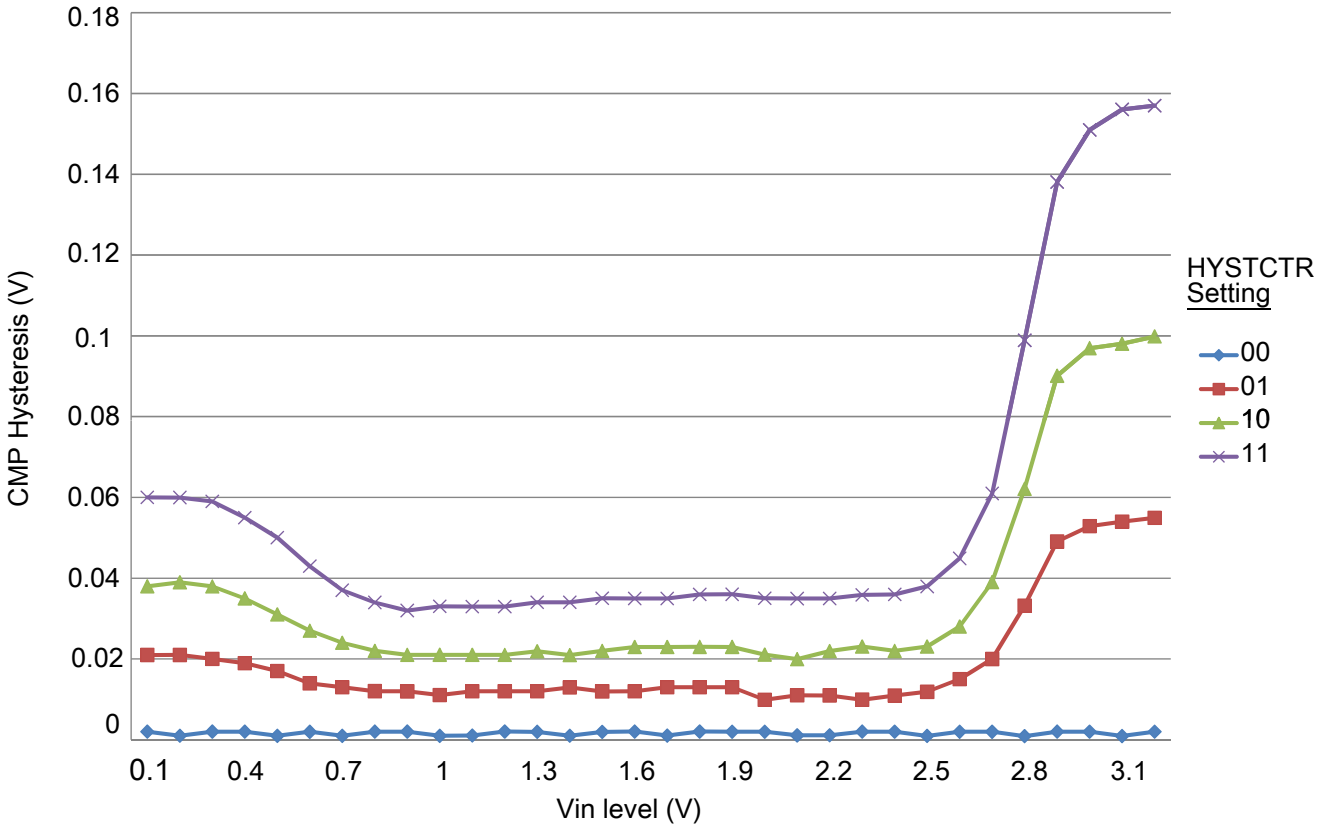


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71[1]	3.6	V	
T_A	Temperature	–40	85	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed ±25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.195	1.2027	V	

Table continues on the next page...

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	90 88 82 76 70 64	92 90 86 82 78 74		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	82 76 70 64 58 52	82 78 74 70 66 62		dB	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	

Table continues on the next page...

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			+/- 5	mV	
$\Delta Offset_{Temp}$	Offset Temperature Drift[3]	Gain=01, V_{pp}=1000mV (full range diff.)			+/- 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts[4]	• Gain=01, V_{pp}=500mV (differential ended) • Gain=32, V_{pp}=15mV (differential ended)			+/- 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each chanel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			1.4 0.5	mA	
R_{as}	Equivalent input impedance per single channel	PGA enabled		8		kΩ	

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5Vpp
3. Represents combined offset temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.
4. Represents combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks.
5. PGA is disabled in low-power modes.

6.4.4.2 ΣΔ ADC Standalone specifications

Table 35. ΣΔ ADC standalone specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode Low-Power Mode	1.5 1.5	1.5 1.5	1.5 1.5	kHz	
V_{CM}	Input Common Mode Reference		0		0.8	V	

Table continues on the next page...

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

6.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides some reference values to be met on SoC.

Table 36. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	1
SCK frequency • Master • Slave	2	12.5 12.5	MHz Mhz	3
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	25 3		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	13 28		ns	
Rise time input • Master • Slave	1 1		ns	
Fall time input • Master • Slave	1 1		ns	
Rise time output • Master • Slave	8.9 8.9		ns	
Fall time output • Master • Slave	7.8 7.8		ns	

1. SPI modules will work on core clock.
2. F_{sys}/(Max Divider Value from registers)
3. F_{SYS}/2 in Master mode and F_{SYS}/4 in Slave mode. F_{SYS}/4 in Master as well as Slave Modes, where F_{SYS}=50Mhz

NOTE

The values assumed for input transition and output load are:
Input transition = 1 ns Output load = 50 pF

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	

Table continues on the next page...

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
31	20	12	VDDA	VDDA							
32	21	13	VSSA	VSSA							
33	22	14	SDADP0	SDADP0							
34	23	15	SDADM0	SDADM0							
35	24	16	SDADP1	SDADP1							
36	25	17	SDADM1	SDADM1							
37	26	18	VREFH	VREFH							
38	27	19	VREFL	VREFL							
39	28	20	SDADP2/ CMP1P2	SDADP2/ CMP1P2							
40	29	21	SDADM2/ CMP1P3	SDADM2/ CMP1P3							
41	30	22	VREF	VREF							
42	—	24	SDADP3/ CMP1P4	SDADP3/ CMP1P4							
43	—	23	SDADM3/ CMP1P5	SDADM3/ CMP1P5							
44	—	—	Disabled	AD0	PTC5	SCI0_RTS	LLWU_P12				
45	—	—	Disabled	AD1	PTC6	SCI0_CTS	QT1				
46	—	—	Disabled	AD2	PTC7	SCI0_TxD	PXBAR_OUT2				
47	—	—	Disabled	CMP0P0	PTD0	SCI0_RxD	PXBAR_IN2	LLWU_P11			
48	31	—	Disabled		PTD1	SCI1_TxD	SPI0_SS_B	PXBAR_OUT3	QT3		
49	32	—	Disabled	CMP0P1	PTD2	SCI1_RxD	SPI0_SCK	PXBAR_IN3	LLWU_P10		
50	33	—	Disabled		PTD3	SCI1_CTS	SPI0_MOSI				
51	34	—	Disabled	AD3	PTD4	SCI1_RTS	SPI0_MISO	LLWU_P9			
52	—	—	Disabled	AD4	PTD5	LPTIM2	QT0	SCI3_CTS			
53	—	—	Disabled	AD5	PTD6	LPTIM1	CMP1OUT	SCI3_RTS	LLWU_P8		
54	—	—	Disabled	CMP0P4	PTD7	I2C0_SCL	PXBAR_IN4	SCI3_RxD	LLWU_P7		
55	—	—	Disabled		PTE0	I2C0_SDA	PXBAR_OUT4	SCI3_TxD	CLKOUT		
56	35	25	RESET_B		PTE1						RESET_B
57	—	26	EXTAL1	EXTAL1	PTE2	EWM_IN	PXBAR_IN6	I2C1_SDA			
58	—	27	XTAL1	XTAL1	PTE3	EWM_OUT	AFE_CLK	I2C1_SCL			
59	36	28	VSS	VSS							
60	36	29	SAR_VSSA	SAR_VSSA							
61	37	30	SAR_VDDA	SAR_VDDA							
62	37	31	VDD	VDD							
63	—	—	Disabled		PTE4	LPTIM0	SCI2_CTS	EWM_IN			
64	—	—	Disabled		PTE5	QT3	SCI2_RTS	EWM_OUT	LLWU_P6		
65	38	32	SWD_IO	CMP0P2	PTE6	PXBAR_IN5	SCI2_RxD	LLWU_P5	I2C0_SCL		SWD_IO
66	39	33	SWD_CLK	AD6	PTE7	PXBAR_OUT5	SCI2_TxD		I2C0_SDA		SWD_CLK
67	40	—	Disabled	AD7	PTF0	RTCCLKOUT	QT2	CMP0OUT	LLWU_P4		

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
68	41	34	Disabled	LCD0/ AD8	PTF1	QT0	PXBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTIM1	SCI0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTIM0	SCI0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL				
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	QT2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	QT1	LPTIM2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTIM0				
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTIM1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTIM2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	SCI1_CTS	SPI1_SS_B	PXBAR_IN7			
90	—	42	Disabled		PTH7	SCI1_RTS	SPI1_SCK	PXBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	SCI1_RxD	PXBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	SCI1_TxD	PXBAR_OUT8	SPI1_MOSI	SPI1_MISO		
93	57	—	Disabled	LCD21	PTI2						
94	58	—	Disabled	LCD22	PTI3						
95	59	—	VSS	VSS							
96	60	—	VLL3	VLL3							
97	61	—	VLL2	VLL2							
98	62	—	VLL1	VLL1							
99	63	—	VCAP2	VCAP2							
100	64	—	VCAP1	VCAP1							

8.3 KM Family Pinouts

8.3.2 64-pin LQFP

Figure below shows the 64-pin LQFP pinouts.

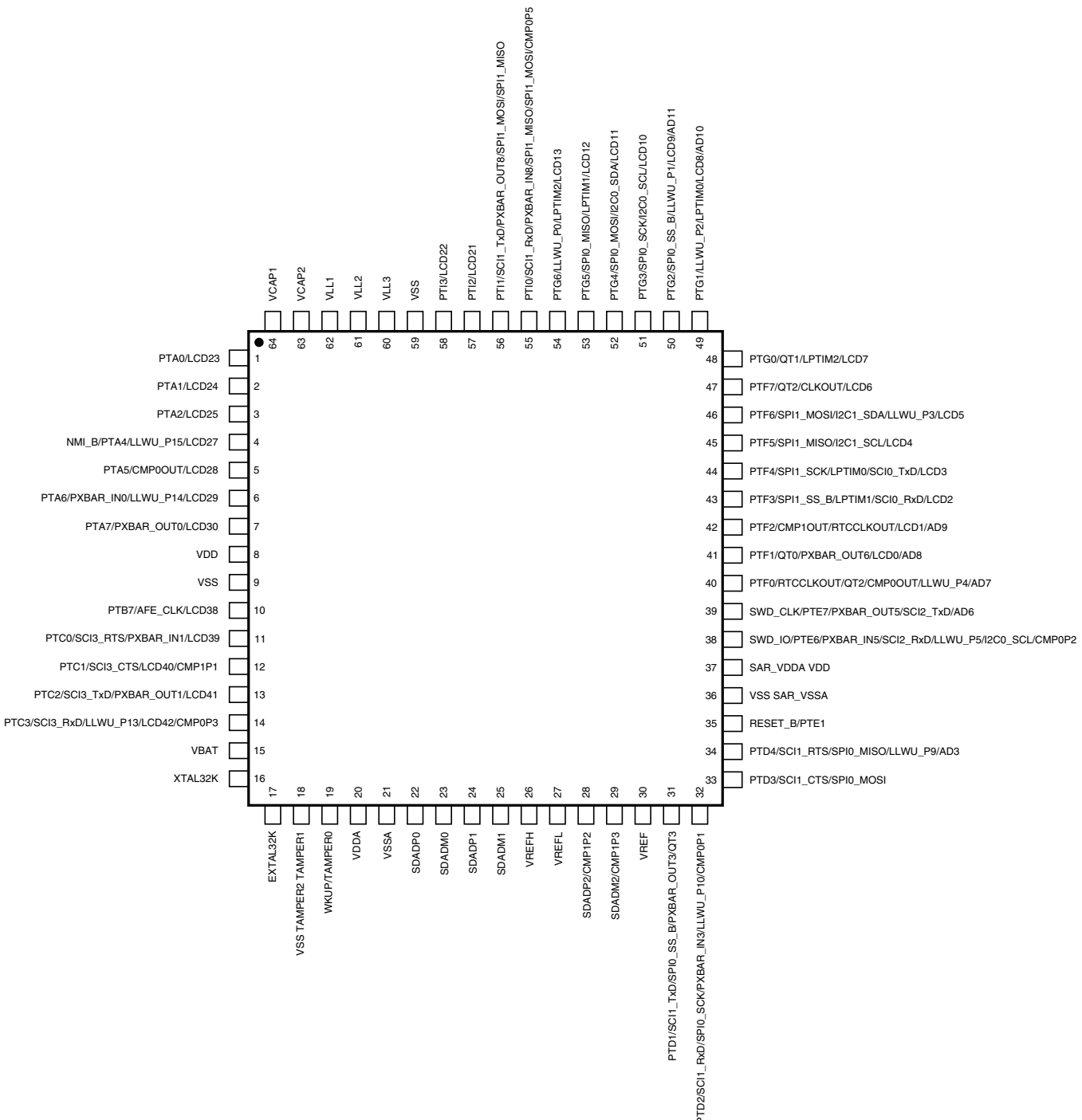


Figure 7. 64-pin LQFP Pinout Diagram

8.3.3 44-pin LGA

Figure below shows the 44-pin LGA pinouts.

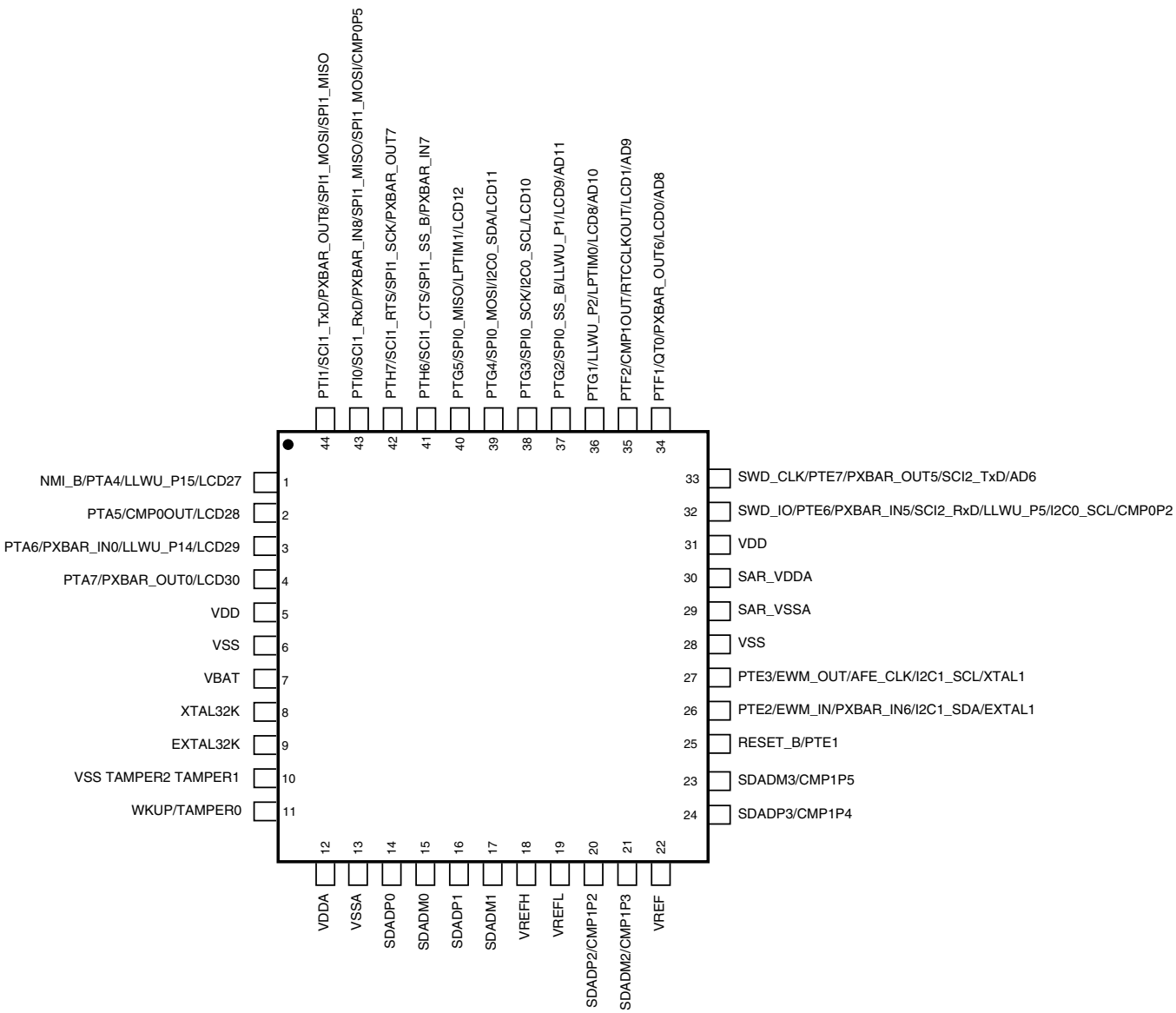


Figure 8. 44-pin LGA Pinout Diagram

NOTE

VSS also connects to flag on 44 LGA.

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