NXP USA Inc. - MKM34Z128ACLL5R Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm34z128acll5r

- Communication interfaces
  - One SPI module with FIFO support (supports 5V AMR operation)
  - One SPI module without FIFO (no AMR operation)
  - Two I2C modules with SMBus support
  - Two UART modules with ISO7816 support and Two UART without ISO 7816 support
  - Any one SCI can be used for IrDA operation. 5V AMR support on one SCI.

1 Ordering parts

1.1 Determining valid order-able parts

Valid order-able part numbers are provided on the web. To determine the order-able part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM14Z64ACHH5
- MKM14Z128ACHH5
- MKM33Z64ACLH5
- MKM33Z128ACLH5
- MKM33Z64ACLL5
- MKM33Z128ACLL5
- MKM34Z128ACLL5

NOTE

It is recommended to order the RevA part numbers for the KM parts.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K M S A FFF R T PP CC N

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

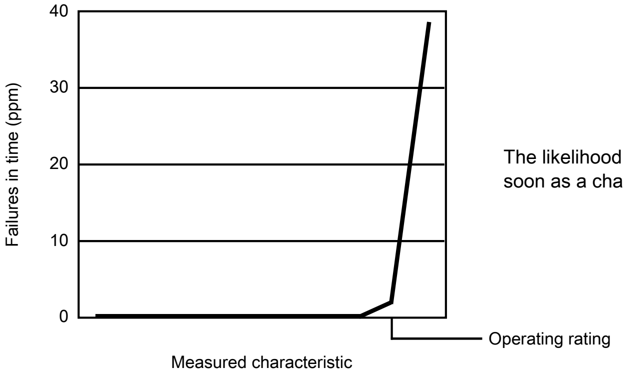
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

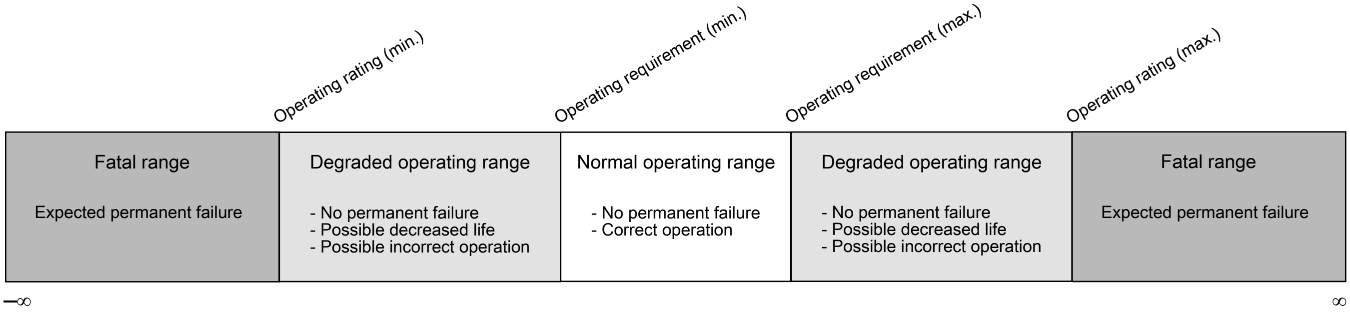
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating

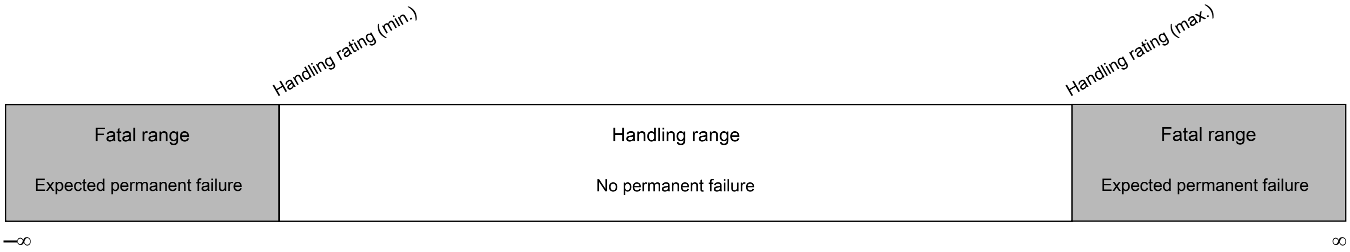


The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

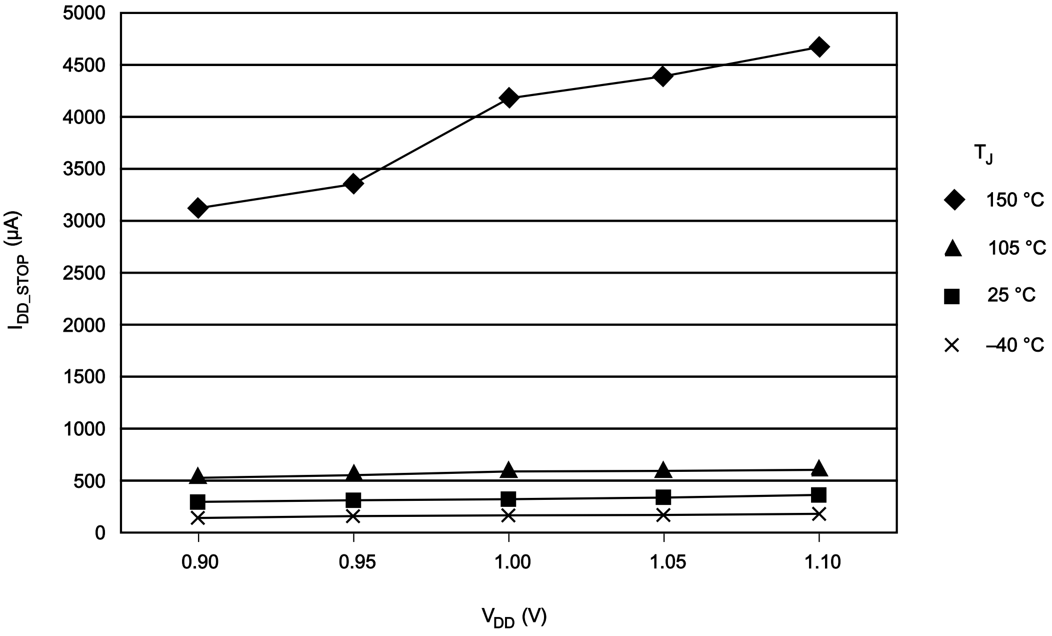
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high-drive strength				
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$, $I_{OH} = 20$ mA	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \leq V_{DD} \leq 2.7\ V$, $I_{OH} = 10$ mA	$V_{DD} - 0.5$	—	V	
	Output high voltage — low-drive strength				
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$, $I_{OH} = 5$ mA	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \leq V_{DD} \leq 2.7\ V$, $I_{OH} = 2.5$ mA	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• STOP → RUN	—	5.0	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 3.0 V					2
	• 25 °C	—	6.17	7.1	mA	
	• -40 °C	—	6.39	6.7	mA	
	• 105 °C	—	6.93	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 3.0 V					2
	• 25 °C	—	8.24	10.4	mA	
	• -40 °C	—	8.26	9.8	mA	
	• 105 °C	—	9.00	11.5	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power					2
	• 25 °C	—	3.95	4.65	mA	
	• -40 °C	—		4.4	mA	
	• 105 °C	—		6	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power)					2, 3
	• 25 °C	—	3.81	4.4	mA	
	• -40 °C	—		4.2	mA	
	• 105 °C	—		5.8	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled					4
	• 25 °C	—	248.8	500	µA	
	• -40 °C	—	245.30	470	µA	
	• 105 °C	—	535.40	1800	µA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled					5
	• 25 °C	—	343.4	530	µA	
	• -40 °C	—	336.62	500	µA	
	• 105 °C	—	626.18	2000	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled					6
	• 25 °C	—	162	350	µA	
	• -40 °C	—	158.50	330	µA	
	• 105 °C	—	446.94	1700	µA	
I_{DD_STOP}	Stop mode current at 3.0 V					
	• 25 °C	—	311.90	730	µA	
	• -40 °C	—	364	700	µA	
	• 105 °C	—	645.13	2250	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• 25 °C	—	8.56	46	µA	
	• -40 °C	—		44	µA	
	• 105 °C	—		1500	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• 25 °C	—	1.98	3.5	µA	
	• -40 °C	—		3.3	µA	
	• 105 °C	—		85	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• 25 °C	—	1.24	2.6	µA	
	• -40 °C	—		2.5	µA	
	• 105 °C	—		59.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• 25 °C	—	0.89	1.7	µA	
	• -40 °C	—		1.6	µA	
	• 105 °C	—		38.8	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• 25 °C	—	0.35	0.67	µA	
	• -40 °C	—		0.64	µA	
	• 105 °C	—		38	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• 25 °C	—	0.472	0.76	µA	
	• -40 °C	—		0.72	µA	
	• 105 °C	—		38.4	µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF					
	• 25 °C	—	0.3	1	µA	
	• -40 °C	—		0.95	µA	
	• 105 °C	—		15	µA	

Table continues on the next page...

6.1 Core modules

6.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1
after clock edge, tDVO	Data valid Time	32	ns	1
tHO	Data Valid Hold	0	ns	1

1. Input transition assumed =1 ns. Output transition assumed = 50 pf.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, tSUI	Data setup time	4.7	ns	
inputs,tHI	Data hold time	0	ns	
after clock edge, tDVO	Data valid Time	49.4	ns	2
tHO	Data Valid Hold	0	ns	

1. Frequency of SWD clock (18 Mhz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

6.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to the XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1

1. Input Transition: 1ns. Output Load: 50 pf.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports)

Table 15. AFE switching characteristics (2.7V-3.6V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	36	ns	
inputs,tHI	Data hold time	0	ns	

AFE switching characteristics at (1.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, tSUI	Data setup time	5.1	ns	
inputs,tHI	Data hold time	0	ns	

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports)

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	54	ns	
inputs,tHI	Data hold time	0	ns	

6.2 Clock modules

6.2.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	

Table continues on the next page...

6.2.3.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2 , 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3 Memories and memory interfaces

6.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1

Table continues on the next page...

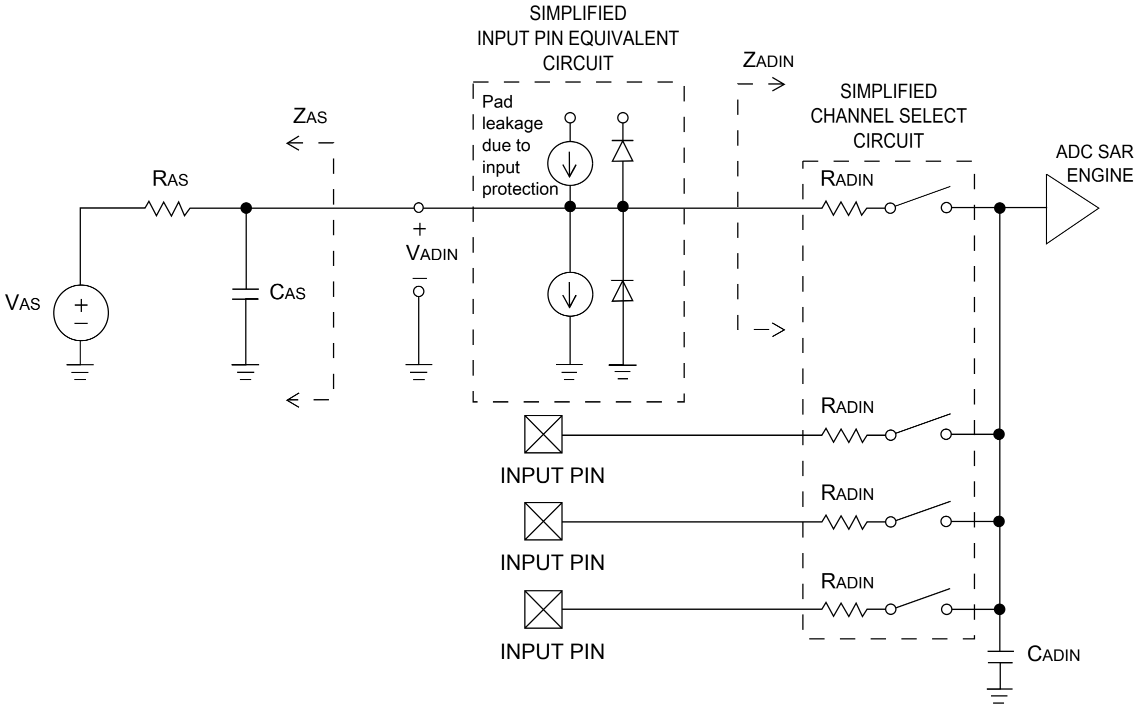


Figure 2. ADC input impedance equivalency diagram

6.4.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

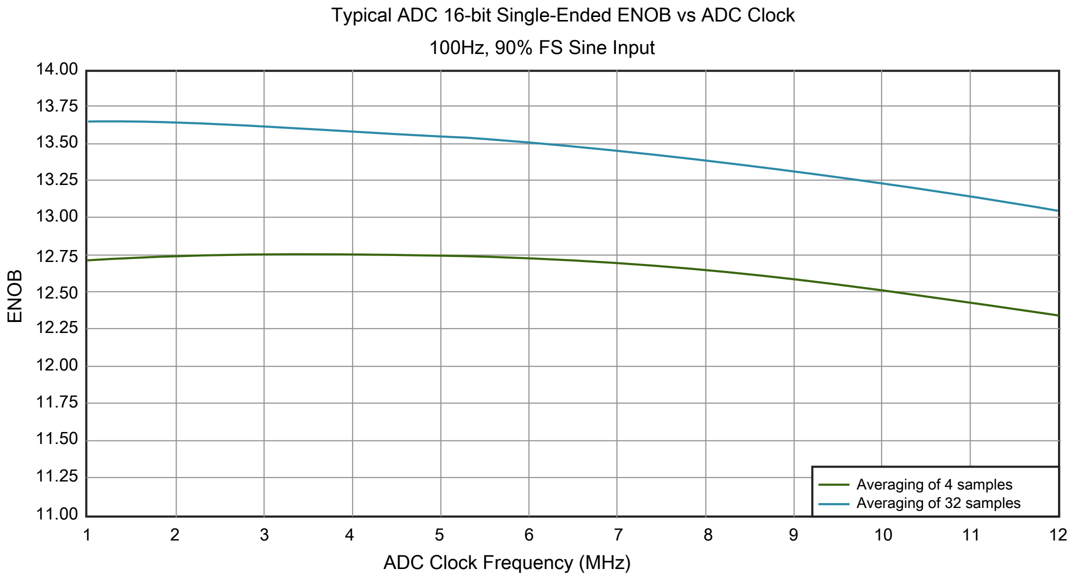


Figure 3. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.4.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1] • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	— — — —	5 10 20 30	— — — —	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

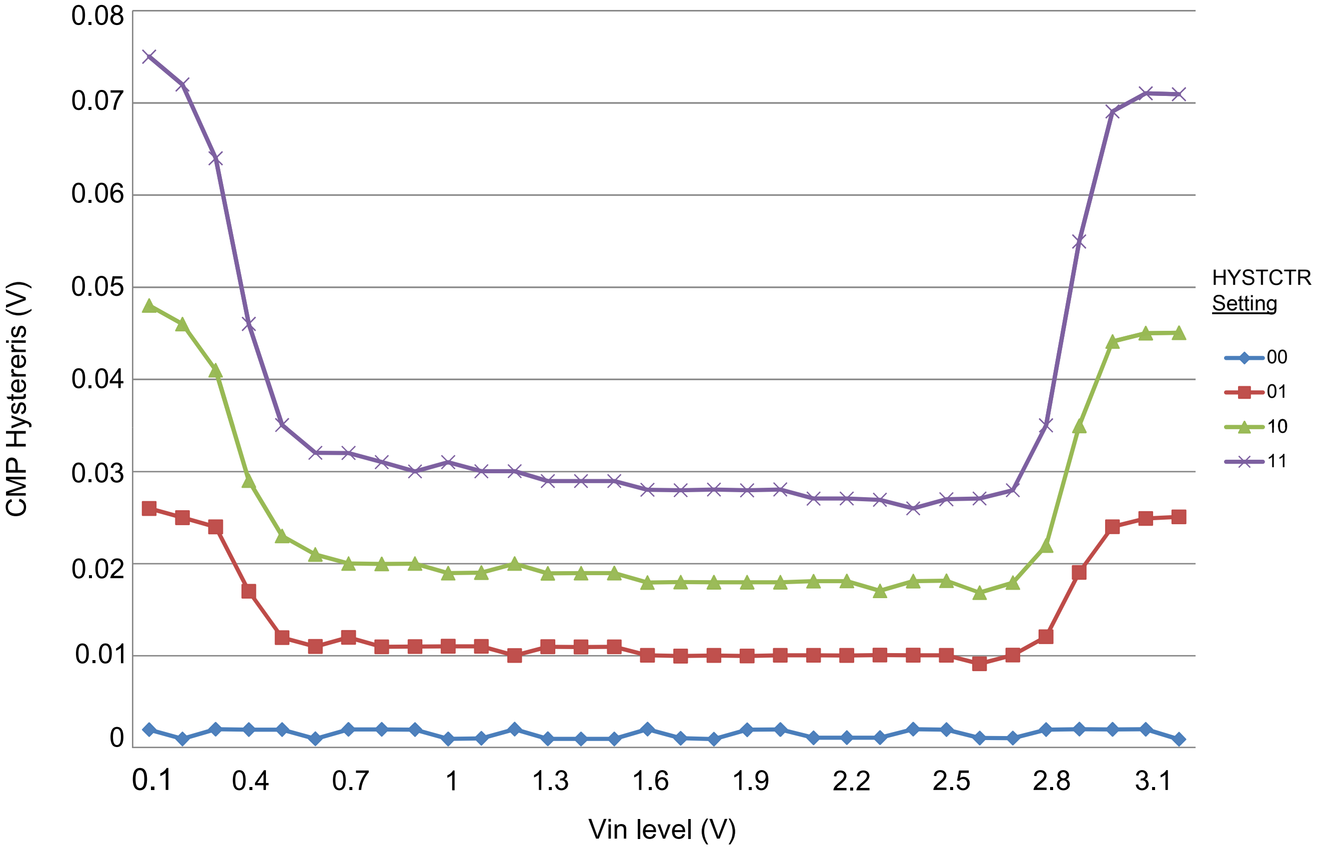


Figure 4. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

6.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides some reference values to be met on SoC.

Table 36. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	1
SCK frequency • Master • Slave	2	 12.5 12.5	 MHz Mhz	3
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	 25 3		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	 0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	 0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	 13 28		ns	
Rise time input • Master • Slave	 1 1		ns	
Fall time input • Master • Slave	 1 1		ns	
Rise time output • Master • Slave	 8.9 8.9		ns	
Fall time output • Master • Slave	 7.8 7.8		ns	

1. SPI modules will work on core clock.
2. F_{sys}/(Max Divider Value from registers)
3. F_{SYS}/2 in Master mode and F_{SYS}/4 in Slave mode. F_{SYS}/4 in Master as well as Slave Modes, where F_{SYS}=50Mhz

NOTE

The values assumed for input transition and output load are:
Input transition = 1 ns Output load = 50 pF

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	

Table continues on the next page...

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	15	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	3	—	µA	
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

NOTE

- For devices other than MKMx4, the SDADP3 and SDADM3 functions on the corresponding pins are disabled.
- All input pins including TAMPER pins must be pulled up or down to avoid extra power consumption.

8.2 KM Signal Multiplexing and Pin Assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	Disabled	LCD23	PTA0						
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	PXBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	PXBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						
18	10	—	Disabled	LCD38	PTB7	AFE_CLK					
19	11	—	Disabled	LCD39	PTC0	SCI3_RTS	PXBAR_IN1				
20	12	—	Disabled	LCD40/ CMP1P1	PTC1	SCI3_CTS					
21	13	—	Disabled	LCD41	PTC2	SCI3_TxD	PXBAR_OUT1				
22	14	—	Disabled	LCD42/ CMP0P3	PTC3	SCI3_RxD	LLWU_P13				
23	—	—	Disabled	LCD43	PTC4						
24	15	7	VBAT	VBAT							
25	16	8	XTAL32K	XTAL32K							
26	17	9	EXTAL32K	EXTAL32K							
27	18	10	VSS	VSS							
28	18	10	TAMPER2	TAMPER2							
29	18	10	TAMPER1	TAMPER1							
30	19	11	WKUP	TAMPER0							

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
68	41	34	Disabled	LCD0/ AD8	PTF1	QT0	PXBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTIM1	SCI0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTIM0	SCI0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL				
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	QT2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	QT1	LPTIM2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTIM0				
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTIM1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTIM2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	SCI1_CTS	SPI1_SS_B	PXBAR_IN7			
90	—	42	Disabled		PTH7	SCI1_RTS	SPI1_SCK	PXBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	SCI1_RxD	PXBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	SCI1_TxD	PXBAR_OUT8	SPI1_MOSI	SPI1_MISO		
93	57	—	Disabled	LCD21	PTI2						
94	58	—	Disabled	LCD22	PTI3						
95	59	—	VSS	VSS							
96	60	—	VLL3	VLL3							
97	61	—	VLL2	VLL2							
98	62	—	VLL1	VLL1							
99	63	—	VCAP2	VCAP2							
100	64	—	VCAP1	VCAP1							

8.3 KM Family Pinouts