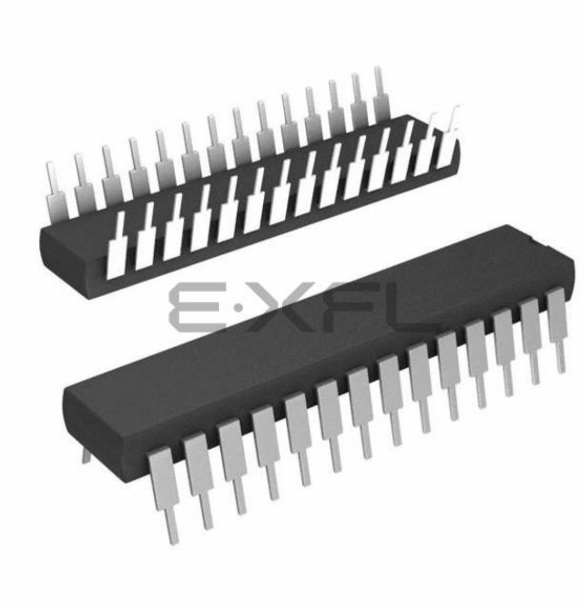

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08km102-e-sp

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F Pin Number 20-Pin PDIP/SSOP/SOIC	F Pin Number 28-Pin PDIP/SSOP/SOIC	F Pin Number 28-Pin QFN	F Pin Number 44-Pin QFN/TQFP	F Pin Number 48-Pin UQFN	FV Pin Number 20-Pin PDIP/SSOP/SOIC	FV Pin Number 28-Pin PDIP/SSOP/SOIC	FV Pin Number 28-Pin QFN	FV Pin Number 44-Pin QFN/TQFP	FV Pin Number 48-Pin UQFN	I/O	Buffer	Description
CN13	16	24	21	11	12	16	24	21	11	12	I	ST	Interrupt-on-Change Inputs
CN14	15	23	20	10	11	15	23	20	10	11	I	ST	Interrupt-on-Change Inputs
CN15	—	22	19	9	10	—	22	19	9	10	I	ST	Interrupt-on-Change Inputs
CN16	—	21	18	8	9	—	21	18	8	9	I	ST	Interrupt-on-Change Inputs
CN17	—	—	—	3	3	—	—	—	3	3	I	ST	Interrupt-on-Change Inputs
CN18	—	—	—	2	2	—	—	—	2	2	I	ST	Interrupt-on-Change Inputs
CN19	—	—	—	5	5	—	—	—	5	5	I	ST	Interrupt-on-Change Inputs
CN20	—	—	—	4	4	—	—	—	4	4	I	ST	Interrupt-on-Change Inputs
CN21	13	18	15	1	1	13	18	15	1	1	I	ST	Interrupt-on-Change Inputs
CN22	12	17	14	44	48	12	17	14	44	48	I	ST	Interrupt-on-Change Inputs
CN23	11	16	13	43	47	11	16	13	43	47	I	ST	Interrupt-on-Change Inputs
CN24	—	15	12	42	46	—	15	12	42	46	I	ST	Interrupt-on-Change Inputs
CN25	—	—	—	37	40	—	—	—	37	40	I	ST	Interrupt-on-Change Inputs
CN26	—	—	—	38	41	—	—	—	38	41	I	ST	Interrupt-on-Change Inputs
CN27	—	14	11	41	45	—	14	11	41	45	I	ST	Interrupt-on-Change Inputs
CN28	—	—	—	36	39	—	—	—	36	39	I	ST	Interrupt-on-Change Inputs
CN29	8	10	7	31	34	8	10	7	31	34	I	ST	Interrupt-on-Change Inputs
CN30	7	9	6	30	33	7	9	6	30	33	I	ST	Interrupt-on-Change Inputs
CN31	—	—	—	26	28	—	—	—	26	28	I	ST	Interrupt-on-Change Inputs
CN32	—	—	—	25	27	—	—	—	25	27	I	ST	Interrupt-on-Change Inputs
CN33	—	—	—	32	35	—	—	—	32	35	I	ST	Interrupt-on-Change Inputs
CN34	—	—	—	35	38	—	—	—	35	38	I	ST	Interrupt-on-Change Inputs
CN35	—	—	—	12	13	—	—	—	12	13	I	ST	Interrupt-on-Change Inputs
CN36	—	—	—	13	14	—	—	—	13	14	I	ST	Interrupt-on-Change Inputs
CTCMP	4	4	1	21	23	4	4	1	21	23	I	ANA	CTMU Comparator Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
$\overline{MCLR}$	1	1	26	18	19	1	1	26	18	19	I	ST	Master Clear (Device Reset) Input (active-low)
OA1INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 1 Input A
OA1INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 1 Input B
OA1INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 1 Input C
OA1IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 1 Input D
OA1OUT	—	7	4	24	26	—	7	4	24	26	O	ANA	Op Amp 1 Analog Output
OA2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 2 Input A
OA2INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 2 Input B
OA2INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 2 Input C
OA2IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 2 Input D
OA2OUT	—	26	23	15	16	—	26	23	15	16	O	ANA	Op Amp 2 Analog Output
OC1A	14	20	17	7	7	11	16	13	43	47	O	—	MCCP1 Output Compare A
OC1B	12	17	14	44	48	12	17	14	44	48	O	—	MCCP1 Output Compare B
OC1C	15	21	18	8	9	15	21	18	8	9	O	—	MCCP1 Output Compare C
OC1D	16	24	21	11	12	16	24	21	11	12	O	—	MCCP1 Output Compare D
OC1E	—	14	11	41	45	—	14	11	41	45	O	—	MCCP1 Output Compare E
OC1F	—	15	12	42	46	—	15	12	42	46	O	—	MCCP1 Output Compare F
OC2A	4	22	19	9	10	4	22	19	9	10	O	—	MCCP2 Output Compare A
OC2B	—	23	20	10	11	—	23	20	10	11	O	—	MCCP2 Output Compare B
OC2C	—	—	—	2	2	—	—	—	2	2	O	—	MCCP2 Output Compare C
OC2D	—	—	—	3	3	—	—	—	3	3	O	—	MCCP2 Output Compare D
OC2E	—	—	—	4	4	—	—	—	4	4	O	—	MCCP2 Output Compare E
OC2F	—	—	—	5	5	—	—	—	5	5	O	—	MCCP2 Output Compare F
OC3A	—	21	18	12	13	—	21	18	12	13	O	—	MCCP3 Output Compare A
OC3B	—	24	21	13	14	—	24	21	13	14	O	—	MCCP3 Output Compare B
OC4	—	18	15	1	1	—	18	15	1	1	O	—	SCCP4 Output Compare
OC5	—	19	16	6	6	—	19	16	6	6	O	—	SCCP5 Output Compare
OCFA	17	25	22	14	15	17	25	22	14	15	I	ST	MCCP/SCCP Output Compare Fault Input A
OCFB	16	24	21	32	35	16	24	21	32	35	I	ST	MCCP/SCCP Output Compare Fault Input B

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

NOTES:

4.0 MEMORY ORGANIZATION

As with Harvard architecture devices, the PIC24F microcontrollers feature separate program and data memory space and busing. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

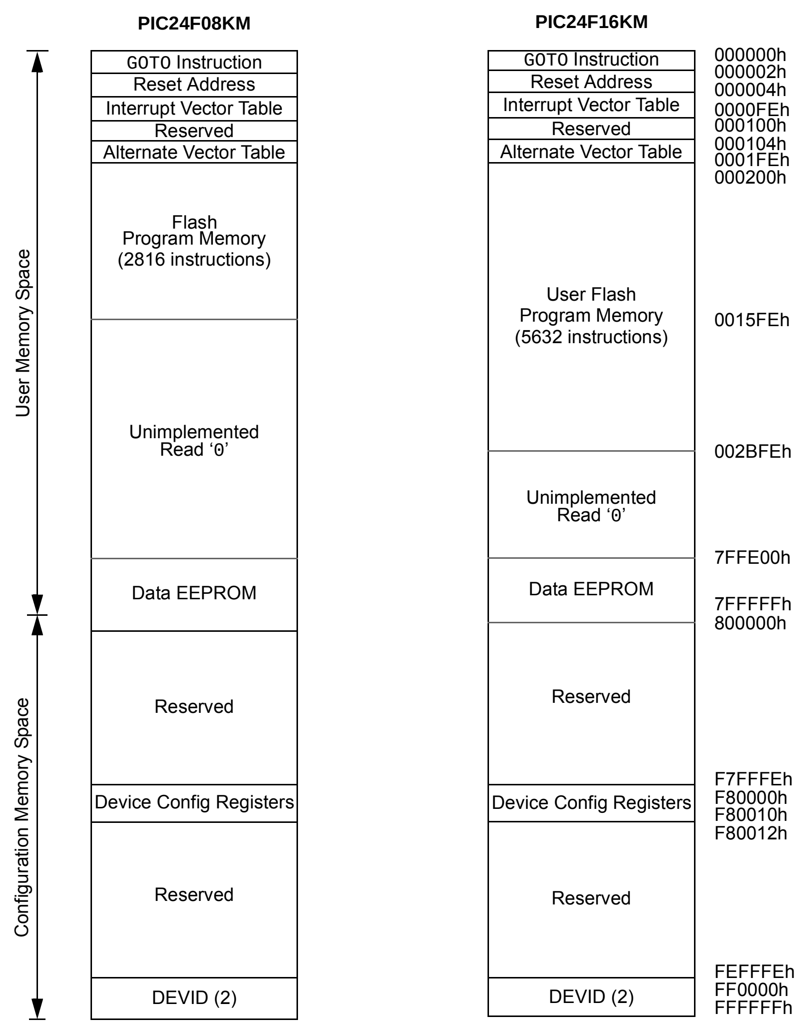
4.1 Program Address Space

The program address memory space of the PIC24F devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from a table operation or Data Space remapping, as described in **Section 4.3 "Interfacing Program and Data Memory Spaces"**.

The user access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FV16KM204 family of devices are displayed in Figure 4-1.

FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES



Note: Memory areas are not displayed to scale.

REGISTER 8-17: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **ULPWUIE:** Ultra Low-Power Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-18: IEC6: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CLC2IE	CLC1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **CLC2IE:** Configurable Logic Cell 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **CLC1IE:** Configurable Logic Cell 1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

10.5 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption. Meanwhile, the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

10.6 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, “XXXEN”, located in the module’s main control SFR.
- The Peripheral Module Disable (PMD) bit, generically named, “XXXMD”, located in one of the PMDx Control registers.

Both bits have similar functions in enabling or disabling its associated module. Setting the PMDx bits for a module, disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect, and read values will be invalid. Many peripheral modules have a corresponding PMDx bit.

In contrast, disabling a module by clearing its XXXEN bit, disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as when the PMDx bits are used. Most peripheral modules have an enable bit; exceptions include capture, compare and RTCC.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, “XXXIDL”. By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

13.3 Output Compare Mode

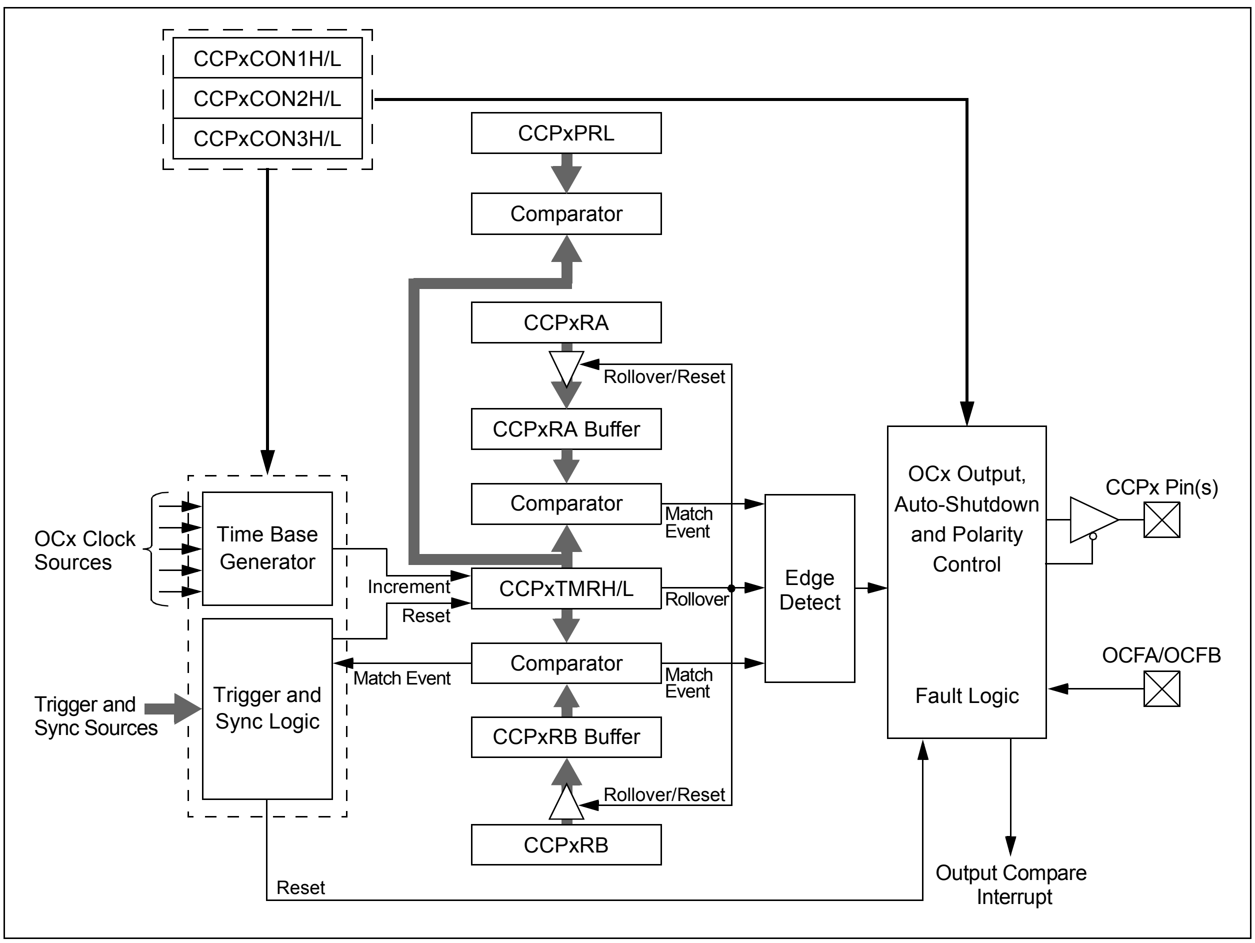
Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The Output Compare x module on compare match events has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the Output Compare x module can also generate interrupts on a compare match event.

Table 13-3 shows the various modes available in Output Compare modes.

TABLE 13-3: OUTPUT COMPARE/PWM MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode	
`0001`	`0`	Output High on Compare (16-bit)	Single Edge Mode
`0001`	`1`	Output High on Compare (32-bit)	
`0010`	`0`	Output Low on Compare (16-bit)	
`0010`	`1`	Output Low on Compare (32-bit)	
`0011`	`0`	Output Toggle on Compare (16-bit)	
`0011`	`1`	Output Toggle on Compare (32-bit)	
`0100`	`0`	Dual Edge Compare (16-bit)	Dual Edge Mode
`0101`	`0`	Dual Edge Compare (16-bit buffered)	PWM Mode
`0110`	`0`	Center-Aligned Pulse (16-bit buffered)	Center PWM
`0111`	`0`	Variable Frequency Pulse (16-bit)	
`0111`	`1`	Variable Frequency Pulse (32-bit)	

FIGURE 13-5: OUTPUT COMPARE x BLOCK DIAGRAM



18.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

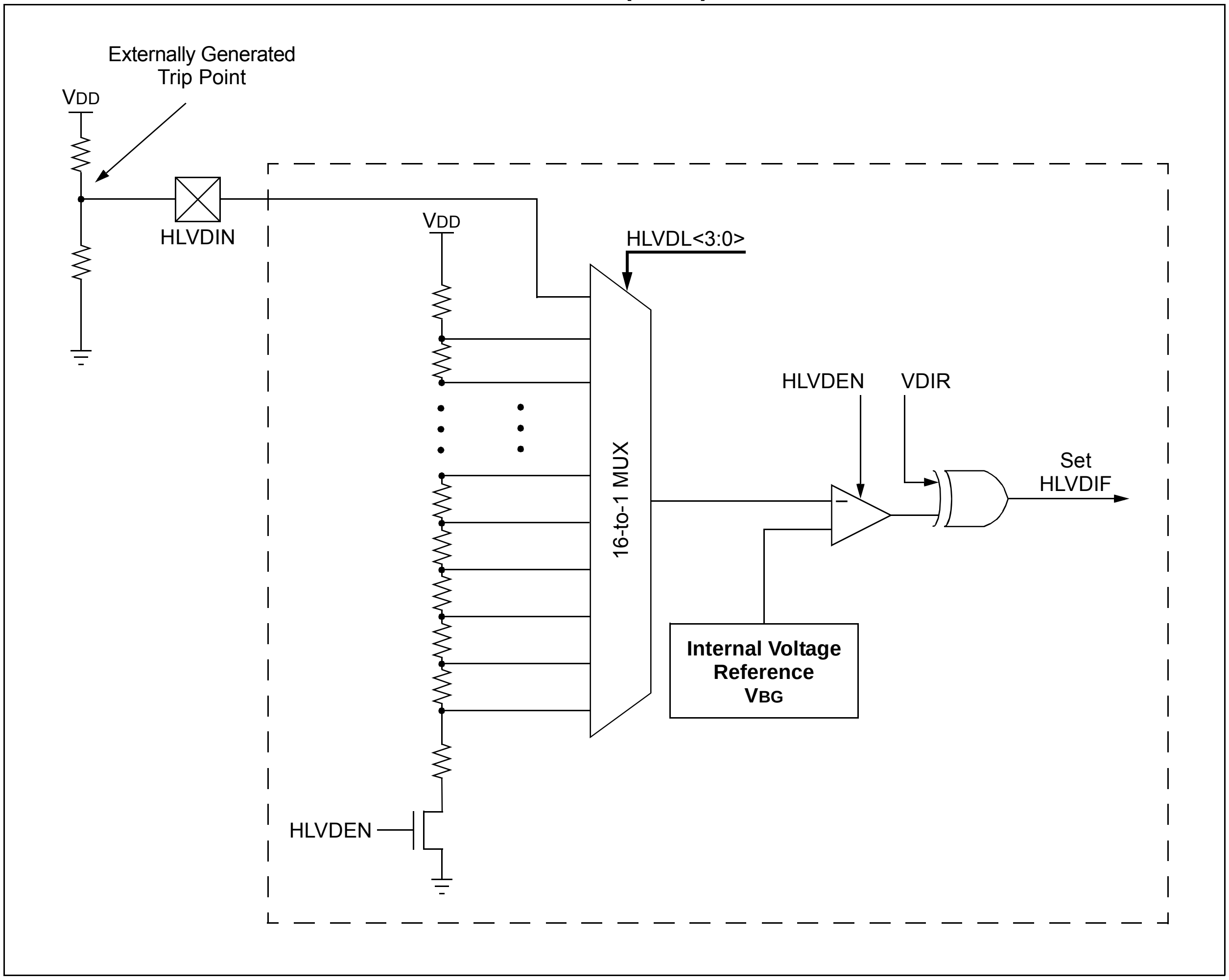
Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the *"PIC24F Family Reference Manual"*, **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725).

The High/Low-Voltage Detect module (HLVD) is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 18-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 18-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



REGISTER 19-8: AD1CSSH: A/D INPUT SCAN SELECT REGISTER (HIGH WORD)(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS23	CSS22	CSS21	CSS20(2)	CSS19(2)	CSS18	CSS17	CSS16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-10 **CSS<30:26>:** A/D Input Scan Selection bits
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CSS<23:16>:** A/D Input Scan Selection bits(2)
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.
2: The CSS<20:19> bits are not implemented in 20-pin devices.

REGISTER 19-9: AD1CSSL: A/D INPUT SCAN SELECT REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(2,3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7(2,3)	CSS6(2,3)	CSS5(2)	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CSS<15:0>:** A/D Input Scan Selection bits(2,3)
1 = Includes the corresponding ANx input for scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.
2: The CSS<8:5> bits are not implemented in 20-pin devices.
3: The CSS<8:6> bits are not implemented in 28-pin devices.

21.0 DUAL OPERATIONAL AMPLIFIER MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **"Operational Amplifier (Op Amp)"** (DS30505). Device-specific information in this data sheet supersedes the information in the *"PIC24F Family Reference Manual"*.

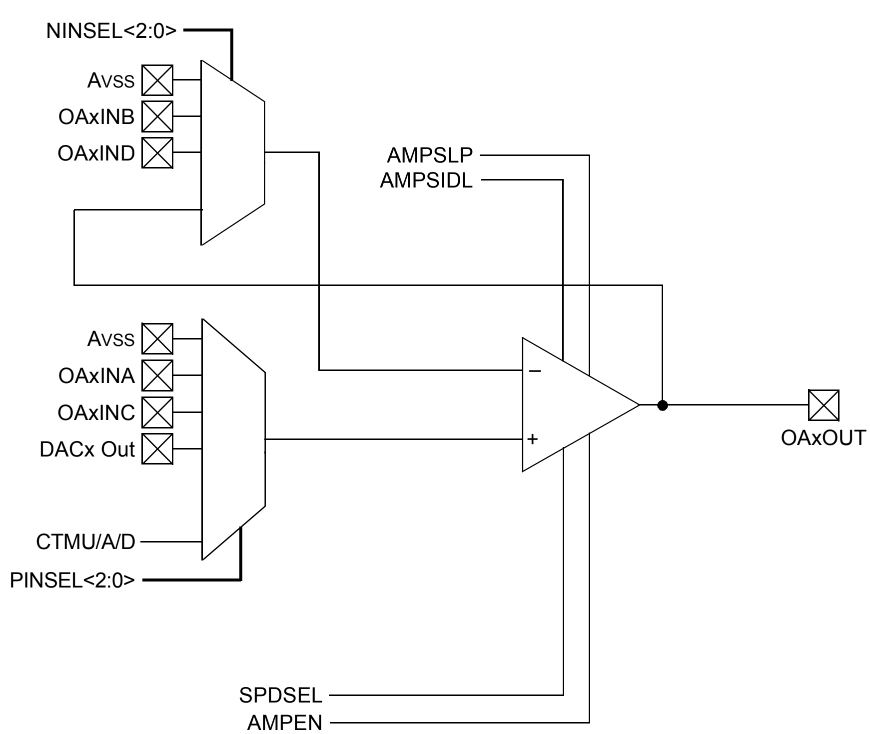
PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal unity-gain buffer option
- Multiple input options each on the inverting and non-inverting amplifier inputs
- Rail-to-rail input and output capabilities
- User-selectable option for regular or low-power operation
- User-selectable operation in Idle and Sleep modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 "Configuring Analog Port Pins"** for more information.

FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM



REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator x Channel Select bits
11 = Inverting input of the comparator connects to BGBUF1(1)
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

Note 1: BGBUF1 voltage is configured by BUFREF1<1:0> (BUFCON0<1:0>).
2: If the EVPOL<1:0> bits are set to a value other than '00', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

REGISTER 22-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	C3EVT(1)	C2EVT(1)	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
—	—	—	—	—	C3OUT(1)	C2OUT(1)	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Comparator x Stop in Idle Mode bit
1 = Comparator interrupts are disabled in Idle mode; enabled comparators remain operational
0 = Continues operation of all enabled comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit (read-only)(1)
Shows the current event status of Comparator 3 (CM3CON<9>).

bit 9 **C2EVT:** Comparator 2 Event Status bit (read-only)(1)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 8 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit (read-only)(1)
Shows the current output of Comparator 3 (CM3CON<8>).

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)(1)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

Note 1: Comparator 2 and Comparator 3 are only available on PIC24F(V)16KM2XX devices.

REGISTER 25-5: FWDT: WATCHDOG TIMER CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN1	WINDIS	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7,5 **FWDTEN<1:0>:** Watchdog Timer Enable bits
11 = WDT is enabled in hardware
10 = WDT is controlled with the SWDTEN bit setting
01 = WDT is enabled only while the device is active, WDT is disabled in Sleep; SWDTEN bit is disabled
00 = WDT is disabled in hardware; SWDTEN bit is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard WDT is selected; windowed WDT is disabled
0 = Windowed WDT is enabled; note that executing a CLRWDT instruction while the WDT is disabled in hardware and software (FWDTEN<1:0> = 00 and SWDTEN (RCON<5>) = 0) will not cause a device Reset

bit 4 **FWPSA:** WDT Prescaler bit
1 = WDT prescaler ratio of 1:128
0 = WDT prescaler ratio of 1:32

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscale Select bits
1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

27.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV16KM204 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV16KM204 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias...-40°C to +125°C
Storage temperature ....-65°C to +150°C
Voltage on VDD with respect to VSS (PIC24FXXKMXXX) ....-0.3V to +4.5V
Voltage on VDD with respect to VSS (PIC24FVXXKMXXX) ....-0.3V to +6.5V
Voltage on any combined analog and digital pin with respect to VSS ....-0.3V to (VDD + 0.3V)
Voltage on any digital only pin with respect to VSS ....-0.3V to (VDD + 0.3V)
Voltage on $\overline{MCLR}$/VPP pin with respect to VSS ....-0.3V to +9.0V
Maximum current out of VSS pin ....300 mA
Maximum current into VDD pin(1)...250 mA
Maximum output current sunk by any I/O pin...25 mA
Maximum output current sourced by any I/O pin ....25 mA
Maximum current sunk by all ports ....200 mA
Maximum current sourced by all ports(1)...200 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 27-1).

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 27-12: DC CHARACTERISTICS: DATA EEPROM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
		Data EEPROM Memory					
D140	EPD	Cell Endurance	100,000	—	—	E/W	
D141	VPRD	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D143A	TIWD	Self-Timed Write Cycle Time	—	4	—	ms	
D143B	TREF	Number of Total Write/Erase Cycles Before Refresh	—	10M	—	E/W	
D144	TRETDD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D145	IDDPD	Supply Current During Programming	—	7	—	mA	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

TABLE 27-13: DC CHARACTERISTICS: COMPARATOR

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D300	VIOFF	Input Offset Voltage	—	20	40	mV	
D301	VICM	Input Common-Mode Voltage	0	—	VDD	V	
D302	CMRR	Common-Mode Rejection Ratio	55	—	—	dB	

TABLE 27-14: DC CHARACTERISTICS: COMPARATOR VOLTAGE REFERENCE

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
VRD310	CVRES	Resolution	—	—	VDD/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	1	LSb	AVDD = 3.3V-5.5V
VRD312	CVRUR	Unit Resistor Value (R)	—	2k	—	Ω	

27.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FV16KM204 family AC characteristics and timing parameters.

TABLE 27-18: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 1.8V to 3.6V** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 27.1 "DC Characteristics"**.

FIGURE 27-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

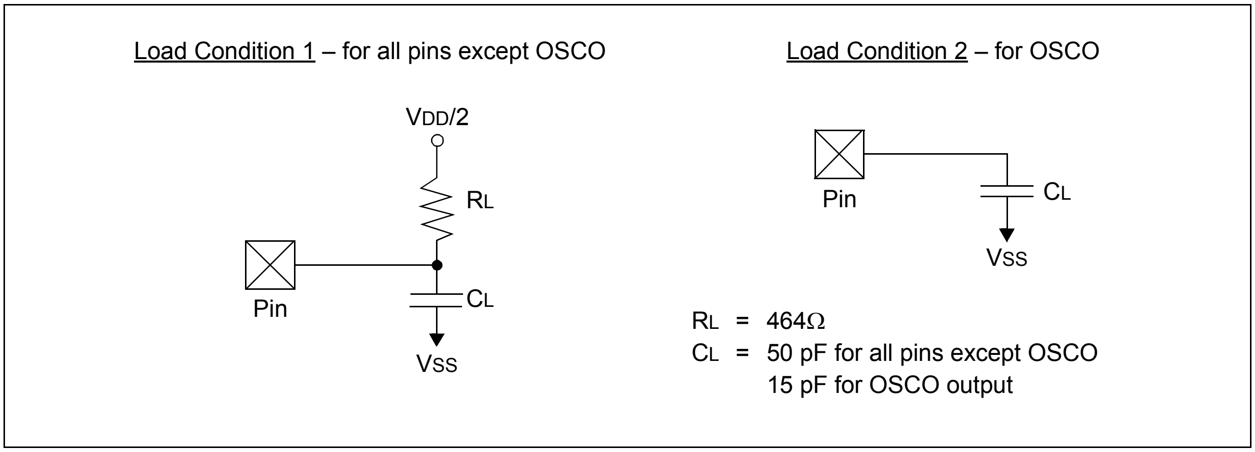


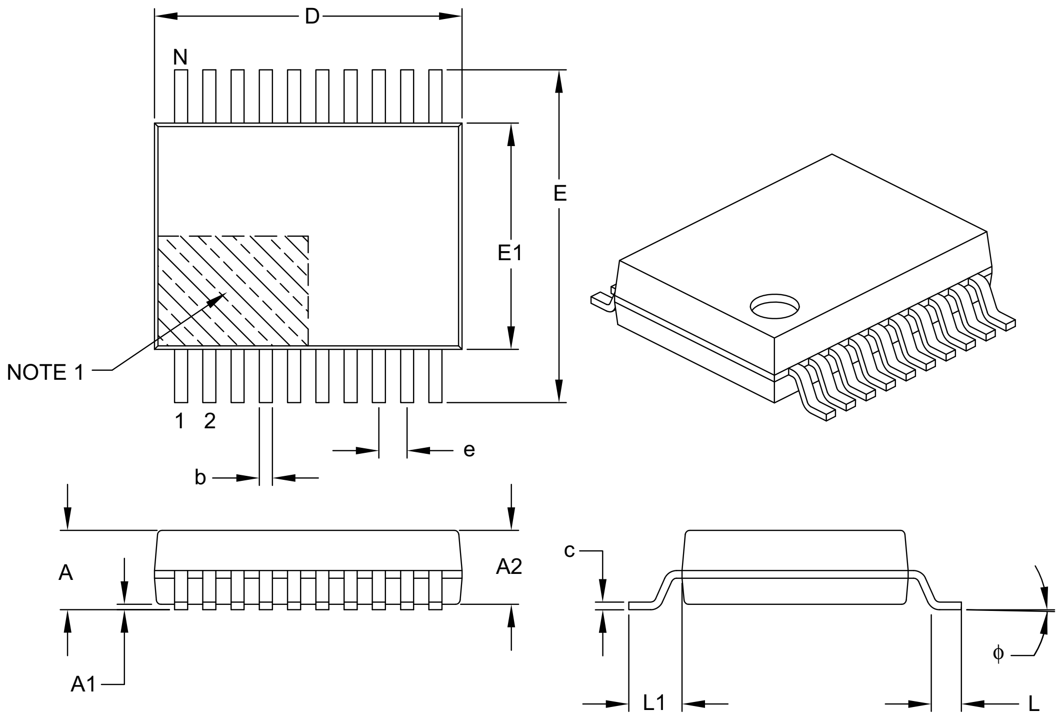
TABLE 27-19: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO50	COSC2	OSCO/CLKO Pin	—	—	15	pF	In XT and HS modes when External Clock is used to drive OSCI
DO56	CIO	All I/O Pins and OSCO	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I²C™ mode

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

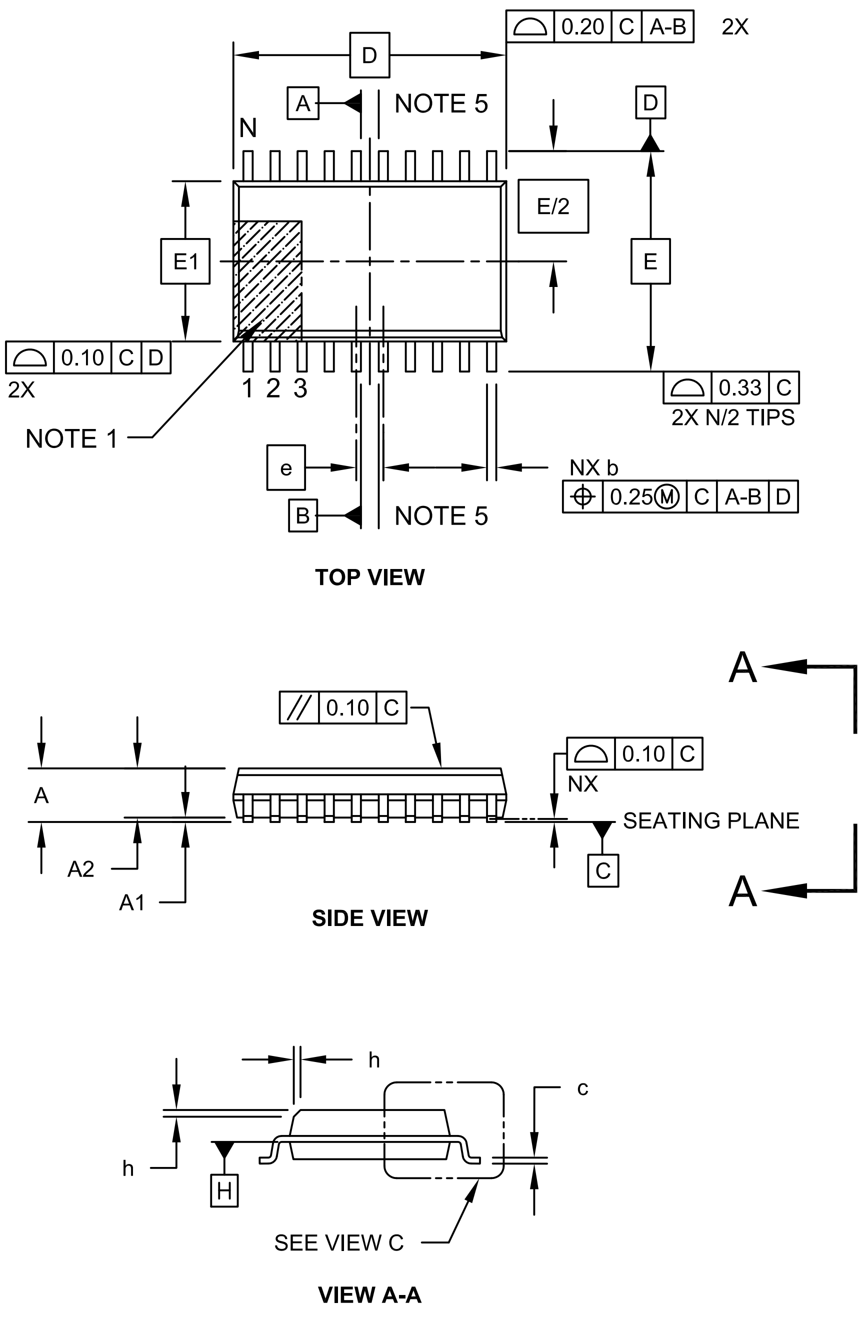
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

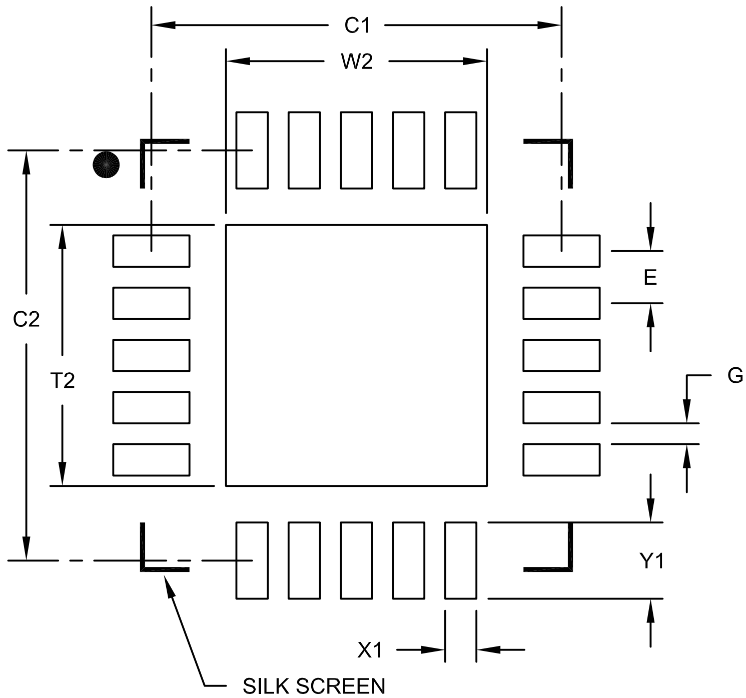
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-094C Sheet 1 of 2

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

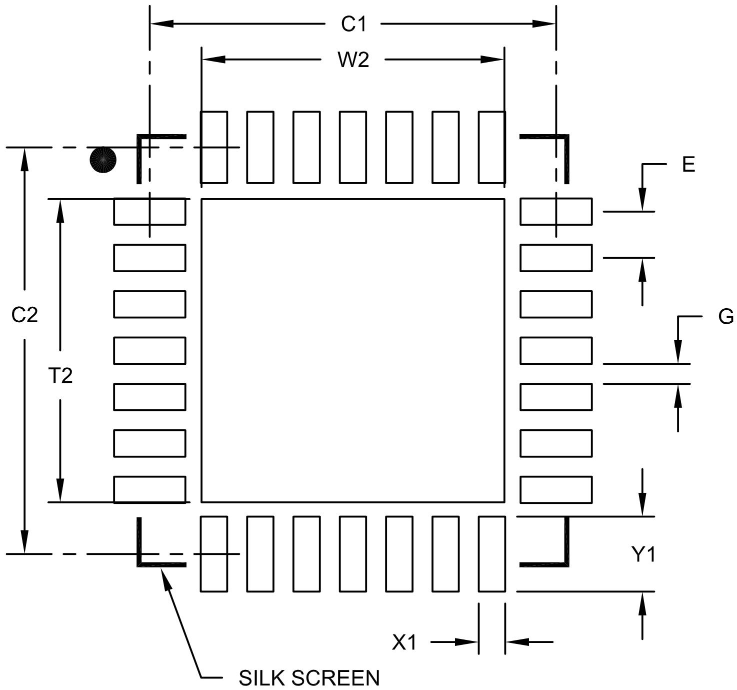
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A