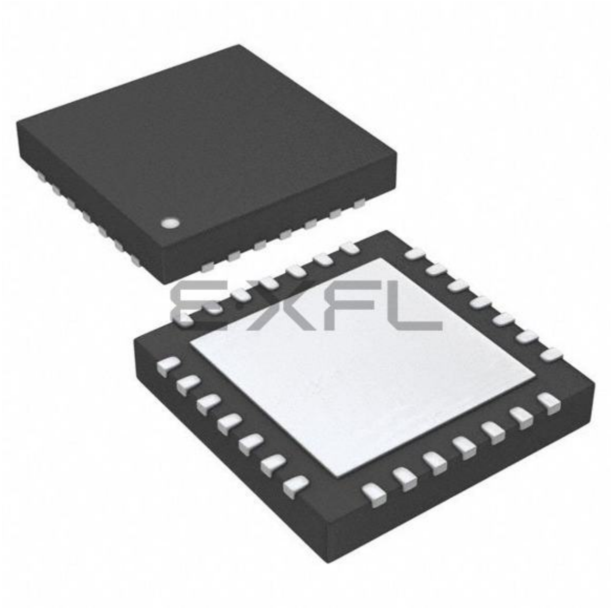

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08km102t-i-ml

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
OSCI	7	9	6	30	33	7	9	6	30	33	I	ANA	Primary Oscillator Input
OSCO	8	10	7	31	34	8	10	7	31	34	O	ANA	Primary Oscillator Output
PGEC1	5	5	2	22	24	5	5	2	22	24	I/O	ST	ICSP Clock 1
PGED1	4	4	1	21	23	4	4	1	21	23	I/O	ST	ICSP Data 1
PGEC2	2	22	19	9	10	2	22	19	9	10	I/O	ST	ICSP Clock 2
PGED2	3	21	18	8	9	3	21	18	8	9	I/O	ST	ICSP Data 2
PGEC3	10	15	12	42	46	10	15	12	42	46	I/O	ST	ICSP Clock 3
PGED3	9	14	11	41	45	9	14	11	41	45	I/O	ST	ICSP Data 3
PWRLCLK	10	12	9	34	37	10	12	9	34	37	I	ST	RTCC Power Line Clock Input
RA0	2	2	27	19	21	2	2	27	19	21	I/O	ST	PORTA Pins
RA1	3	3	28	20	22	3	3	28	20	22	I/O	ST	PORTA Pins
RA2	7	9	6	30	33	7	9	6	30	33	I/O	ST	PORTA Pins
RA3	8	10	7	31	34	8	10	7	31	34	I/O	ST	PORTA Pins
RA4	10	12	9	34	37	10	12	9	34	37	I/O	ST	PORTA Pins
RA5	1	1	26	18	19	1	1	26	18	19	I/O	ST	PORTA Pins
RA6	14	20	17	7	7	—	—	—	—	—	I/O	ST	PORTA Pins
RA7	—	19	16	6	6	—	19	16	6	6	I/O	ST	PORTA Pins
RA8	—	—	—	32	35	—	—	—	32	35	I/O	ST	PORTA Pins
RA9	—	—	—	35	38	—	—	—	35	38	I/O	ST	PORTA Pins
RA10	—	—	—	12	13	—	—	—	12	13	I/O	ST	PORTA Pins
RA11	—	—	—	13	14	—	—	—	13	14	I/O	ST	PORTA Pins
RB0	4	4	1	21	23	4	4	1	21	23	I/O	ST	PORTB Pins
RB1	5	5	2	22	24	5	5	2	22	24	I/O	ST	PORTB Pins
RB2	6	6	3	23	25	6	6	3	23	25	I/O	ST	PORTB Pins
RB3	—	7	4	24	26	—	7	4	24	26	I/O	ST	PORTB Pins
RB4	9	11	8	33	36	9	11	8	33	36	I/O	ST	PORTB Pins
RB5	—	14	11	41	45	—	14	11	41	45	I/O	ST	PORTB Pins
RB6	—	15	12	42	46	—	15	12	42	46	I/O	ST	PORTB Pins
RB7	11	16	13	43	47	11	16	13	43	47	I/O	ST	PORTB Pins
RB8	12	17	14	44	48	12	17	14	44	48	I/O	ST	PORTB Pins

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

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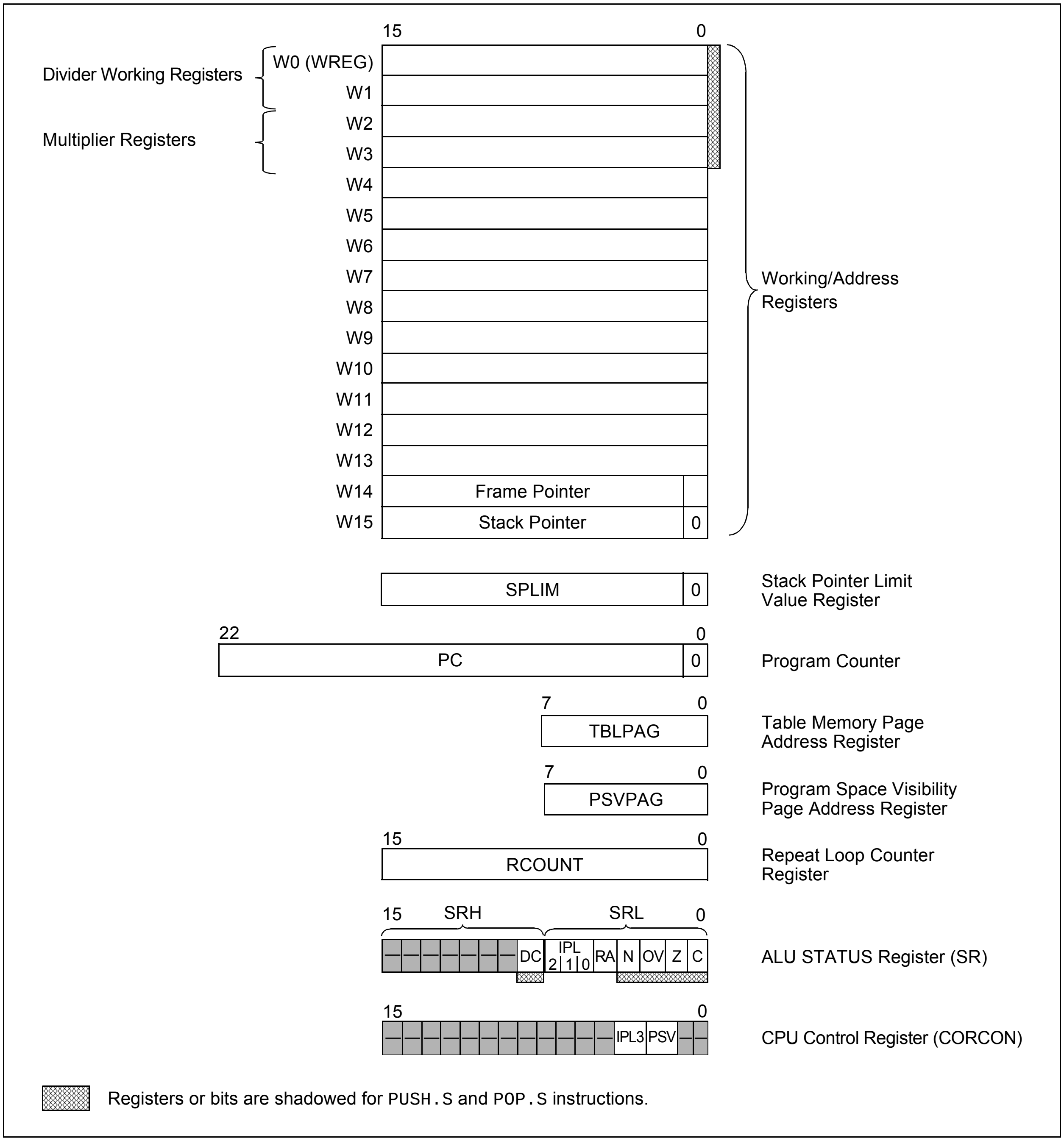
FIGURE 3-2: PROGRAMMER'S MODEL



6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
/*------------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the erase
-------------------------------------------------------------------------------------------------
*/
    unsigned int offset;

    // Set up NVMCON to erase one word of data EEPROM
    NVMCON = 0x4058;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);             // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);           // Initizlize lower word of address
    __builtin_tblwtl(offset, 0);                     // Write EEPROM data to write latch

    asm volatile ("disi #5");                        // Disable Interrupts For 5 Instructions
    __builtin_write_NVM();                           // Issue Unlock Sequence & Start Write Cycle
    while(NVMCONbits.WR=1);                          // Optional: Poll WR bit to wait for
                                                     // write sequence to complete
```

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REGISTER 7-1: RCON: RESET CONTROL REGISTER[1] (CONTINUED)

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
2: If the FWDTEN<1:0> Configuration bits are ‘11’ (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.
3: This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	R/W-0, HS
NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	CCT2IF
bit 15							bit 8

R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
CCT1IF	CCP4IF	CCP3IF	—	T1IF	CCP2IF	CCP1IF	INT0IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NVMIF:** NVM Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **AD1IF:** A/D Conversion Complete Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **U1TXIF:** UART1 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **U1RXIF:** UART1 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **CCT2IF:** Capture/Compare 2 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CCT1IF:** Capture/Compare 1 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **CCP4IF:** Capture/Compare 4 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **CCP3IF:** Capture/Compare 3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CCP2IF:** Capture/Compare 2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **CCP1IF:** Capture/Compare 1 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 8-32: IPC19: INTERRUPT PRIORITY CONTROL REGISTER 19

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	DAC2IP2	DAC2IP1	DAC2IP0	—	DAC1IP2	DAC1IP1	DAC1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **DAC2IP<2:0>:** Digital-to-Analog Converter 2 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **DAC1IP<2:0>:** Digital-to-Analog Converter 1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CTMUIP<2:0>:** CTMU Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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11.2.2 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation, and a read operation of the same port. Typically, this instruction would be a NOP.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC24FXXXXX family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 37 external signals (CN0 through CN36) that may be selected (enabled) for generating an interrupt request on a Change-of-State.

There are six control registers associated with the CN module. The CNEN1 and CNEN3 registers contain the interrupt enable control bits for each of the CNx input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CNx pin also has a weak pull-up/pull-down connected to it. The pull-ups act as a current source that is connected to the pin. The pull-downs act as a current sink to eliminate the need for external resistors when push button or keypad devices are connected.

On any pin, only the pull-up resistor or the pull-down resistor should be enabled, but not both of them. If the push button or the keypad is connected to V_{DD}, enable the pull-down, or if they are connected to V_{SS}, enable the pull-up resistors. The pull-ups are enabled separately using the CNPU1 and CNPU3 registers, which contain the control bits for each of the CNx pins.

Setting any of the control bits enables the weak pull-ups for the corresponding pins. The pull-downs are enabled separately using the CNPD1 and CNPD3 registers, which contain the control bits for each of the CNx pins. Setting any of the control bits enables the weak pull-downs for the corresponding pins.

When the internal pull-up is selected, the pin uses V_{DD} as the pull-up source voltage. When the internal pull-down is selected, the pins are pulled down to V_{SS} by an internal resistor. Make sure that there is no external pull-up source/pull-down sink when the internal pull-ups/pull-downs are enabled.

Note:	Pull-ups and pull-downs on Change Notification (CN) pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0;          //Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
MOV   W0, TRISB;
NOP;                       //Delay 1 cycle
BTSS  PORTB, #13;          //Next Instruction

Equivalent ‘C’ Code
TRISB = 0xFF00;            //Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
NOP();                     //Delay 1 cycle
if(PORTBbits.RB13 == 1)    // execute following code if PORTB pin 13 is set.
{
}
```


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REGISTER 13-1: CCPxCON1L: CCPx CONTROL 1 LOW REGISTERS

R/W-0	U-0	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2(1)	CLKSEL1(1)	CLKSEL0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CCPON:** CCPx Module Enable bit
1 = Module is enabled with an operating mode specified by the MOD<3:0> control bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CCPSIDL:** CCPx Stop in Idle Mode Bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Reserved:** Maintain as ‘0’

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Asynchronous module time base clock is selected and synchronized to the internal system clocks (CLKSEL<2:0> ≠ 000)
0 = Synchronous module time base clock is selected and does not require synchronization (CLKSEL<2:0> = 000)

bit 10-8 **CLKSEL<2:0>:** CCPx Time Base Clock Select bits(1)
111 = External TCLKIA input
110 = External TCLKIB input
101 = CLC1
100 = Reserved
011 = LPRC (31 kHz source)
010 = Secondary Oscillator
001 = Reserved
000 = System clock (T_{CY})

bit 7-6 **TMRPS<1:0>:** Time Base Prescale Select bits
11 = 1:64 Prescaler
10 = 1:16 Prescaler
01 = 1:4 Prescaler
00 = 1:1 Prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = Uses 32-bit time base for timer, single edge output compare or input capture function
0 = Uses 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture peripheral
0 = Output Compare/PWM/Timer peripheral (exact function is selected by the MOD<3:0> bits)

Note 1: Clock options are limited in some operating modes. See Table 13-1 for restrictions.

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REGISTER 13-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS (1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT5	DT4	DT3	DT2	DT1	DT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DT<5:0>:** CCPx Dead-Time Select bits

111111 = Insert 63 dead-time delay periods between complementary output signals
111110 = Insert 62 dead-time delay periods between complementary output signals
. . .
000010 = Insert 2 dead-time delay periods between complementary output signals
000001 = Insert 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in MCCPx modules only.

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15.2 Transmitting in 8-Bit Data Mode

1. Set up the UARTx:
   a) Write the appropriate values for data, parity and Stop bits.
   b) Write the appropriate baud rate value to the UxBRG register.
   c) Set up transmit and receive interrupt enable and priority bits.
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write the data byte to the lower byte of the UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternately, the data byte may be transferred while UTXEN = `0`, and then, the user may set UTXEN. This will cause the serial bit stream to begin immediately, because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bit, UTXISELx.

15.3 Transmitting in 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 15.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write UxTXREG as a 16-bit value only.
5. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
6. A transmit interrupt will be generated as per the setting of control bit, UTXISELx.

15.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header, made up of a Break, followed by an Auto-Baud Sync byte.

1. Configure the UARTx for the desired mode.
2. Set UTXEN and UTXBRK – this sets up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write '55h' to UxTXREG – loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

15.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 15.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. A receive interrupt will be generated when one or more data characters have been received, as per interrupt control bit, URXISELx.
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

15.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-To-Send ($\overline{\text{UxCTS}}$) and Request-To-Send ($\overline{\text{UxRTS}}$) are the two hardware controlled pins that are associated with the UARTx module. These two pins allow the UARTx to operate in Simplex and Flow Control modes. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN<1:0> bits in the UxMODE register configure these pins.

15.7 Infrared Support

The UARTx module provides two types of infrared UARTx support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder.

As the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE<3>) is '`0`'.

15.7.1 EXTERNAL IrDA SUPPORT – IrDA CLOCK OUTPUT

To support external IrDA encoder and decoder devices, the UxBCLK pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. When UEN<1:0> = `11`, the UxBCLK pin will output the 16x baud clock if the UARTx module is enabled; it can be used to support the IrDA codec chip.

15.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE<12>). When enabled (IREN = `1`), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

To perform an A/D conversion:

1. Configure the A/D module:
    a) Configure the port pins as analog inputs and/or select band gap reference inputs (ANSx registers).
    b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2<15:13>).
    c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
    d) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
    e) Configure the MODE12 bit to select A/D resolution (AD1CON1<10>).
    f) Select how conversion results are presented in the buffer (AD1CON1<9:8>).
    g) Select the interrupt rate (AD1CON2<6:2>).
    h) Turn on the A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
    a) Clear the AD1IF bit.
    b) Select the A/D interrupt priority.

To perform an A/D sample and conversion using Threshold Detect scanning:

1. Configure the A/D module:
    a) Configure the port pins as analog inputs (ANSx registers).
    b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2<15:13>).
    c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
    d) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
    e) Configure the MODE12 bit to select A/D resolution (AD1CON1<10>).
    f) Select how the conversion results are presented in the buffer (AD1CON1<9:8>).
    g) Select the interrupt rate (AD1CON2<6:2>).
2. Configure the threshold compare channels:
    a) Enable auto-scan; set the ASEN bit (AD1CON5<15>).
    b) Select the Compare mode, “Greater Than, Less Than or Windowed”; set the CMx bits (AD1CON5<1:0>).
    c) Select the threshold compare channels to be scanned (AD1CSSH, AD1CSSL).
    d) If the CTMU is required as a current source for a threshold compare channel, enable the corresponding CTMU channel (AD1CTMENH, AD1CTMENL).
    e) Write the threshold values into the corresponding ADC1BUFx registers.
    f) Turn on the A/D module (AD1CON1<15>).

Note:	If performing an A/D sample and conversion, using Threshold Detect in Sleep Mode, the RC A/D clock source must be selected before entering into Sleep mode.

3. Configure the A/D interrupt (OPTIONAL):
    a) Clear the AD1IF bit.
    b) Select the A/D interrupt priority.

REGISTER 19-8: AD1CSSH: A/D INPUT SCAN SELECT REGISTER (HIGH WORD)(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS23	CSS22	CSS21	CSS20(2)	CSS19(2)	CSS18	CSS17	CSS16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-10 **CSS<30:26>:** A/D Input Scan Selection bits
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CSS<23:16>:** A/D Input Scan Selection bits(2)
1 = Includes the corresponding channel for input scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.
2: The CSS<20:19> bits are not implemented in 20-pin devices.

REGISTER 19-9: AD1CSSL: A/D INPUT SCAN SELECT REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(2,3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7(2,3)	CSS6(2,3)	CSS5(2)	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CSS<15:0>:** A/D Input Scan Selection bits(2,3)
1 = Includes the corresponding ANx input for scan
0 = Skips the channel for input scan

Note 1: Unimplemented channels are read as ‘0’. Do not select unimplemented channels for sampling as indeterminate results may be produced.
2: The CSS<8:5> bits are not implemented in 20-pin devices.
3: The CSS<8:6> bits are not implemented in 28-pin devices.

REGISTER 20-2: BUFCON0: INTERNAL VOLTAGE REFERENCE CONTROL REGISTER 0

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-1
—	—	—	—	—	—	BUFREF1	BUFREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1-0 **BUFREF<1:0>:** Internal Voltage Reference Select bits
11 = Reference output is set at 4 * BGBUF1(1)
10 = Reference output is set at 2 * BGBUF1(2)
01 = Reference output is set at BGBUF1
00 = Reserved, do not use

Note 1: Available only on PIC24FV16KMXXX devices. The reference may not be within specifications for VDD below specified levels; see Table 27-15 for minimum VDD limits.

2: The reference may not be within specifications for VDD below specified levels; see Table 27-15 for minimum VDD limits.

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REGISTER 24-1: CTMUCON1L: CTMU CONTROL 1 LOW REGISTER (CONTINUED)

bit 1-0 **IRNG<1:0>:** Current Source Range Select bits

`11` = 100 × Base Current
`10` = 10 × Base Current
`01` = Base Current Level (0.55 μA nominal)
`00` = 1000 × Base Current

25.4 Program Verification and Code Protection

For all devices in the PIC24FXXXXX family, code protection for the Boot Segment is controlled by the Configuration bit, BSS0, and the General Segment by the Configuration bit, GCP. These bits inhibit external reads and writes to the program memory space This has no direct effect in normal execution mode.

Write protection is controlled by bit, BWRP, for the Boot Segment and bit, GWRP, for the General Segment in the Configuration Word. When these bits are programmed to '0', internal write and erase operations to program memory are blocked.

25.5 In-Circuit Serial Programming

PIC24FXXXXX family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

25.6 In-Circuit Debugger

When MPLAB® ICD 3, MPLAB REAL ICE™ or PICkit™ 3 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx and PGEDx pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS}, PGECx, PGEDx and the pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

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TABLE 27-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000(2)	—	—	1.90	V	
			HLVDL<3:0> = 0001	1.88	—	2.13	V	
			HLVDL<3:0> = 0010	2.09	—	2.35	V	
			HLVDL<3:0> = 0011	2.25	—	2.53	V	
			HLVDL<3:0> = 0100	2.35	—	2.62	V	
			HLVDL<3:0> = 0101	2.55	—	2.84	V	
			HLVDL<3:0> = 0110	2.80	—	3.10	V	
			HLVDL<3:0> = 0111	2.95	—	3.25	V	
			HLVDL<3:0> = 1000	3.09	—	3.41	V	
			HLVDL<3:0> = 1001	3.27	—	3.59	V	
			HLVDL<3:0> = 1010(1)	3.46	—	3.79	V	
			HLVDL<3:0> = 1011(1)	3.62	—	4.01	V	
			HLVDL<3:0> = 1100(1)	3.91	—	4.26	V	
			HLVDL<3:0> = 1101(1)	4.18	—	4.55	V	
			HLVDL<3:0> = 1110(1)	4.49	—	4.87	V	

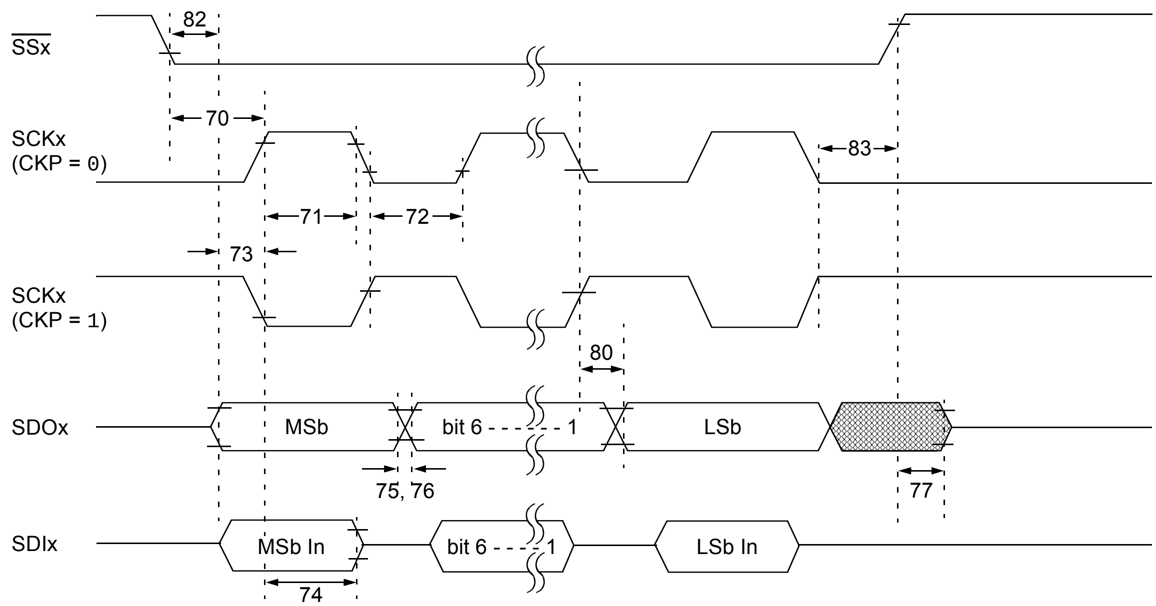
Note 1: These trip points should not be used on PIC24FXXKMXXX devices.
2: This trip point should not be used on PIC24FVXXKMXXX devices.

TABLE 27-5: BOR TRIP POINTS

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended								
Param No.	**Sym**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC15		BOR Hysteresis		—	5	—	mV	
DC19		BOR Voltage on VDD Transition	BORV<1:0> = 00	—	—	—	—	Valid for LPBOR (**Note 1)**
			BORV<1:0> = 01	2.90	3	3.38	V	
			BORV<1:0> = 10	2.53	2.7	3.07	V	
			BORV<1:0> = 11	1.75	1.85	2.05	V	**(Note 2)**
			BORV<1:0> = 11	1.95	2.05	2.16	V	**(Note 3)**

Note 1: LPBOR re-arms the POR circuit but does not cause a BOR.
2: This is valid for PIC24F (3.3V) devices.
3: This is valid for PIC24FV (5V) devices.

FIGURE 27-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 27-5 for load conditions.

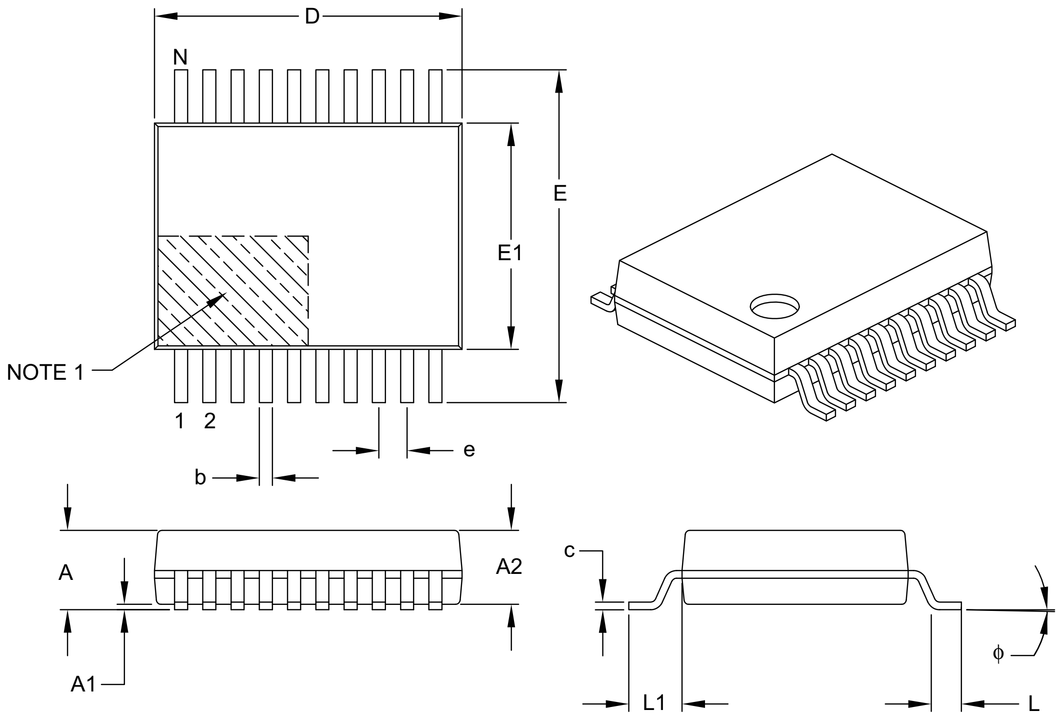
TABLE 27-32: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TSSL2SCH, TSSL2SCL	SSx ↓ to SCKx ↓ or SCKx ↑ Input		3 TCY	—	ns	
70A	TSSL2WB	SSx to Write to SSPxBUF		3 TCY	—	ns	
71	TSCH	SCKx Input High Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
71A			Single Byte	40	—	ns	**(Note 1)**
72	TSCL	SCKx Input Low Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
72A			Single Byte	40	—	ns	**(Note 1)**
73A	TB2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 TCY + 40	—	ns	**(Note 2)**
74	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TDOR	SDOx Data Output Rise Time		—	25	ns	
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
77	TSSH2DOZ	SSx ↑ to SDOx Output High-Impedance		10	50	ns	
80	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
82	TSSL2DOV	SDOx Data Output Valid After SSx ↓ Edge		—	50	ns	
83	TSCH2SSH, TSCL2SSH	SSx ↑ After SCKx Edge		1.5 TCY + 40	—	ns	
	FSCK	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.
2: Only if Parameters 71A and 72A are used.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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