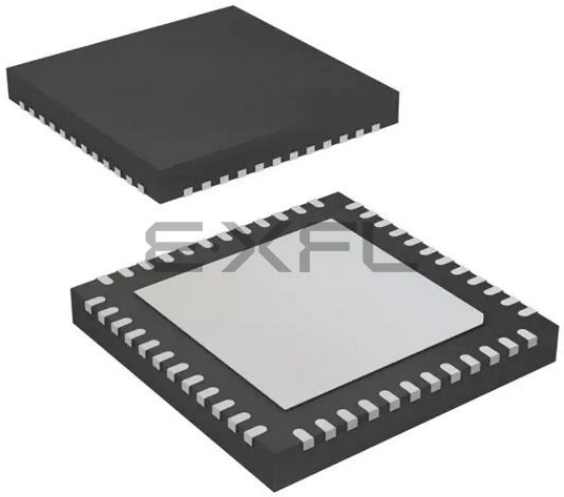

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Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f08km204-i-mv

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to for **Section 9.0 "Oscillator Configuration"**details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals, in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

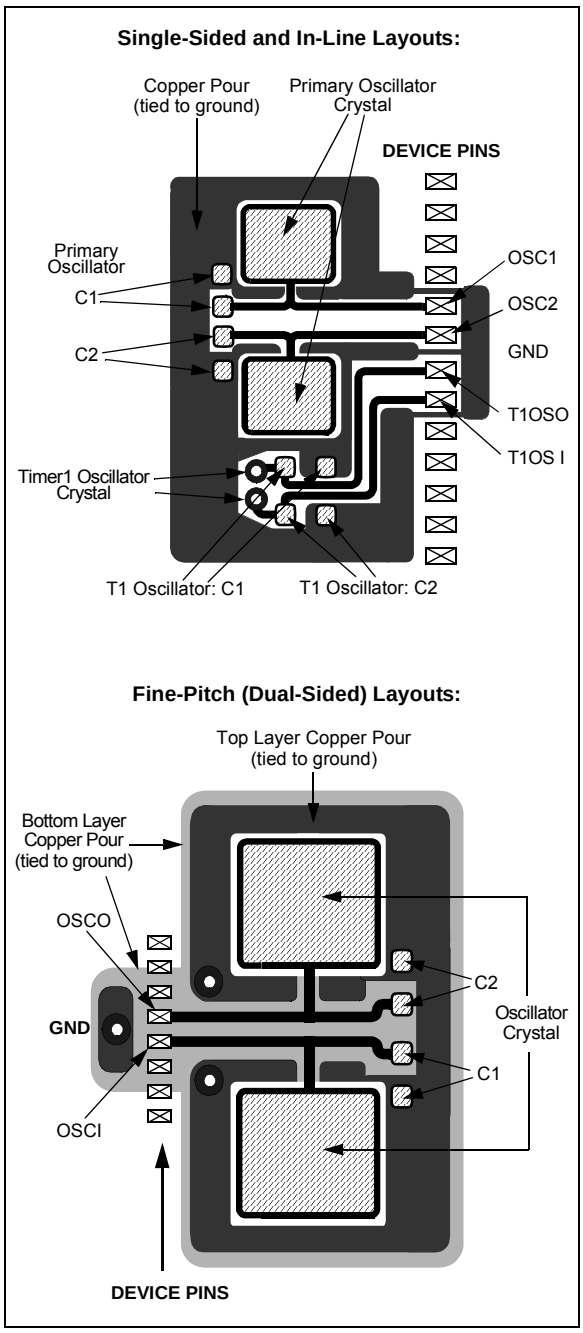
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the *"PIC24F Family Reference Manual"*, **"CPU"** (DS39703).

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory, defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to Data Space mapping feature lets any instruction access program space as if it were Data Space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (i.e., A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

TABLE 4-12: SCCP5 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP5CON1L(1)	1D0h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP5CON1H(1)	1D2h	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP5CON2L(1)	1D4h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP5CON2H(1)	1D6h	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICSEL2	ICSEL1	ICSEL0	0100
CCP5CON3H(1)	1DAh	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	—	—	—	—	—	POLACE	—	PSSACE1	PSSACE0	—	—	0000
CCP5STATL(1)	1DCh	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP5TMRL(1)	1E0h	SCCP5 Time Base Register Low Word																0000
CCP5TMRH(1)	1E2h	SCCP5 Time Base Register High Word																0000
CCP5PRL(1)	1E4h	SCCP5 Time Base Period Register Low Word																FFFF
CCP5PRH(1)	1E6h	SCCP5 Time Base Period Register High Word																FFFF
CCP5RAL(1)	1E8h	Output Compare 5 Data Word A																0000
CCP5RBL(1)	1ECh	Output Compare 5 Data Word B																0000
CCP5BUFL(1)	1F0h	Input Capture 5 Data Buffer Low Word																0000
CCP5BUFH(1)	1F2h	Input Capture 5 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-25: A/D REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	300h	A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF1	302h	A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF2	304h	A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF3	306h	A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF4	308h	A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF5	30Ah	A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF6	30Ch	A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF7	30Eh	A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF8	310h	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF9	312h	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF10	314h	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF11	316h	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare																xxxx
ADC1BUF12	318h	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF13	31Ah	A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF14	31Ch	A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF15	31Eh	A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF16	320h	A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF17	322h	A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF18	324h	A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF19	326h	A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF20	328h	A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF21	32Ah	A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF22	32Ch	A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF23	32Eh	A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare																xxxx
AD1CON1	340h	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	342h	PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	344h	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	348h	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	34Eh	—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—	CSS23	CSS22	CSS21	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16	0000
AD1CSSL	350h	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(1,2)	CSS7(1,2)	CSS6(1,2)	CSS5(1)	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON5	354h	ASEN	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	356h	—	—	—	—	—	—	—	—	CHH23	CHH22	CHH21	CHH20(1)	CHH19(1)	CHH18	CHH17	CHH16	0000
AD1CHITL	358h	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8(1,2)	CHH7(1,2)	CHH6(1,2)	CHH5(1)	CHH4	CHH3	CHH2	CHH1	CHH0	0000
AD1CTMENH	360h	—	—	—	—	—	—	—	—	CTMEN23	CTMEN22	CTMEN21	CTMEN20(1)	CTMEN19(1)	CTMEN18	CTMEN17	CTMEN16	0000
AD1CTMENL	362h	CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8((1,2)	CTMEN7(1,2)	CTMEN6(1,2)	CTMEN5(1)	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

4.2.5 SOFTWARE STACK

In addition to its use as a working register, the W15 register in PIC24F devices is also used as a Software Stack Pointer. The pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as depicted in Figure 4-4.

For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

Note:	A PC push during exception processing will concatenate the SRL register to the MSB of the PC prior to the push.

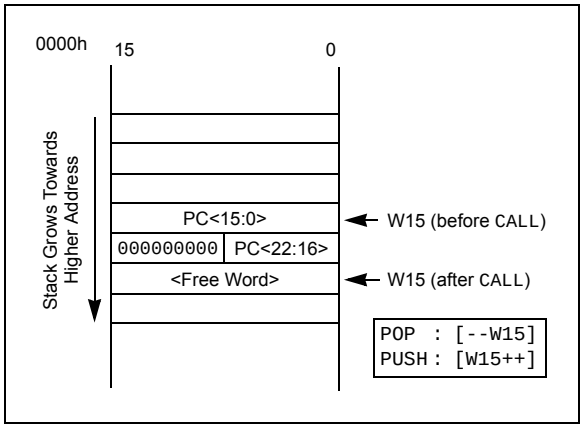
The Stack Pointer Limit Value (SPLIM) register, associated with the Stack Pointer, sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' as all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation.

Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address, 0DF6 in RAM, initialize the SPLIM with the value, 0DF4.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0800h. This prevents the stack from interfering with the Special Function Register (SFR) space.

Note:	A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-4: CALL STACK FRAME



4.3 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit-wide program space and 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Apart from the normal execution, the PIC24F architecture provides two methods by which the program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space, PSV

Table instructions allow an application to read or write small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. It can only access the least significant word (lsw) of the program word.

4.3.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit (MSb) of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility Page Address register (PSVPAG) is used to define a 16K word page in the program space. When the MSb of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike the table operations, this limits remapping operations strictly to the user memory area.

See Table 4-35 and Figure 4-5 to know how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a Data Space word.

REGISTER 7-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.

3: This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

7.1 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 7-2. If clock switching is disabled, the system clock source is always selected according to the Oscillator Configuration bits. For more information, see **Section 9.0 "Oscillator Configuration"**.

TABLE 7-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC<2:0> Configuration bits (FOSCSEL<2:0>)
BOR	
$\overline{\text{MCLR}}$	COSC<2:0> Control bits (OSCCON<14:12>)
WDTO	
SWR	

7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-3. Note that the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR and PWRT delay times expire.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR(6)	EC	TPOR + TPWRT	—	1, 2
	FRC, FRCDIV	TPOR + TPWRT	TFRC	1, 2, 3
	LPRC	TPOR + TPWRT	TLPRC	1, 2, 3
	ECPLL	TPOR + TPWRT	TLOCK	1, 2, 4
	FRCPLL	TPOR + TPWRT	TFRC + TLOCK	1, 2, 3, 4
	XT, HS, SOSC	TPOR+ TPWRT	TOST	1, 2, 5
	XTPLL, HSPLL	TPOR + TPWRT	TOST + TLOCK	1, 2, 4, 5
BOR	EC	TPWRT	—	2
	FRC, FRCDIV	TPWRT	TFRC	2, 3
	LPRC	TPWRT	TLPRC	2, 3
	ECPLL	TPWRT	TLOCK	2, 4
	FRCPLL	TPWRT	TFRC + TLOCK	2, 3, 4
	XT, HS, SOSC	TPWRT	TOST	2, 5
	XTPLL, HSPLL	TPWRT	TFRC + TLOCK	2, 3, 4
All Others	Any Clock	—	—	None

Note 1: TPOR = Power-on Reset delay.

2: TPWRT = 64 ms nominal if the Power-up Timer is enabled; otherwise, it is zero.

3: TFRC and TLPRC = RC Oscillator start-up times.

4: TLOCK = PLL Lock time.

5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

6: If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

Note: For detailed operating frequency and timing specifications, see **Section 27.0 "Electrical Characteristics"**.

7.2.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer (OST) has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.2.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

7.3 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSCx bits in the Flash Configuration Word (FOSCSEL<2:0>); see Table 7-2. The RCFGCAL and NVMCON registers are only affected by a POR.

7.4 Brown-out Reset (BOR)

The PIC24FXXXXX family devices implement a BOR circuit, which provides the user several configuration and power-saving options. The BOR is controlled by the BORV<1:0> and BOREN<1:0> Configuration bits (FPOR<6:5,1:0>). There are a total of four BOR configurations, which are provided in Table 7-3.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of V_{DD} below the set threshold point will reset the device. The chip will remain in BOR until V_{DD} rises above the threshold.

If the Power-up Timer is enabled, it will be invoked after V_{DD} rises above the threshold. Then, it will keep the chip in Reset for an additional time delay, T_{PWRT}, if V_{DD} drops below the threshold while the Power-up Timer is running. The chip goes back into a BOR and the Power-up Timer will be initialized. Once V_{DD} rises above the threshold, the Power-up Timer will execute the additional time delay.

BOR and the Power-up Timer (PWRT) are independently configured. Enabling the Brown-out Reset does not automatically enable the PWRT.

7.4.1 LOW-POWER BOR (LPBOR)

The Low-Power BOR is an alternate setting for the BOR, designed to consume minimal power. In LPBOR mode, BORV<1:0> (FPOR<6:5>) = 00. The BOR trip point is approximately 2.0V. Due to the low current consumption, the accuracy of the LPBOR mode can vary.

Unlike the other BOR modes, LPBOR mode will not cause a device Reset when V_{DD} drops below the trip point. Instead, it re-arms the POR circuit to ensure that the device will reset properly in the event that V_{DD} continues to drop below the minimum operating voltage.

The device will continue to execute code when V_{DD} is below the level of the LPBOR trip point. A device that requires falling edge BOR protection to prevent code from improperly executing should use one of the other BOR voltage settings.

7.4.2 SOFTWARE ENABLED BOR

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON<13>). Setting SBOREN enables the BOR to function as previously described. Clearing the SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise, it is read as '0'.

Placing BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change the BOR configuration. It also allows the user to tailor the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when the BOR is under software control, the Brown-out Reset voltage level is still set by the BORV<1:0> Configuration bits; it can not be changed in software.

7.4.3 DETECTING BOR

When BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

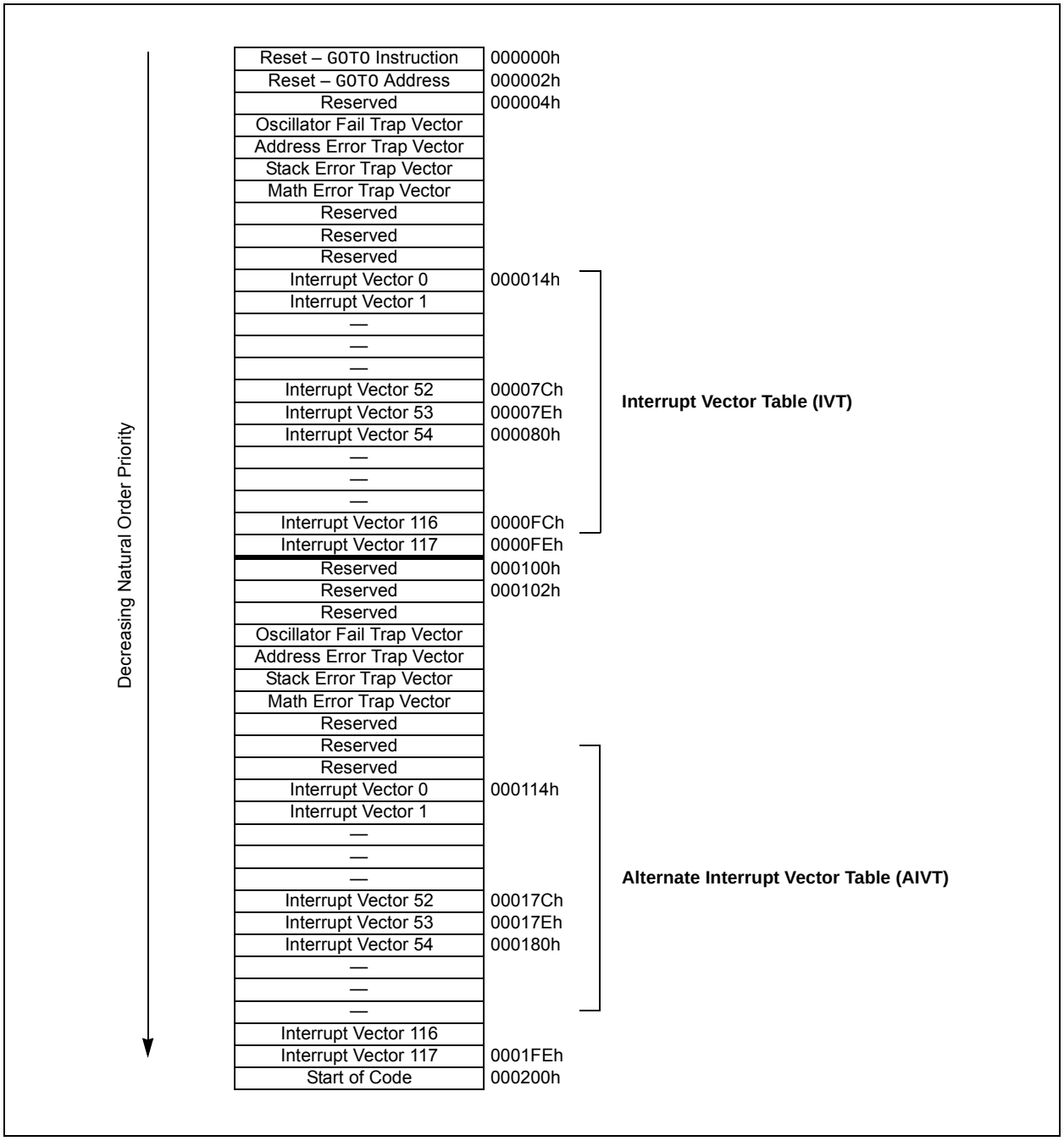
7.4.4 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

Note:	BOR levels differ depending on device type; PIC24FV16KM204 devices are at different levels than those of PIC24F16KM204 devices. See **Section 27.0 "Electrical Characteristics"** for BOR voltage levels.

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



14.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on MSSP, refer to the *"PIC24F Family Reference Manual"*.

The Master Synchronous Serial Port (MSSP) module is an 8-bit serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, Shift registers, display drivers, A/D Converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C™)
  - Full Master mode
  - Slave mode (with general address call)

The SPI interface supports these modes in hardware:

- Master mode
- Slave mode
- Daisy-Chaining Operation in Slave mode
- Synchronized Slave Operation

The I^2C interface supports the following modes in hardware:

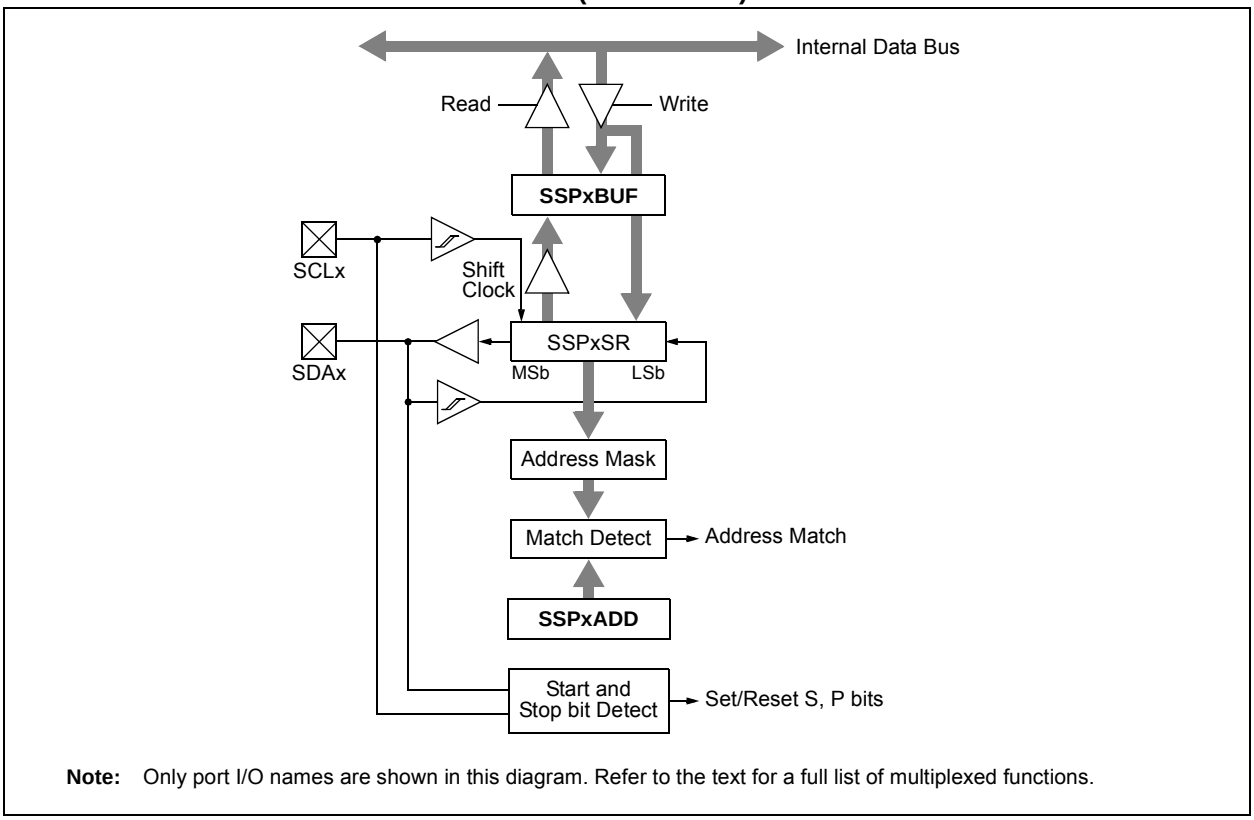
- Master mode
- Multi-Master mode
- Slave mode with 10-Bit and 7-Bit Addressing and Address Masking
- Byte NACKing
- Selectable Address and Data Hold, and Interrupt Masking

14.1 I/O Pin Configuration for SPI

In SPI Master mode, the MSSP module will assert control over any pins associated with the SDOx and SCKx outputs. This does not automatically disable other digital functions associated with the pin and may result in the module driving the digital I/O port inputs. To prevent this, the MSSP module outputs must be disconnected from their output pins while the module is in SPI Master mode. While disabling the module temporarily may be an option, it may not be a practical solution in all applications.

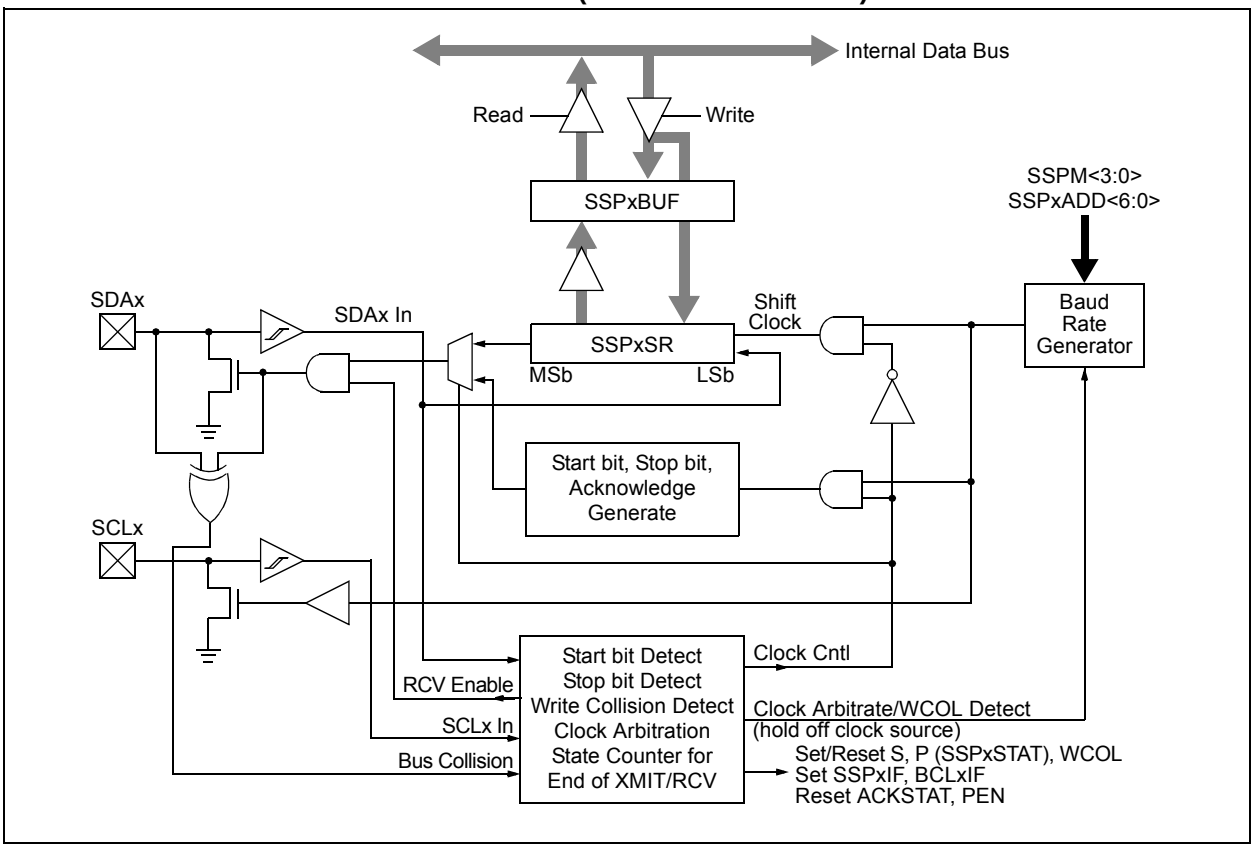
The SDOx and SCKx outputs for the module can be selectively disabled by using the SDOxDIS and SCKxDIS bits in the PADCFG1 register (Register 14-10). Setting the bit disconnects the corresponding output for a particular module from its assigned pin.

FIGURE 14-3: MSSPx BLOCK DIAGRAM (I^2C™ MODE)



Note: Only port I/O names are shown in this diagram. Refer to the text for a full list of multiplexed functions.

FIGURE 14-4: MSSPx BLOCK DIAGRAM (I^2C™ MASTER MODE)



16.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"PIC24F Family Reference Manual"*, **"Real-Time Clock and Calendar (RTCC)"** (DS39696).

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

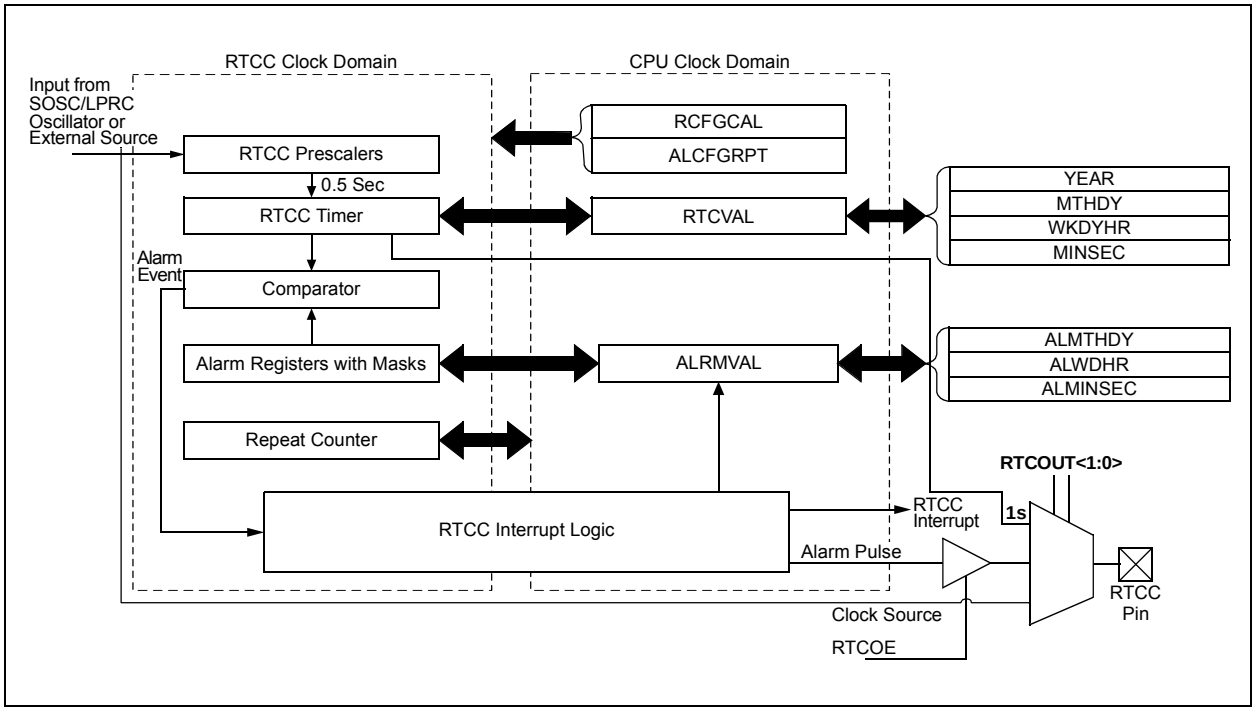
Key features of the RTCC module are:

- Operates in Sleep and Retention Sleep modes
- Selectable clock source
- Provides hours, minutes and seconds using 24-hour format
- Visibility of one half second period
- Provides calendar – weekday, date, month and year
- Alarm-configurable for half a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month or one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat chime
- Year 2000 to 2099 leap year correction
- BCD format for smaller software overhead
- Optimized for long term battery operation
- User calibration of the 32.768 kHz clock crystal/32K INTRC frequency with periodic auto-adjust
- Optimized for long term battery operation
- Fractional second synchronization
- Calibration to within ±2.64 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Ability to periodically wake-up external devices without CPU intervention (external power control)
- Power control output for external circuit control
- Calibration takes effect every 15 seconds
- Runs from any one of the following:
  - External Real-Time Clock of 32.768 kHz
  - Internal 31.25 kHz LPRC Clock
  - 50 Hz or 60 Hz External Input

16.1 RTCC Source Clock

The user can select between the SOSC crystal oscillator, LPRC internal oscillator or an external 50 Hz/60 Hz power line input as the clock reference for the RTCC module. This gives the user an option to trade off system cost, accuracy and power consumption, based on the overall system needs.

FIGURE 16-1: RTCC BLOCK DIAGRAM



16.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 16-4: YEAR: YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 16-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 17-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

NOTES:

21.0 DUAL OPERATIONAL AMPLIFIER MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **"Operational Amplifier (Op Amp)"** (DS30505). Device-specific information in this data sheet supersedes the information in the *"PIC24F Family Reference Manual"*.

PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal unity-gain buffer option
- Multiple input options each on the inverting and non-inverting amplifier inputs
- Rail-to-rail input and output capabilities
- User-selectable option for regular or low-power operation
- User-selectable operation in Idle and Sleep modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 "Configuring Analog Port Pins"** for more information.

FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM

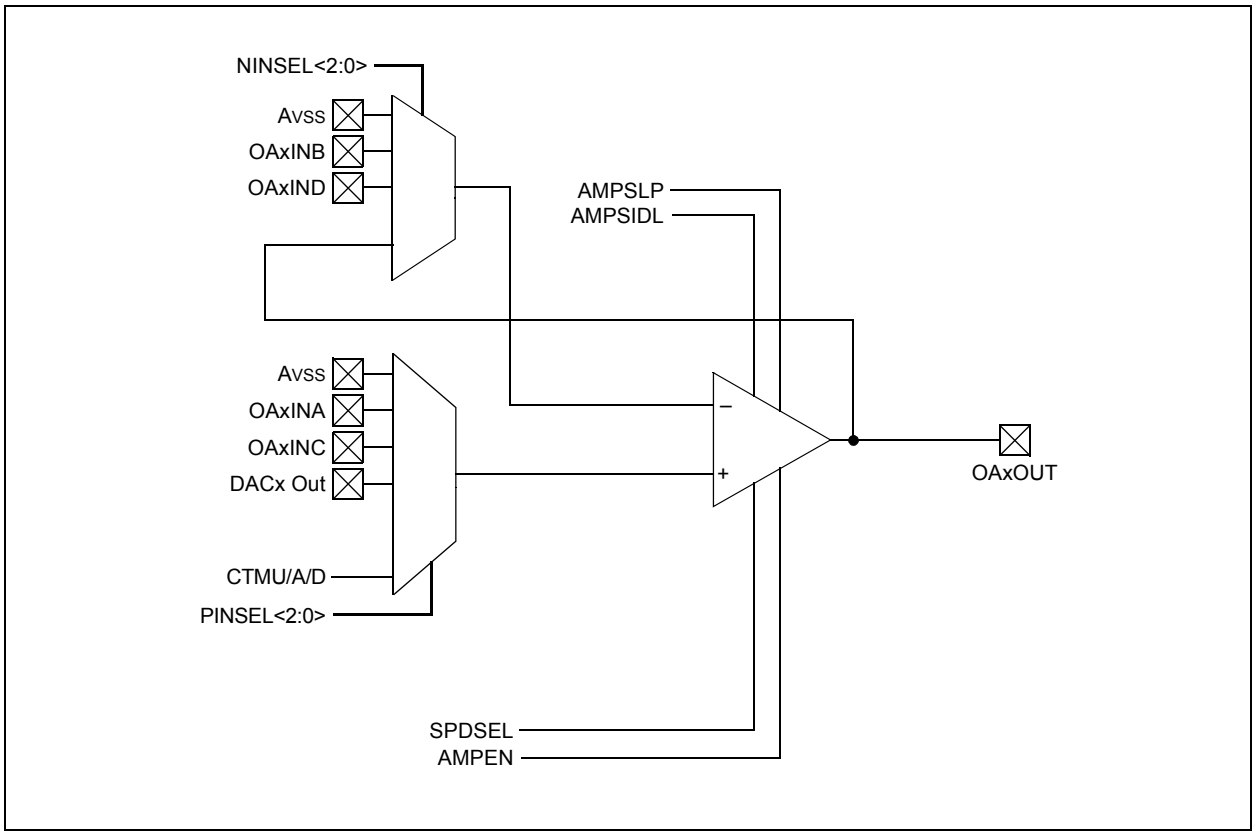
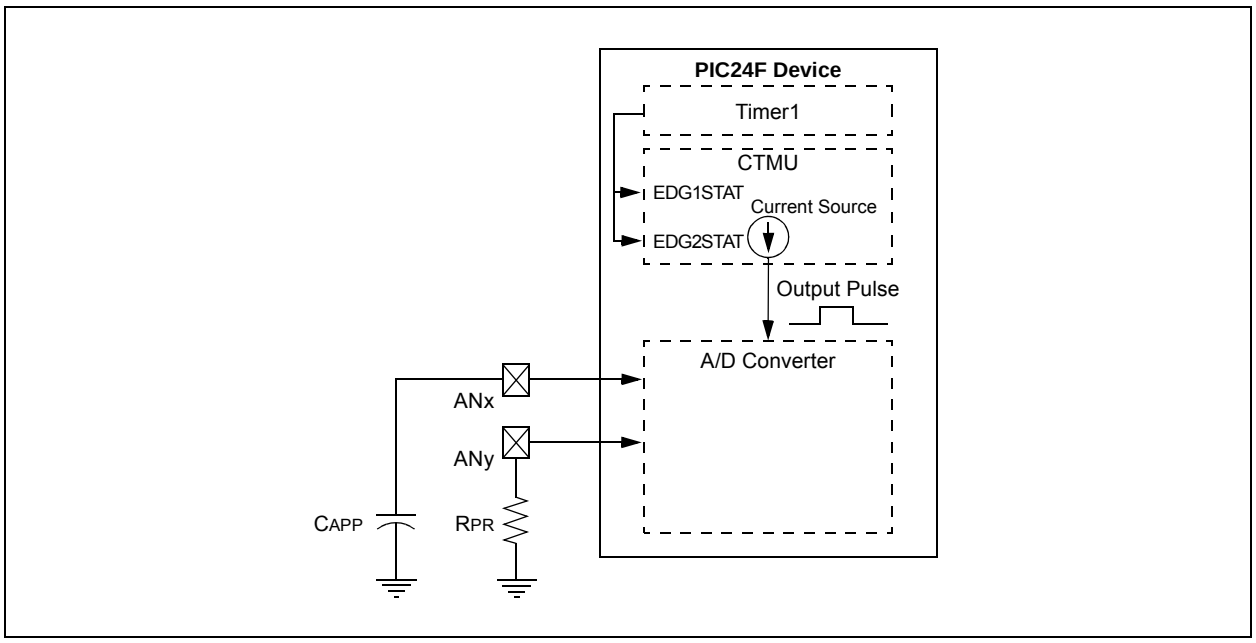


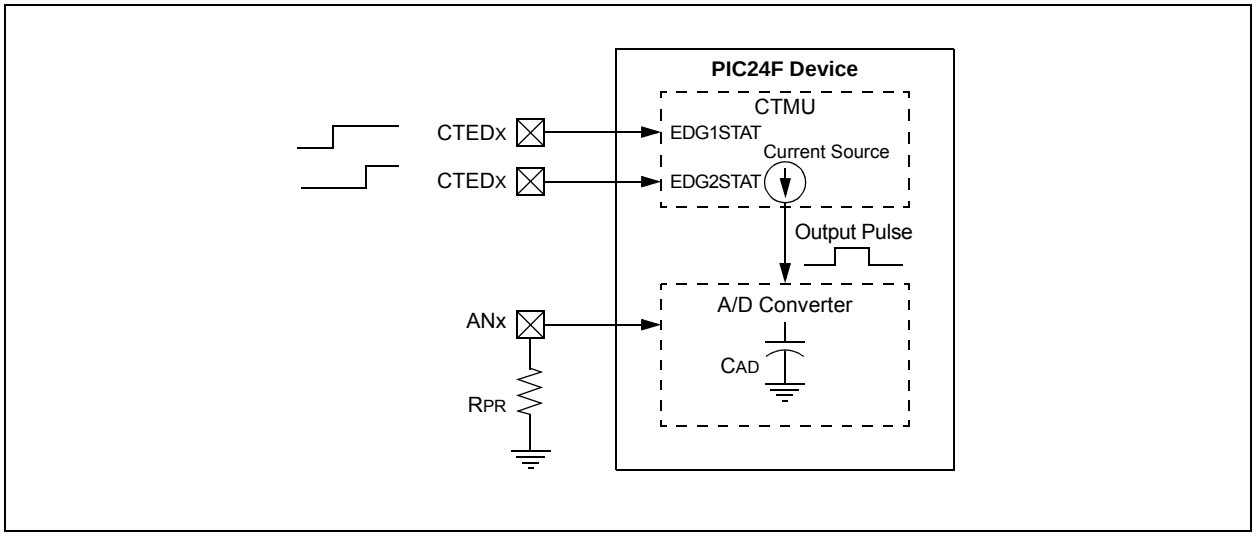
FIGURE 24-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT



24.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (C_{AD}) and a precision resistor for current calibration. Figure 24-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

FIGURE 24-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT



26.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

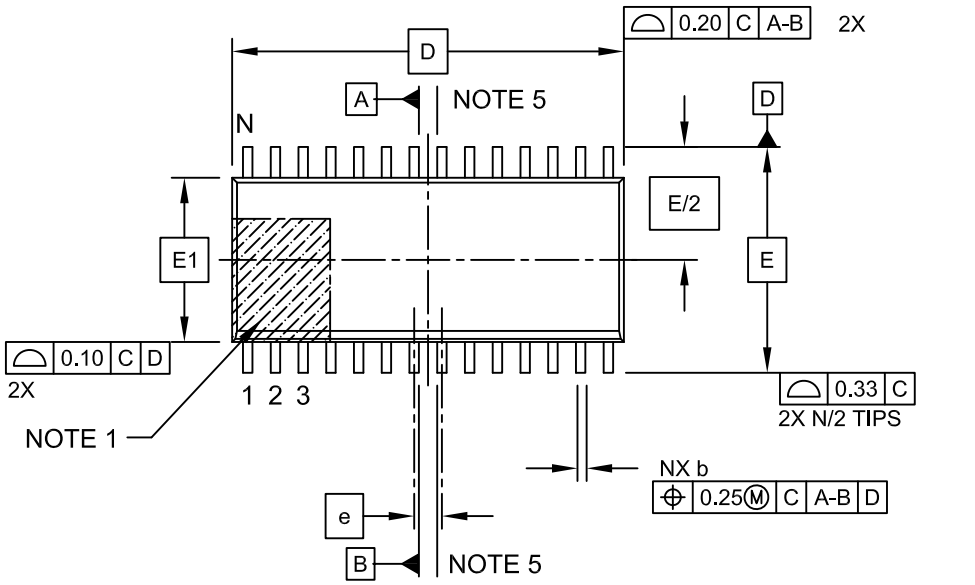
26.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

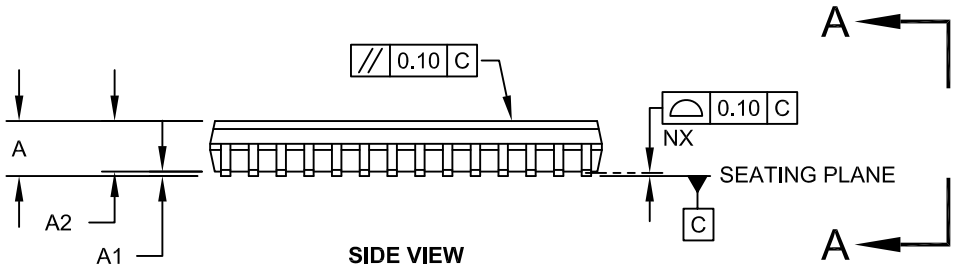
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

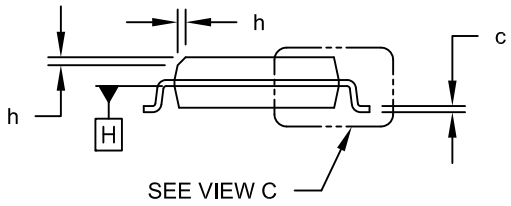
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2