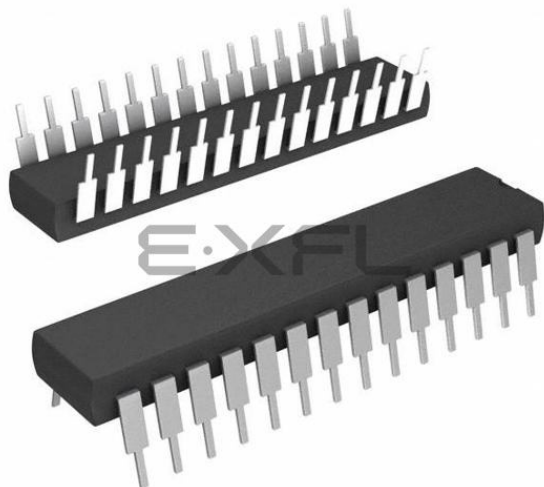




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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km102-e-sp

PIC24FV16KM204 FAMILY

Device	Pins	Memory			Voltage Range (V)	Peripherals												ICD BRKPT
		Flash Program (bytes)	SRAM (bytes)	EE Data (bytes)		16-Bit Timer	16-Bit MCCP/SCCP	MSSP	UART	12-Bit A/D Channels	8-Bit DAC	Op Amp	Comparators	CTMU	RTCC	CLC		
5V Devices																		
PIC24FV16KM204	44	16K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3	
PIC24FV16KM202	28	16K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3	
PIC24FV08KM204	44	8K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3	
PIC24FV08KM202	28	8K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3	
PIC24FV16KM104	44	16K	1K	512	2.0-5.5	1	1/1	1	1	22	—	—	1	Yes	—	1	3	
PIC24FV16KM102	28	16K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3	
PIC24FV08KM102	28	8K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3	
PIC24FV08KM101	20	8K	1K	512	2.0-5.5	1	1/1	1	1	16	—	—	1	Yes	—	1	3	
3V Devices																		
PIC24F16KM204	44	16K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3	
PIC24F16KM202	28	16K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3	
PIC24F08KM204	44	8K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3	
PIC24F08KM202	28	8K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3	
PIC24F16KM104	44	16K	1K	512	1.8-3.6	1	1/1	1	1	22	—	—	1	Yes	—	1	3	
PIC24F16KM102	28	16K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3	
PIC24F08KM102	28	8K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3	
PIC24F08KM101	20	8K	1K	512	1.8-3.6	1	1/1	1	1	16	—	—	1	Yes	—	1	3	

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Analog Inputs
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	A/D Analog Inputs
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	A/D Analog Inputs
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	A/D Analog Inputs
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	A/D Analog Inputs
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	A/D Analog Inputs
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	A/D Analog Inputs
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	A/D Analog Inputs
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	A/D Analog Inputs
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	A/D Analog Inputs
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	A/D Analog Inputs
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	A/D Analog Inputs
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	A/D Analog Inputs
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	A/D Analog Inputs
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	A/D Analog Inputs
AN16	10	12	9	34	37	10	12	9	34	37	I	ANA	A/D Analog Inputs
AN17	—	14	11	41	45	—	14	11	41	45	I	ANA	A/D Analog Inputs
AN18	—	15	12	42	46	—	15	12	42	46	I	ANA	A/D Analog Inputs
AN19	11	16	13	43	47	11	16	13	43	47	I	ANA	A/D Analog Inputs
AN20	12	17	14	44	48	12	17	14	44	48	I	ANA	A/D Analog Inputs
AN21	13	18	15	1	1	13	18	15	1	1	I	ANA	A/D Analog Inputs
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I ² C™	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I ² C	Alternate I2C1 Data Input/Output
AVDD	20	28	25	17	18	20	28	25	17	18	P	—	A/D Supply Pins
AVss	19	27	24	16	17	19	27	24	16	17	P	—	A/D Supply Pins
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I²C™ = I²C/SMBus input buffer

PIC24FV16KM204 FAMILY

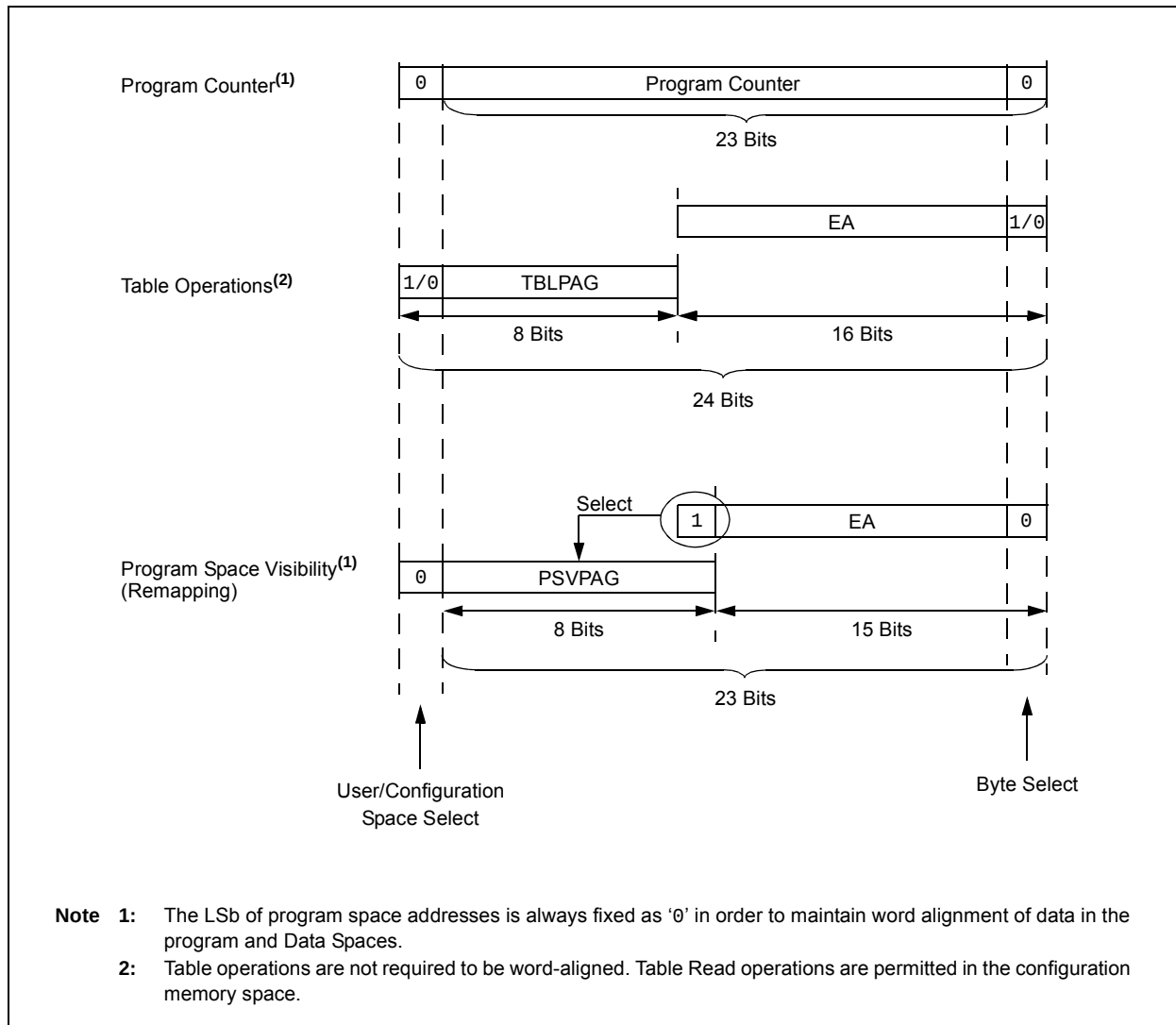
TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG<7:0> ⁽²⁾		Data EA<14:0> ⁽¹⁾	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

2: PSVPAG can have only two values ('00' to access program memory and FF to access data EEPROM) on the PIC24F16KM family.

FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



PIC24FV16KM204 FAMILY

REGISTER 8-16: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
DAC2IE	DAC1IE	CTMUIE	—	—	—	—	HLVDIE
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	U2ERIE	U1ERIE	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **DAC2IE:** Digital-to-Analog Converter 2 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 14 **DAC1IE:** Digital-to-Analog Converter 1 Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

PIC24FV16KM204 FAMILY

REGISTER 8-17: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ULPWUIE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ULPWUIE:** Ultra Low-Power Wake-up Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

REGISTER 8-18: IEC6: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CLC2IE	CLC1IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **CLC2IE:** Configurable Logic Cell 2 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 0 **CLC1IE:** Configurable Logic Cell 1 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

PIC24FV16KM204 FAMILY

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7	CLKLOCK: Clock Selection Lock Enable bit <u>If FSCM is Enabled (FCKSM1 = 1):</u> 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit <u>If FSCM is Disabled (FCKSM1 = 0):</u> Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.
bit 6	Unimplemented: Read as '0'
bit 5	LOCK: PLL Lock Status bit ⁽²⁾ 1 = PLL module is in lock or PLL module start-up timer is satisfied 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
bit 4	Unimplemented: Read as '0'
bit 3	CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected
bit 2	SOSCDRV: Secondary Oscillator Drive Strength bit ⁽³⁾ 1 = High-power SOSC circuit is selected 0 = Low/high-power select is done via the SOSCSRC Configuration bit
bit 1	SOSCEN: 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enables the Secondary Oscillator 0 = Disables the Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Initiates an oscillator switch to the clock source specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Reset values for these bits are determined by the FNOSCx Configuration bits.
- 2:** This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
- 3:** When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSCSRC = 0), this bit has no effect.

PIC24FV16KM204 FAMILY

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN ⁽¹⁾	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit

1 = Interrupts clear the DOZEN bit, and reset the CPU and peripheral clock ratio to 1:1

0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU and Peripheral Clock Ratio Select bits

111 = 1:128

110 = 1:64

101 = 1:32

100 = 1:16

011 = 1:8

010 = 1:4

001 = 1:2

000 = 1:1

bit 11 **DOZEN:** Doze Enable bit⁽¹⁾

1 = DOZE<2:0> bits specify the CPU and peripheral clock ratio

0 = CPU and peripheral clock ratio are set to 1:1

bit 10-8 **RCDIV<2:0>:** FRC Postscaler Select bits

When COSC<2:0> (OSCCON<14:12>) = 111:

111 = 31.25 kHz (divide-by-256)

110 = 125 kHz (divide-by-64)

101 = 250 kHz (divide-by-32)

100 = 500 kHz (divide-by-16)

011 = 1 MHz (divide-by-8)

010 = 2 MHz (divide-by-4)

001 = 4 MHz (divide-by-2) – default

000 = 8 MHz (divide-by-1)

When COSC<2:0> (OSCCON<14:12>) = 110:

111 = 1.95 kHz (divide-by-256)

110 = 7.81 kHz (divide-by-64)

101 = 15.62 kHz (divide-by-32)

100 = 31.25 kHz (divide-by-16)

011 = 62.5 kHz (divide-by-8)

010 = 125 kHz (divide-by-4)

001 = 250 kHz (divide-by-2) – default

000 = 500 kHz (divide-by-1)

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

PIC24FV16KM204 FAMILY

NOTES:

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PIC24FV16KM204 FAMILY

21.0 DUAL OPERATIONAL AMPLIFIER MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, “Operational Amplifier (Op Amp)” (DS30505). Device-specific information in this data sheet supersedes the information in the “PIC24F Family Reference Manual”.

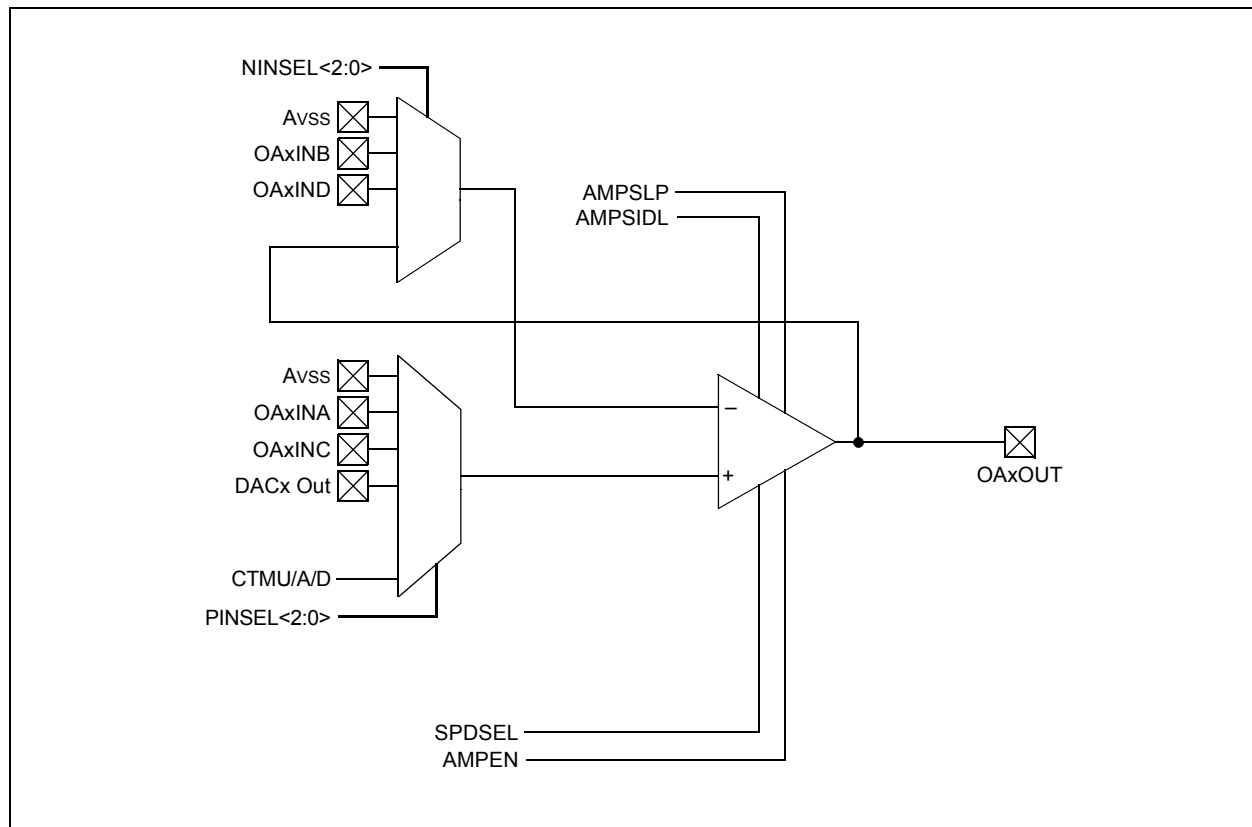
PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal unity-gain buffer option
- Multiple input options each on the inverting and non-inverting amplifier inputs
- Rail-to-rail input and output capabilities
- User-selectable option for regular or low-power operation
- User-selectable operation in Idle and Sleep modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 “Configuring Analog Port Pins”** for more information.

FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM



PIC24FV16KM204 FAMILY

REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
EVPOL1 ⁽²⁾	EVPOL0 ⁽²⁾	—	CREF1	CREF0	—	CCH1	CCH0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **CON:** Comparator x Enable bit

1 = Comparator is enabled

0 = Comparator is disabled

bit 14 **COE:** Comparator x Output Enable bit

1 = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 **CPOL:** Comparator x Output Polarity Select bit

1 = Comparator output is inverted

0 = Comparator output is not inverted

bit 12 **CLPWR:** Comparator x Low-Power Mode Select bit

1 = Comparator operates in Low-Power mode

0 = Comparator does not operate in Low-Power mode

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator x Event bit

1 = Comparator event, defined by EVPOL<1:0>, has occurred; subsequent Triggers and interrupts are disabled until the bit is cleared

0 = Comparator event has not occurred

bit 8 **COUT:** Comparator x Output bit

When CPOL = 0:

1 = $V_{IN+} > V_{IN-}$

0 = $V_{IN+} < V_{IN-}$

When CPOL = 1:

1 = $V_{IN+} < V_{IN-}$

0 = $V_{IN+} > V_{IN-}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits⁽²⁾

11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output

01 = Trigger/event/interrupt is generated on the low-to-high transition of the comparator output

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **CREF<1:0>:** Comparator x Reference Select bits (non-inverting input)

11 = Non-inverting input connects to the DAC2 output

10 = Non-inverting input connects to the DAC1 output

01 = Non-inverting input connects to the internal CVREF voltage

00 = Non-inverting input connects to the CxINA pin

Note 1: BGBUF1 voltage is configured by BUFREF1<1:0> (BUFCON0<1:0>).

2: If the EVPOL<1:0> bits are set to a value other than '00', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

23.0 COMPARATOR VOLTAGE REFERENCE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to the “PIC24F Family Reference Manual”, “Comparator Voltage Reference Module” (DS39709).

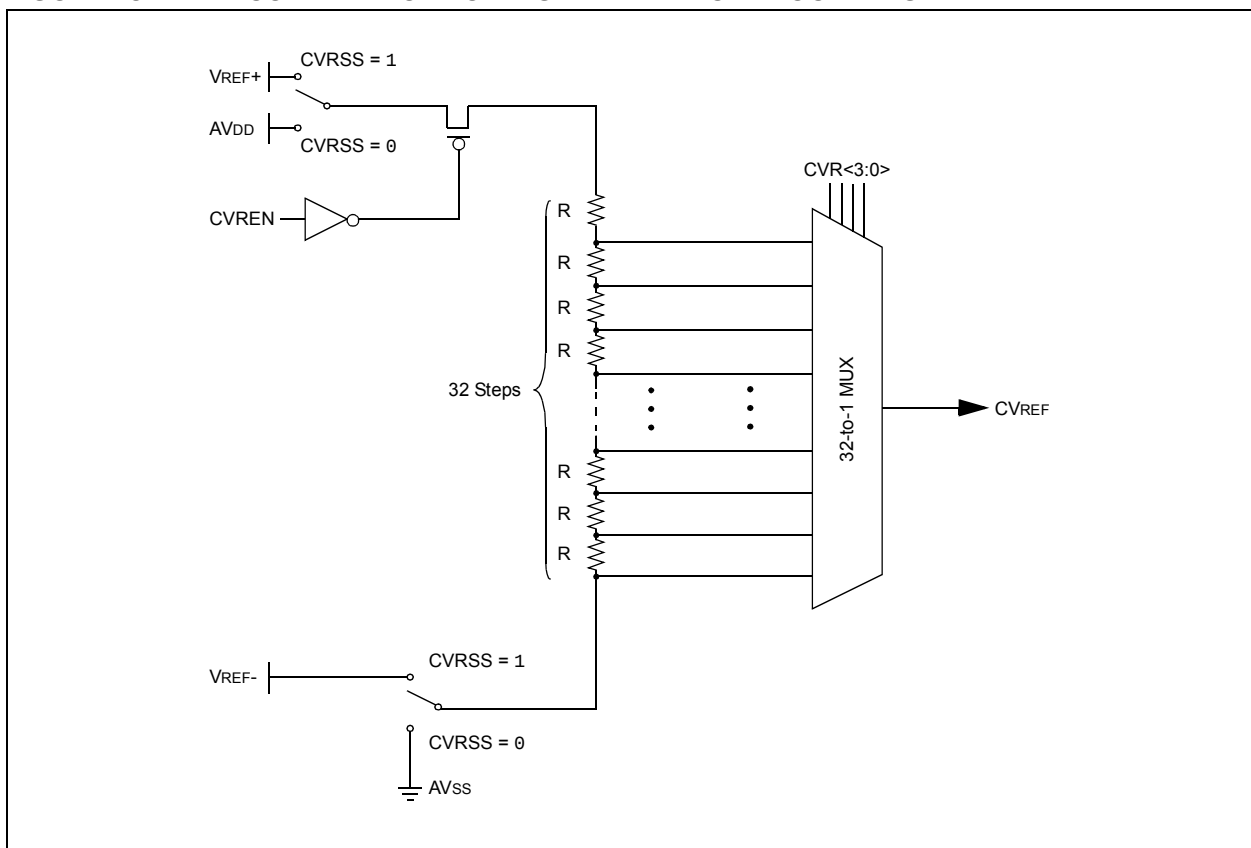
23.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 23-1). The comparator voltage reference provides a range of output voltages with 32 distinct levels.

The comparator voltage reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



PIC24FV16KM204 FAMILY

REGISTER 25-2: FGS: GENERAL SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
—	—	—	—	—	—	GCP	GWRP
bit 7							bit 0

Legend:

R = Readable bit C = Clearable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7-2 **Unimplemented:** Read as '0'
- bit 1 **GCP:** General Segment Code Flash Code Protection bit
 1 = No protection
 0 = Standard security is enabled
- bit 0 **GWRP:** General Segment Code Flash Write Protection bit
 1 = General Segment may be written
 0 = General Segment is write-protected

REGISTER 25-3: FOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
IESO	LPRCSEL	SOSCSRC	—	—	FNOSC2	FNOSC1	FNOSC0
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **IESO:** Internal External Switchover bit
 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **LPRCSEL:** Internal LPRC Oscillator Power Select bit
 1 = High-Power/High-Accuracy mode
 0 = Low-Power/Low-Accuracy mode
- bit 5 **SOSCSRC:** Secondary Oscillator Clock Source Configuration bit
 1 = SOSC analog crystal function is available on the SOSCI/SOSCO pins
 0 = SOSC crystal is disabled; digital SCLKI function is selected on the SOSCO pin
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
 000 = Fast RC Oscillator (FRC)
 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCDIV+PLL)
 010 = Primary Oscillator (XT, HS, EC)
 011 = Primary Oscillator with PLL module (HS+PLL, EC+PLL)
 100 = Secondary Oscillator (SOSC)
 101 = Low-Power RC Oscillator (LPRC)
 110 = 500 kHz Low-Power FRC Oscillator with Divide-by-N (LPFRCDIV)
 111 = 8 MHz FRC Oscillator with Divide-by-N (FRCDIV)

PIC24FV16KM204 FAMILY

TABLE 27-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Parameter No.	Device	Typical ⁽¹⁾	Max	Units	Conditions		
Power-Down Current (IPD)							
DC60	PIC24FV16KMXXX	6.0	—	μA	-40°C	2.0V	Sleep Mode ⁽²⁾
			8.0		+25°C		
			8.5		+60°C		
			9.0		+85°C		
			15.0		+125°C		
		6.0	—	μA	-40°C	5.0V	
			8.0		+25°C		
			9.0		+60°C		
			10.0		+85°C		
			15.0		+125°C		
	PIC24F16KMXXX	0.025	—	μA	-40°C	1.8V	
			0.80		+25°C		
			1.5		+60°C		
			2.0		+85°C		
			7.5		+125°C		
		0.040	—	μA	-40°C	3.3V	
			1.0		+25°C		
			2.0		+60°C		
			3.0		+85°C		
			7.5		+125°C		
DC61	PIC24FV16KMXXX	0.25	—	μA	+85°C	2.0V	Low-Voltage Sleep Mode ⁽²⁾
			7.5		+125°C		
		0.35	3.0	μA	+85°C	5.0V	
			7.5		+125°C		

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: Data in the Typical column is at 3.3V, +25°C (PIC24F16KMXXX) or 5.0V, +25°C (PIC24FV16KMXXX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low. PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

PIC24FV16KM204 FAMILY

TABLE 27-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated) -40°C ≤ TA ≤ +125°C for Extended							
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VBG	Band Gap Reference Voltage	0.973	1.024	1.075	V	VDD > 4.5V for 4*VBG reference VDD > 2.3V for 2*VBG reference
	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
	VRGOUT	Regulator Output Voltage	3.1	3.3	3.6	V	
	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Series resistance < 3 Ohm recommended; < 5 Ohm is required.
	VLVR	Low-Voltage Regulator Output Voltage	—	2.6	—	V	

TABLE 27-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Comments	Conditions
	IOUT1	CTMU Current Source, Base Range	—	550	—	nA	CTMUCON1L<1:0> = 01	2.5V < VDD < VDDMAX
	IOUT2	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUCON1L<1:0> = 10	
	IOUT3	CTMU Current Source, 100x Range	—	55	—	μA	CTMUCON1L<1:0> = 11	
	IOUT4	CTMU Current Source, 1000x Range	—	550	—	μA	CTMUCON1L<1:0> = 00 (Note 2)	
	VF	Temperature Diode Forward Voltage	—	.76	—	V		
	VΔ	Voltage Change per Degree Celsius	—	1.6	—	mV/°C		

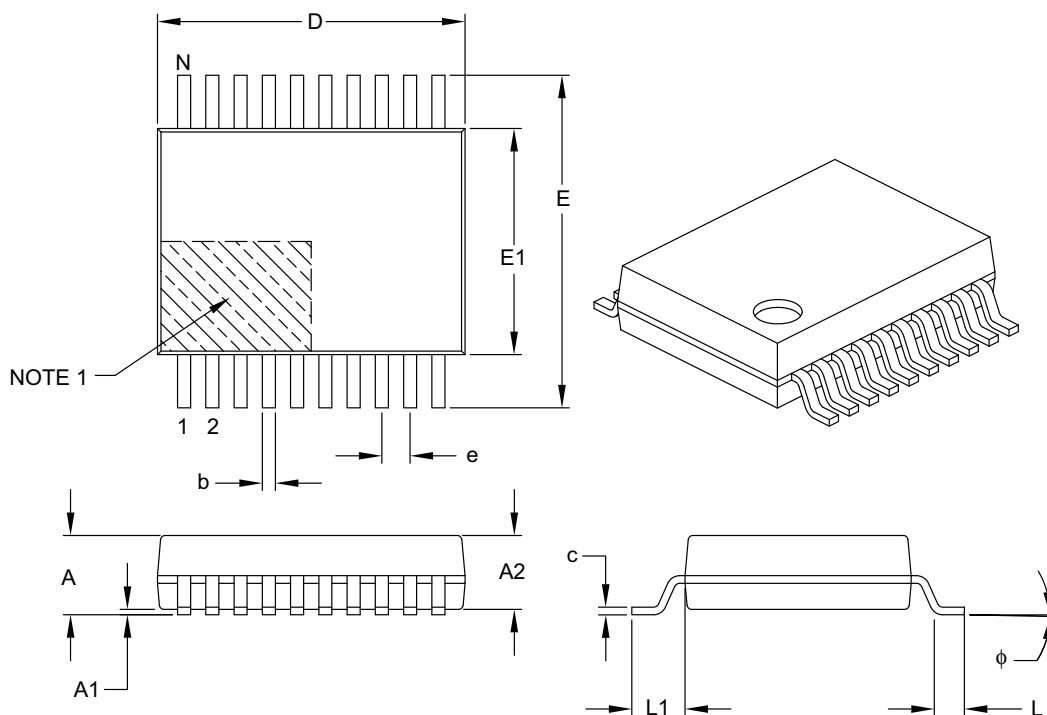
Note 1: Nominal value at the center point of the current trim range (CTMUCON1L<7:2> = 000000). On PIC24F16KM parts, the current output is limited to the typical current value when IOUT4 is chosen.

2: Do not use this current range with a temperature sensing diode.

PIC24FV16KM204 FAMILY

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

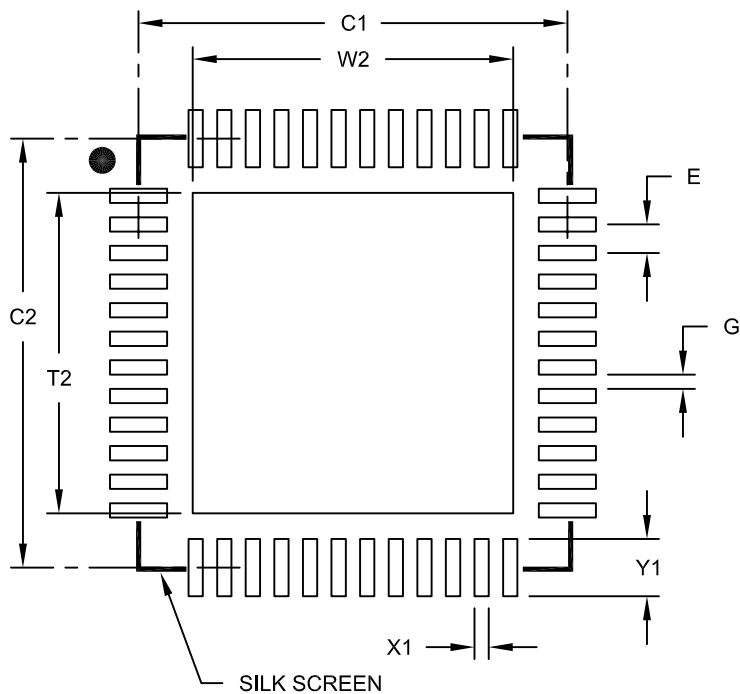
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

PIC24FV16KM204 FAMILY

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

PIC24FV16KM204 FAMILY

Comparator Voltage Reference	239	Device Overview	13
Configuring	239	Core Features	13
Configurable Logic Cell (CLC)	195	Other Special Features	14
Configuration Bits	249	Pinout Description	20
CPU		Dual Operational Amplifier	233
ALU	39	E	
Control Registers	38	Electrical Characteristics	
Core Registers	36	Absolute Maximum Ratings	265
Programmer's Model	35	Thermal Operating Conditions	268
CTMU		Thermal Packaging	268
Measuring Capacitance	241	Equations	
Measuring Time	242	A/D Conversion Clock Period	223
Pulse Generation and Delay	243	UARTx Baud Rate with BRGH = 0	174
Customer Change Notification Service	332	UARTx Baud Rate with BRGH = 1	174
Customer Notification Service	332	Errata	11
Customer Support	332	Examples	
D		Baud Rate Error Calculation (BRGH = 0)	174
Data EEPROM Memory	73	F	
Erasing	76	Flash Program Memory	
Operations	75	Control Registers	68
Programming		Enhanced ICSP Operation	68
Bulk Erase	77	Programming Algorithm	70
Reading Data EEPROM	78	Programming Operations	68
Single-Word Write	77	RTSP Operation	68
Programming Control Registers		Table Instructions	67
NVMADR(U)	75	G	
NVMCON	73	Getting Started Guidelines	29
NVMKEY	73	External Oscillator Pins	33
Data Memory		ICSP Pins	32
Address Space	43	Master Clear ($\overline{\text{MCLR}}$) Pin	30
Width	43	Power Supply Pins	30
Near Data Space	44	Unused I/Os	33
Organization, Alignment	44	Voltage Regulator Pin (VCAP)	31
SFR Space	44	H	
Software Stack	63	High/Low-Voltage Detect (HLVD)	207
Data Space		I	
Memory Map	43	I/O Ports	
DC Characteristics		Analog Port Pins Configuration	138
BOR Trip Points	269	Analog Selection Registers	138
Comparator	276	Input Change Notification	140
CTMU Current Source	277	Open-Drain Configuration	138
Data EEPROM Memory	276	Parallel (PIO)	137
High/Low-Voltage Detect	269	In-Circuit Debugger	259
I/O Pin Input Specifications	274	In-Circuit Serial Programming (ICSP)	259
I/O Pin Output Specifications	275	Inter-Integrated Circuit. See I ² C.	
Idle Current (I _{IDLE})	271	Internet Address	332
Internal Voltage Regulator	277	Interrupts	
Operating Current (I _{DD})	270	Alternate Interrupt Vector Table (AIVT)	85
Operational Amplifier	278	Control and Status Registers	88
Power-Down Current (I _{PD})	272	Implemented Vectors	87
Program Memory	275	Interrupt Vector Table (IVT)	85
Temperature and Voltage Specifications	268	Reset Sequence	85
Demo/Development Boards, Evaluation and		Setup Procedures	119
Starter Kits	264	Trap Vectors	87
Development Support	261	Vector Table	86
Third-Party Tools	264		
Device Features			
PIC24F16KM104 Family	16		
PIC24F16KM204 Family	15		
PIC24FV16KM104 Family	18		
PIC24FV16KM204 Family	17		