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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km102t-i-ml

PIC24FV16KM204 FAMILY

Device	Pins	Memory			Voltage Range (V)	Peripherals											ICD BRKPT
		Flash Program (bytes)	SRAM (bytes)	EE Data (bytes)		16-Bit Timer	16-Bit MCCP/SCCP	MSSP	UART	12-Bit A/D Channels	8-Bit DAC	Op Amp	Comparators	CTMU	RTCC	CLC	
5V Devices																	
PIC24FV16KM204	44	16K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24FV16KM202	28	16K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24FV08KM204	44	8K	2K	512	2.0-5.5	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24FV08KM202	28	8K	2K	512	2.0-5.5	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24FV16KM104	44	16K	1K	512	2.0-5.5	1	1/1	1	1	22	—	—	1	Yes	—	1	3
PIC24FV16KM102	28	16K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24FV08KM102	28	8K	1K	512	2.0-5.5	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24FV08KM101	20	8K	1K	512	2.0-5.5	1	1/1	1	1	16	—	—	1	Yes	—	1	3
3V Devices																	
PIC24F16KM204	44	16K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24F16KM202	28	16K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24F08KM204	44	8K	2K	512	1.8-3.6	1	3/2	2	2	22	2	2	3	Yes	Yes	2	3
PIC24F08KM202	28	8K	2K	512	1.8-3.6	1	3/2	2	2	19	2	2	3	Yes	Yes	2	3
PIC24F16KM104	44	16K	1K	512	1.8-3.6	1	1/1	1	1	22	—	—	1	Yes	—	1	3
PIC24F16KM102	28	16K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24F08KM102	28	8K	1K	512	1.8-3.6	1	1/1	1	1	19	—	—	1	Yes	—	1	3
PIC24F08KM101	20	8K	1K	512	1.8-3.6	1	1/1	1	1	16	—	—	1	Yes	—	1	3

PIC24FV16KM204 FAMILY

Peripheral Features

- High-Current Sink/Source, 18 mA/18 mA All Ports
- Independent Ultra Low-Power, 32 kHz Timer Oscillator
- Up to Two Master Synchronous Serial Ports (MSSPs) with SPI and I²C™ modes:
 - In SPI mode:
 - User-configurable SCKx and SDOx pin outputs
 - Daisy-chaining of SPI slave devices
 - In I²C mode:
 - Serial clock synchronization (clock stretching)
 - Bus collision detection and will arbitrate accordingly
 - Support for 16-bit read/write interface
- Up to Two Enhanced Addressable UARTs:
 - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect, Break character support)
 - High and low speed (SCI)
 - IrDA® mode (hardware encoder/decoder function)
- Two External Interrupt Pins
- Hardware Real-Time Clock and Calendar (RTCC)
- Configurable Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLC)
- Up to Two Single Output Capture/Compare/PWM (SCCP) modules and up to Three Multiple Output Capture/Compare/PWM (MCCP) modules

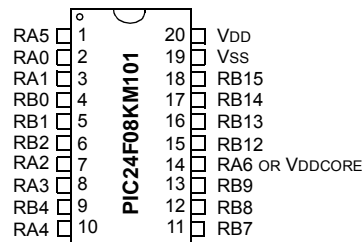
Special Microcontroller Features

- Wide Operating Voltage Range Options:
 - 1.8V to 3.6V (PIC24F devices)
 - 2.0V to 5.0V (PIC24FV devices)
- Selectable Power Management modes:
 - Idle: CPU shuts down, allowing for significant power reduction
 - Sleep: CPU and peripherals shut down for substantial power reduction and fast wake-up
 - Retention Sleep mode: PIC24FV devices can enter Sleep mode, employing the Retention Regulator, further reducing power consumption
 - Doze: CPU can run at a lower frequency than peripherals, a user-programmable feature
 - Alternate Clock modes allow on-the-fly switching to a lower clock speed for selective power reduction
- Fail-Safe Clock Monitor:
 - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Ultra Low-Power Wake-up Pin Provides an External Trigger for Wake from Sleep
- 10,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- 100,000 Erase/Write Cycle Endurance Data EEPROM, Typical
- Flash and Data EEPROM Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its Own On-Chip RC Oscillator for Reliable Operation
- On-Chip Regulator for 5V Operation
- Selectable Windowed WDT Feature
- Selectable Oscillator Options including:
 - 4x Phase Locked Loop (PLL)
- 8 MHz (FRC) Internal RC Oscillator:
 - HS/EC, High-Speed Crystal/Resonator Oscillator or External Clock
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) – via Two Pins
- In-Circuit Debugging
- Programmable High/Low-Voltage Detect (HLVD) module
- Programmable Brown-out Reset (BOR):
 - Software enable feature
 - Configurable shutdown in Sleep
 - Auto-configures power mode and sensitivity based on device operating speed
 - LPBOR available for re-arming of the POR

PIC24FV16KM204 FAMILY

Pin Diagrams

20-Pin PDIP/SSOP/SOIC



Pin	Pin Features	
	PIC24F08KM101	PIC24FVKM08KM101
1	MCLR/VPP/RA5	
2	PGEC2/CVREF+/VREF+/AN0/CN2/RA0	
3	PGED2/CVREF-/VREF-/AN1/CN3/RA1	
4	PGED1/AN2/CTCMP/ULPWU/C1IND/OC2A/CN4/RB0	
5	PGEC1/AN3/C1INC/CTED12/CN5/RB1	
6	AN4/U1RX/TCKIB/CTED13/CN6/RB2	
7	OSCI/CLKI/AN13/C1INB/CN30/RA2	
8	OSCO/CLKO/AN14/C1INA/CN29/RA3	
9	PGED3/SOSCI/AN15/CLCINA/CN1/RB4	
10	PGEC3/SOSCO/SCLKI/AN16/PWRLCLK/CLCINB/CN0/RA4	
11	AN19/U1TX/CTED1/INT0/CN23/RB7	AN19/U1TX/IC1/OC1A/CTED1/INT0/CN23/RB7
12	AN20/SCL1/U1CTS/OC1B/CTED10/CN22/RB8	
13	AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/CLC1O/CTED4/CN21/RB9	
14	IC1/OC1A/INT2/CN8/RA6	VCAP OR VDDCORE
15	AN12/HLVDIN/SCK1/OC1C/CTED2/CN14/RB12	AN12/HLVDIN/SCK1/OC1C/CTED2/INT2/CN14/RB12
16	AN11/SDO1/OCFB/OC1D/CTPLS/CN13/RB13	
17	CVREF/AN10/SDI1/C1OUT/OCFA/CTED5/INT1/CN12/RB14	
18	AN9/REFO/SS1/TCKIA/CTED6/CN11/RB15	
19	VSS/AVSS	
20	VDD/AVDD	

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
MCLR	1	1	26	18	19	1	1	26	18	19	I	ST	Master Clear (Device Reset) Input (active-low)
OA1INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 1 Input A
OA1INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 1 Input B
OA1INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 1 Input C
OA1IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 1 Input D
OA1OUT	—	7	4	24	26	—	7	4	24	26	O	ANA	Op Amp 1 Analog Output
OA2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 2 Input A
OA2INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 2 Input B
OA2INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 2 Input C
OA2IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 2 Input D
OA2OUT	—	26	23	15	16	—	26	23	15	16	O	ANA	Op Amp 2 Analog Output
OC1A	14	20	17	7	7	11	16	13	43	47	O	—	MCCP1 Output Compare A
OC1B	12	17	14	44	48	12	17	14	44	48	O	—	MCCP1 Output Compare B
OC1C	15	21	18	8	9	15	21	18	8	9	O	—	MCCP1 Output Compare C
OC1D	16	24	21	11	12	16	24	21	11	12	O	—	MCCP1 Output Compare D
OC1E	—	14	11	41	45	—	14	11	41	45	O	—	MCCP1 Output Compare E
OC1F	—	15	12	42	46	—	15	12	42	46	O	—	MCCP1 Output Compare F
OC2A	4	22	19	9	10	4	22	19	9	10	O	—	MCCP2 Output Compare A
OC2B	—	23	20	10	11	—	23	20	10	11	O	—	MCCP2 Output Compare B
OC2C	—	—	—	2	2	—	—	—	2	2	O	—	MCCP2 Output Compare C
OC2D	—	—	—	3	3	—	—	—	3	3	O	—	MCCP2 Output Compare D
OC2E	—	—	—	4	4	—	—	—	4	4	O	—	MCCP2 Output Compare E
OC2F	—	—	—	5	5	—	—	—	5	5	O	—	MCCP2 Output Compare F
OC3A	—	21	18	12	13	—	21	18	12	13	O	—	MCCP3 Output Compare A
OC3B	—	24	21	13	14	—	24	21	13	14	O	—	MCCP3 Output Compare B
OC4	—	18	15	1	1	—	18	15	1	1	O	—	SCCP4 Output Compare
OC5	—	19	16	6	6	—	19	16	6	6	O	—	SCCP5 Output Compare
OCFA	17	25	22	14	15	17	25	22	14	15	I	ST	MCCP/SCCP Output Compare Fault Input A
OCFB	16	24	21	32	35	16	24	21	32	35	I	ST	MCCP/SCCP Output Compare Fault Input B

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I²C™ = I²C/SMBus input buffer

TABLE 4-10: M CCP3 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP3CON1L ⁽¹⁾	188h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP3CON1H ⁽¹⁾	18Ah	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP3CON2L ⁽¹⁾	18Ch	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP3CON2H ⁽¹⁾	18Eh	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP3CON3L ⁽¹⁾	190h	—	—	—	—	—	—	—	—	—	—	DT5	DT4	DT3	DT2	DT1	DT0	0000
CCP3CON3H ⁽¹⁾	192h	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP3STAT ⁽¹⁾	194h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP3TMRL ⁽¹⁾	198h	MCCP3 Time Base Register Low Word																0000
CCP3TMRH ⁽¹⁾	19Ah	MCCP3 Time Base Register High Word																0000
CCP3PRL ⁽¹⁾	19Ch	MCCP3 Time Base Period Register Low Word																FFFF
CCP3PRH ⁽¹⁾	19Eh	MCCP3 Time Base Period Register High Word																FFFF
CCP3RAL ⁽¹⁾	1A0h	Output Compare 3 Data Word A																0000
CCP3RBL ⁽¹⁾	1A4h	Output Compare 3 Data Word B																0000
CCP3BUFL ⁽¹⁾	1A8h	Input Capture 3 Data Buffer Low Word																0000
CCP3BUFH ⁽¹⁾	1AAh	Input Capture 3 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

PIC24FV16KM204 FAMILY

6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__((space(eedata))) eeData = 0x1234;
/*-----
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the erase
-----*/
unsigned int offset;

// Set up NVMCON to erase one word of data EEPROM
NVMCON = 0x4058;

// Set up a pointer to the EEPROM location to be erased
TBLPAG = __builtin_tblpage(&eeData);           // Initialize EE Data page pointer
offset = __builtin_tbloffset(&eeData);          // Initizlize lower word of address
__builtin_tblwtl(offset, 0);                     // Write EEPROM data to write latch

asm volatile ("disi #5");                        // Disable Interrupts For 5 Instructions
__builtin_write_NVM();                           // Issue Unlock Sequence & Start Write Cycle
while(NVMCONbits.WR==1);                        // Optional: Poll WR bit to wait for
// write sequence to complete
```

PIC24FV16KM204 FAMILY

REGISTER 8-30: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

PIC24FV16KM204 FAMILY

REGISTER 8-32: IPC19: INTERRUPT PRIORITY CONTROL REGISTER 19

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	DAC2IP2	DAC2IP1	DAC2IP0	—	DAC1IP2	DAC1IP1	DAC1IP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **DAC2IP<2:0>:** Digital-to-Analog Converter 2 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DAC1IP<2:0>:** Digital-to-Analog Converter 1 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **CTMUIP<2:0>:** CTMU Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

PIC24FV16KM204 FAMILY

9.1 CPU Clocking Scheme

The system clock source can be provided by one of four sources:

- Primary Oscillator (POSC) on the OSC1 and OSCO pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins

The PIC24FXXXXX family devices consist of two types of secondary oscillator:

- High-Power Secondary Oscillator
- Low-Power Secondary Oscillator

These can be selected by using the SOSSEL (FOSC<5>) bit.

- Fast Internal RC (FRC) Oscillator:
 - 8 MHz FRC Oscillator
 - 500 kHz Lower Power FRC Oscillator
- Low-Power Internal RC (LPRC) Oscillator with two modes:
 - High-Power/High-Accuracy mode
 - Low-Power/Low-Accuracy mode

The Primary Oscillator and 8 MHz FRC sources have the option of using the internal 4x PLL. The frequency of the FRC clock source can optionally be reduced by the programmable clock divider. The selected clock source generates the processor and peripheral clock sources.

The processor clock source is divided by two to produce the internal instruction cycle clock, Fcy. In this document, the instruction cycle clock is also denoted by Fosc/2. The internal instruction cycle clock, Fosc/2, can be provided on the OSCO I/O pin for some operating modes of the Primary Oscillator.

9.2 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset (POR) event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory (for more information, see **Section 25.1 “Configuration Bits”**). The Primary Oscillator Configuration bits, POSCMD<1:0> (FOSC<1:0>), and the Initial Oscillator Select Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), select the oscillator source that is used at a POR. The FRC Primary Oscillator with Postscaler (FRCDIV) is the default (unprogrammed) selection. The Secondary Oscillator, or one of the internal oscillators, may be chosen by programming these bit locations. The EC mode Frequency Range Configuration bits, POSCFREQ<1:0> (FOSC<4:3>), optimize power consumption when running in EC mode. The default configuration is “frequency range is greater than 8 MHz”.

The Configuration bits allow users to choose between the various clock modes, shown in Table 9-1.

9.2.1 CLOCK SWITCHING MODE CONFIGURATION BITS

The FCKSM<1:0> Configuration bits (FOSC<7:6>) are used jointly to configure device clock switching and the FSCM. Clock switching is enabled only when FCKSM1 is programmed ('0'). The FSCM is enabled only when FCKSM<1:0> are both programmed ('00').

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	Notes
8 MHz FRC Oscillator with Postscaler (FRCDIV)	Internal	11	111	1, 2
500 kHz FRC Oscillator with Postscaler (LPFRCDIV)	Internal	11	110	1
Low-Power RC Oscillator (LPRC)	Internal	11	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	00	100	1
Primary Oscillator (HS) with PLL Module (HSPLL)	Primary	10	011	
Primary Oscillator (EC) with PLL Module (ECPLL)	Primary	00	011	
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	
8 MHz FRC Oscillator with PLL Module (FRCPLL)	Internal	11	001	1
8 MHz FRC Oscillator (FRC)	Internal	11	000	1

Note 1: The OSCO pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

11.0 I/O PORTS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the I/O ports, refer to the “PIC24F Family Reference Manual”, “I/O Ports with Peripheral Pin Select (PPS)” (DS39711). Note that the PIC24FV16KM204 family devices do not support Peripheral Pin Select features.

All of the device pins (except VDD and VSS) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through”, in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

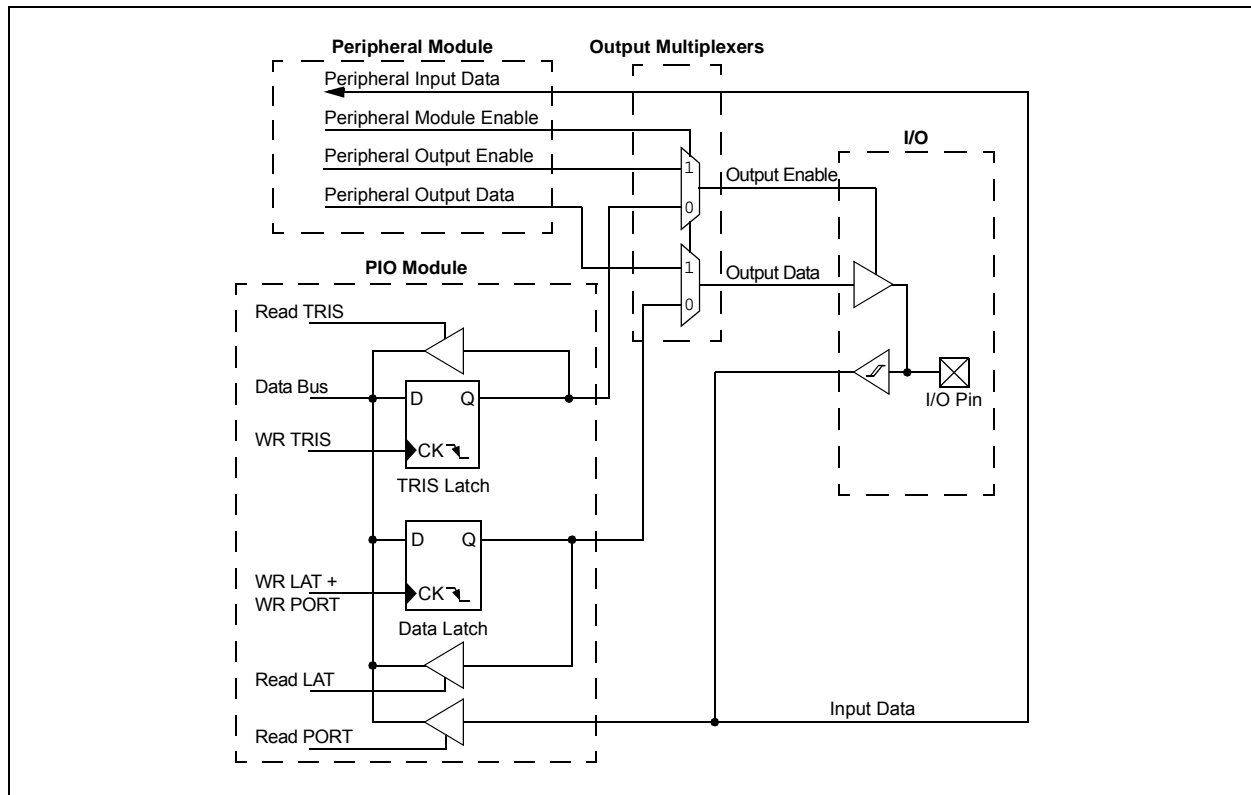
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Data Latch register (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



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REGISTER 13-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OENSYNC	—	OCFEN ⁽¹⁾	OCEEN ⁽¹⁾	OCDEN ⁽¹⁾	OCCEN ⁽¹⁾	OCBEN ⁽¹⁾	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit

1 = Update by output enable bits occurs on the next Time Base Reset or rollover

0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **OC<F:A>EN:** Output Enable/Steering Control bits⁽¹⁾

1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal

0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits

11 = Reserved

10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)

01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)

00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits

11 = Input capture or output compare event; no signal in Timer mode

10 = Signal output is defined by module operating mode (see Table 13-5)

01 = Time base rollover event (all modes)

00 = Disabled

bit 2-0 **ICS<2:0>:** Input Capture Source Select bits

111 = Unused

110 = CLC2 output

101 = CLC1 output

100 = Unused

011 = Comparator 3 output

010 = Comparator 2 output

001 = Comparator 1 output

000 = Input Capture x (ICx) I/O pin

Note 1: OCFEN through OCBEN (bits<13:9>) are implemented in MCCPx modules only.

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16.2.4 RTCC CONTROL REGISTERS

REGISTER 16-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
 1 = RTCC module is enabled
 0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
 1 = RTCVALH and RTCVALL registers can be written to by the user
 0 = RTCVALH and RTCVALL registers are locked out from being written to by the user
- bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
 1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
 0 = RTCVALH, RTCVALL or ALCFGRPT registers can be read without concern over a rollover ripple
- bit 11 **HALFSEC:** Half Second Status bit⁽³⁾
 1 = Second half period of a second
 0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
 1 = RTCC output is enabled
 0 = RTCC output is disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
 Points to the corresponding RTCC Value registers when reading the RTCVALH and RTCVALL registers. The RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
 RTCVAL<15:8>:
 00 = MINUTES
 01 = WEEKDAY
 10 = MONTH
 11 = Reserved
 RTCVAL<7:0>:
 00 = SECONDS
 01 = HOURS
 10 = DAY
 11 = YEAR

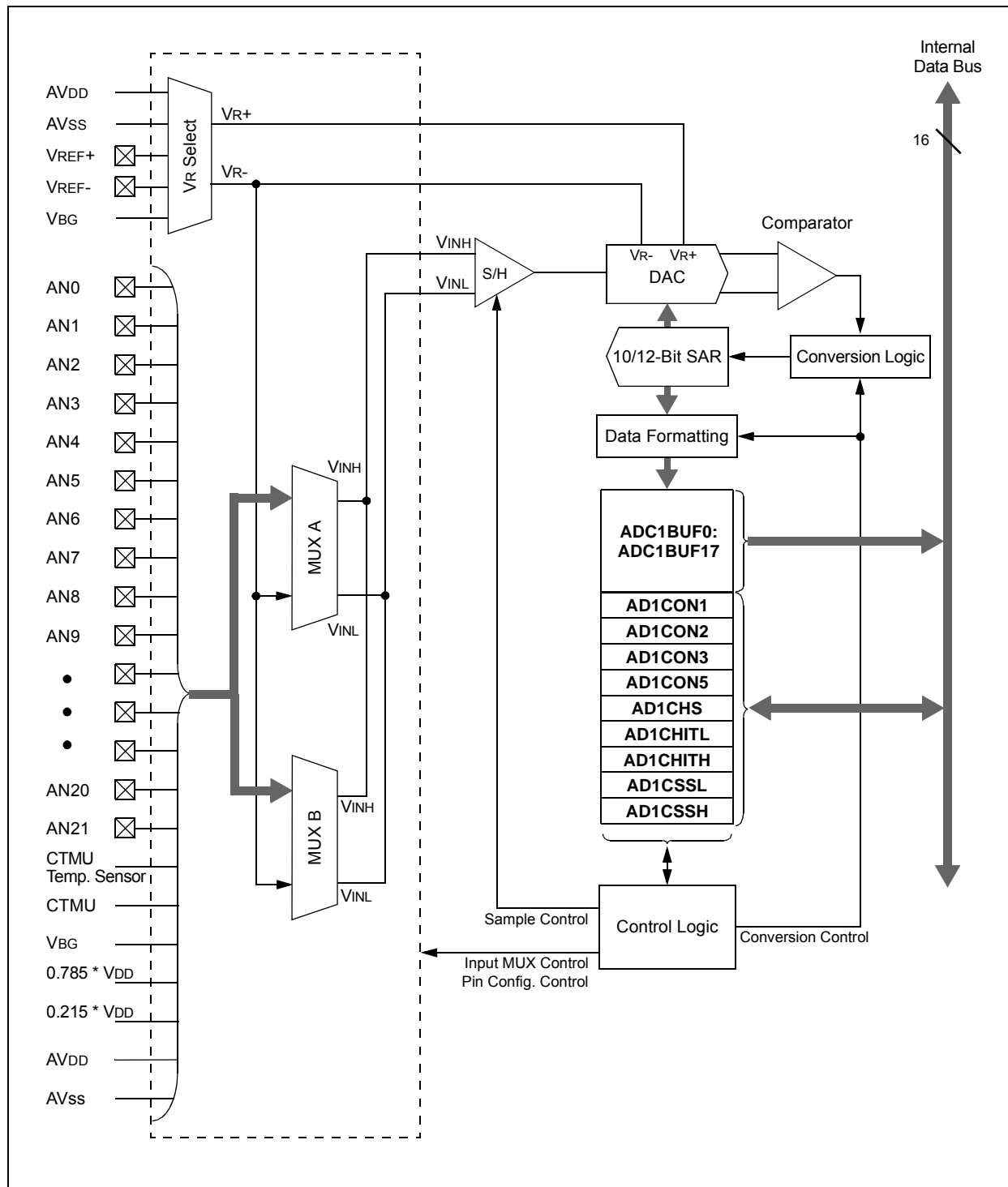
Note 1: The RCFGAL register is only affected by a POR.

2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

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FIGURE 19-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM



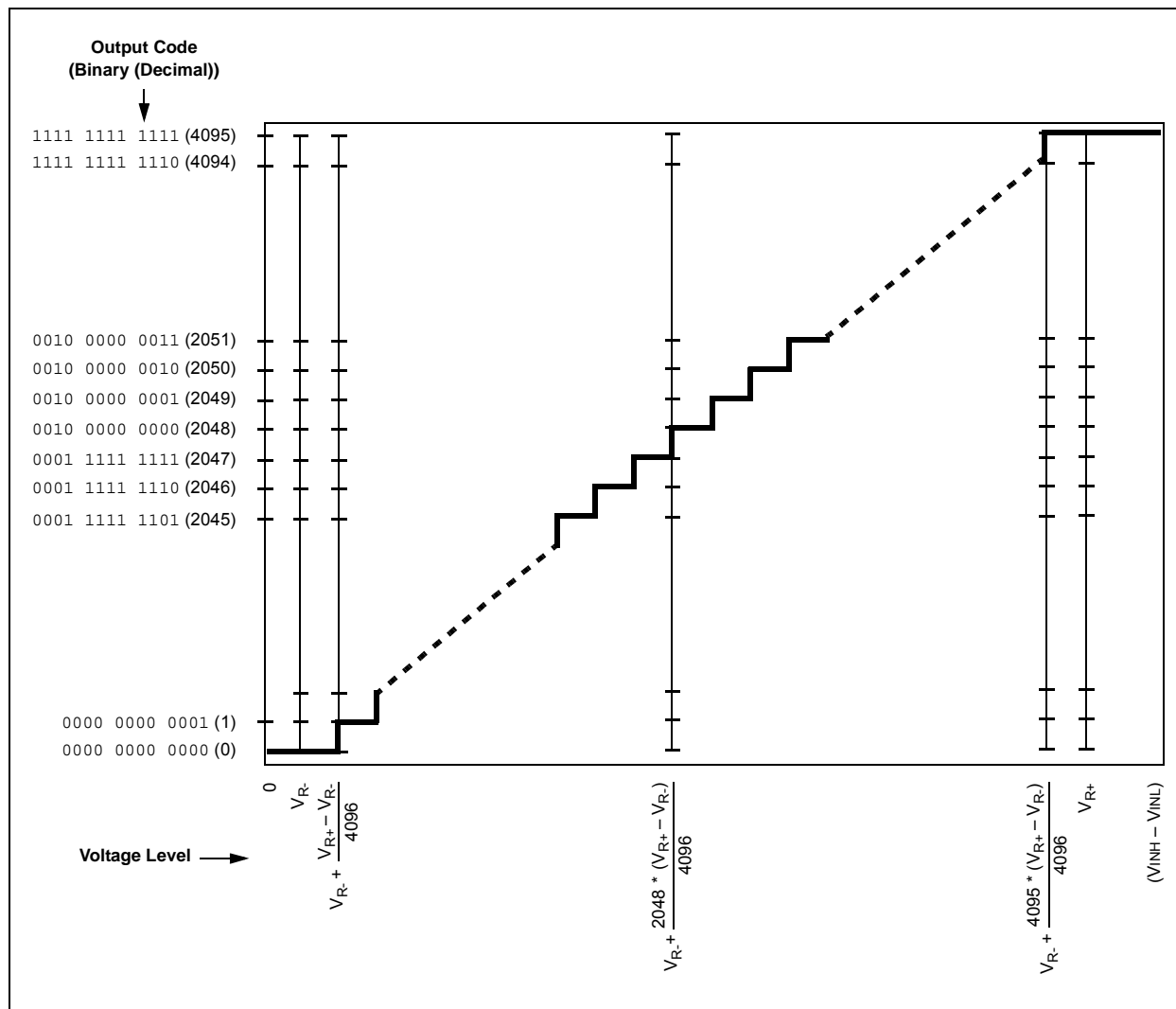
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19.3 Transfer Function

The transfer functions of the A/D Converter in 12-bit resolution are shown in Figure 19-3. The difference of the input voltages ($V_{INH} - V_{INL}$) is compared to the reference ($(V_{R+}) - (V_{R-})$).

- The first code transition occurs when the input voltage is $((V_{R+}) - (V_{R-}))/4096$ or 1.0 LSB.
- The '0000 0000 0001' code is centered at $V_{R-} + (1.5 * ((V_{R+}) - (V_{R-}))/4096)$.
- The '0010 0000 0000' code is centered at $V_{REFL} + (2048.5 * ((V_{R+}) - (V_{R-}))/4096)$.
- An input voltage less than $V_{R-} + (((V_{R-}) - (V_{R-}))/4096)$ converts as '0000 0000 0000'.
- An input voltage greater than $(V_{R-}) + (4095 * ((V_{R+}) - (V_{R-}))/4096)$ converts as '1111 1111 1111'.

FIGURE 19-3: 12-BIT A/D TRANSFER FUNCTION



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**TABLE 19-4: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES:
10-BIT FRACTIONAL FORMATS**

VIN/VREF	10-Bit Differential Output Code (11-bit result)	16-Bit Fractional Format/ Equivalent Decimal Value		16-Bit Signed Fractional Format/ Equivalent Decimal Value	
+1023/1024	011 1111 1111	1111 1111 1100 0000	0.999	0111 1111 1110 0000	0.999
+1022/1024	011 1111 1110	1111 1111 1000 0000	0.998	0111 1111 1000 0000	0.998
...					
+1/1024	000 0000 0001	0000 0000 0100 0000	0.001	0000 0000 0010 0000	0.001
0/1024	000 0000 0000	0000 0000 0000 0000	0.000	0000 0000 0000 0000	0.000
-1/1024	101 1111 1111	0000 0000 0000 0000	0.000	1111 1111 1110 0000	-0.001
...					
-1023/1024	100 0000 0001	0000 0000 0000 0000	0.000	1000 0000 0010 0000	-0.999
-1024/1024	100 0000 0000	0000 0000 0000 0000	0.000	1000 0000 0000 0000	-1.000

22.0 COMPARATOR MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator module, refer to the “PIC24F Family Reference Manual”, “**Scalable Comparator Module**” (DS39734).

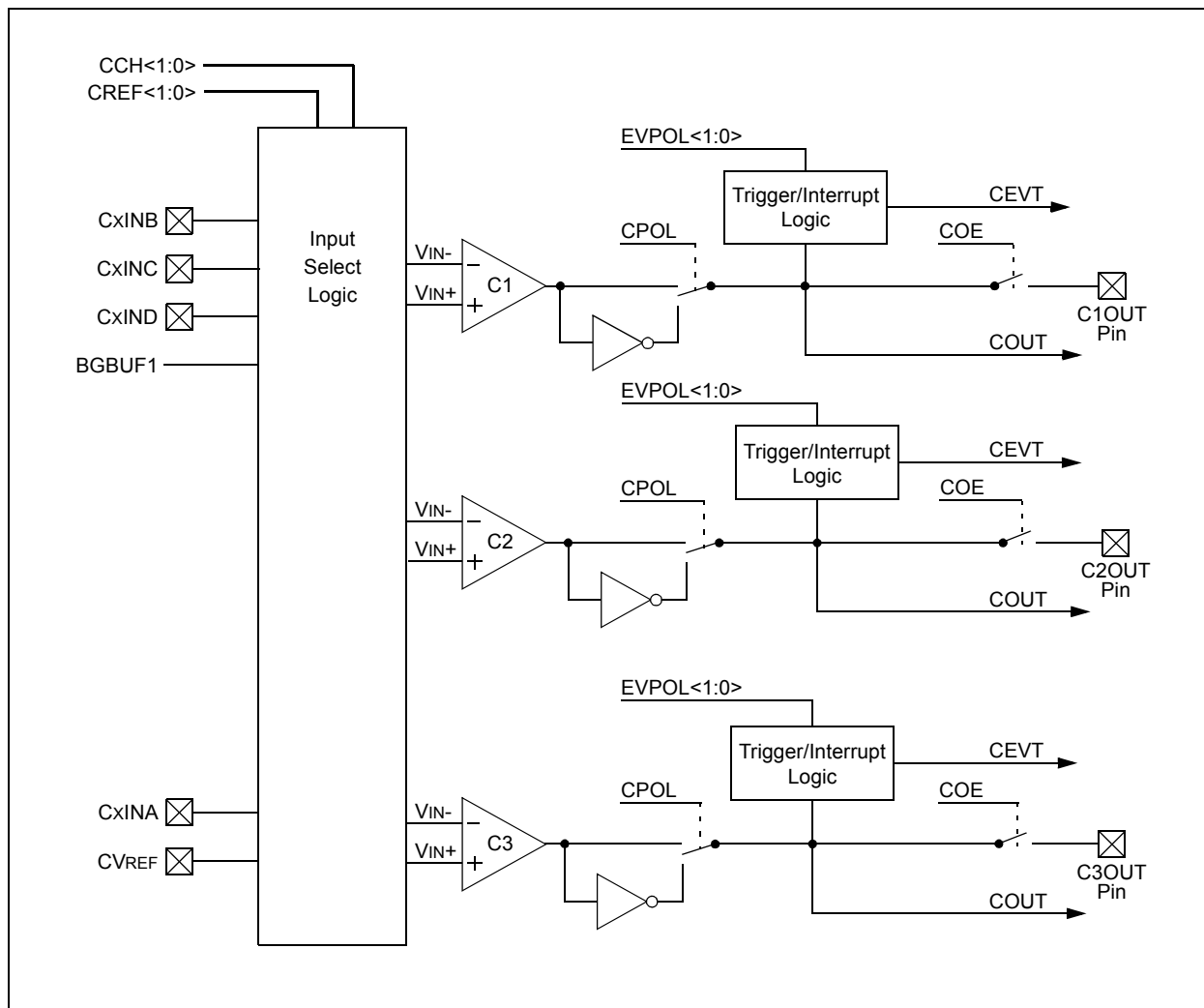
The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as a voltage reference input from either the Internal Band Gap Buffer 1 (BGBUF1) or the comparator voltage reference generator.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 22-1. Diagrams of the possible individual comparator configurations are shown in Figure 22-2.

Each comparator has its own control register, CMxCON (Register 22-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 22-2).

FIGURE 22-1: COMPARATOR x MODULE BLOCK DIAGRAM



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26.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

26.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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TABLE 27-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended			
Parameter No.	Device	Typical ⁽¹⁾	Max	Units	Conditions
Module Differential Current (ΔI_{PD})⁽³⁾					
DC71	PIC24FV16KMXXX	0.50	—	μA	2.0V
		0.70	1.5	μA	5.0V
	PIC24F16KMXXX	0.50	—	μA	1.8V
		0.70	1.5	μA	3.3V
DC72	PIC24FV16KMXXX	0.80	—	μA	2.0V
		1.50	2.0	μA	5.0V
	PIC24F16KMXXX	0.70	—	μA	1.8V
		1.0	1.5	μA	3.3V
DC75	PIC24FV16KMXXX	5.4	—	μA	2.0V
		8.1	14.0	μA	5.0V
	PIC24F16KMXXX	4.9	—	μA	1.8V
		7.5	14.0	μA	3.3V
DC76	PIC24FV16KMXXX	5.6	—	μA	2.0V
		6.5	11.2	μA	5.0V
	PIC24F16KMXXX	5.6	—	μA	1.8V
		6.0	11.2	μA	3.3V
DC78	PIC24FV16KMXXX	0.03	—	μA	2.0V
		0.05	0.3	μA	5.0V
	PIC24F16KMXXX	0.03	—	μA	1.8V
		0.05	0.3	μA	3.3V

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: Data in the Typical column is at 3.3V, +25°C (PIC24F16KMXXX) or 5.0V, +25°C (PIC24FV16KMXXX) unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as outputs and set low. PMSLP is set to '0' and WDT, etc., are all switched off.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

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FIGURE 27-17: MSSPx I²C™ BUS START/STOP BITS TIMING WAVEFORMS

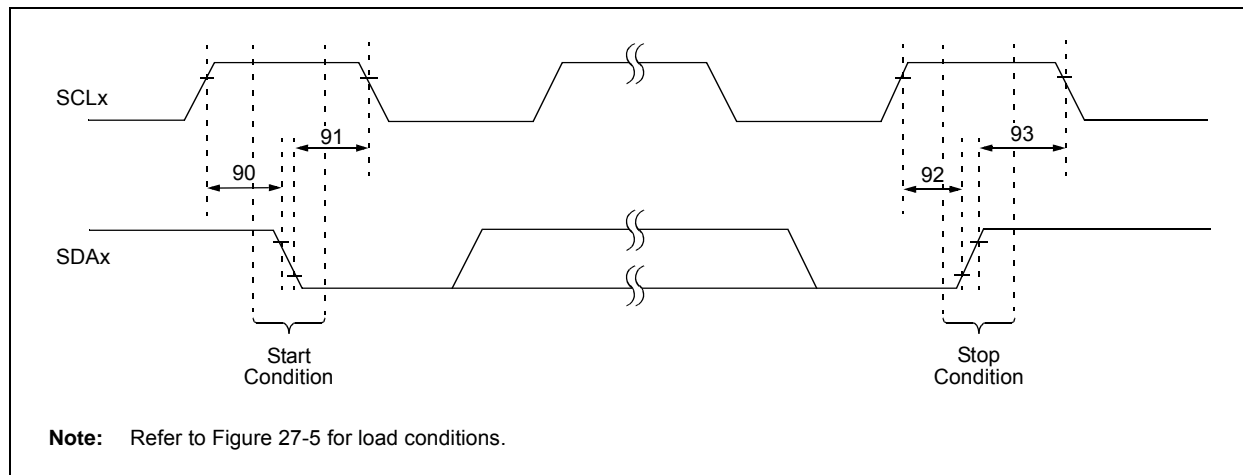


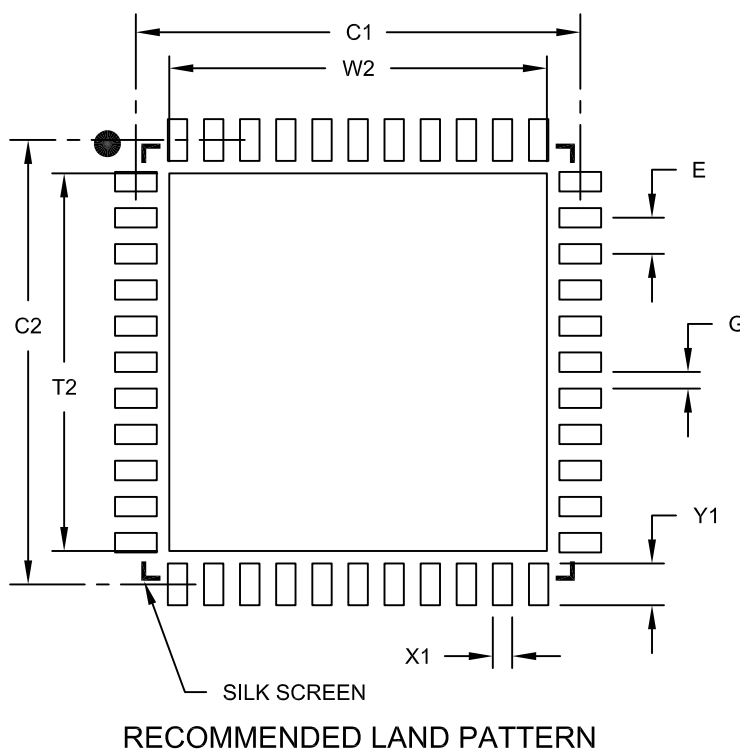
TABLE 27-35: I²C™ BUS START/STOP BITS REQUIREMENTS (MASTER MODE)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	$2(T_{osc})(BRG + 1)$	—	ns Only relevant for Repeated Start condition
			400 kHz mode	$2(T_{osc})(BRG + 1)$	—	
91	THD:STA	Start Condition Hold Time	100 kHz mode	$2(T_{osc})(BRG + 1)$	—	ns After this period, the first clock pulse is generated
			400 kHz mode	$2(T_{osc})(BRG + 1)$	—	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	$2(T_{osc})(BRG + 1)$	—	ns
			400 kHz mode	$2(T_{osc})(BRG + 1)$	—	
93	THD:STO	Stop Condition Hold Time	100 kHz mode	$2(T_{osc})(BRG + 1)$	—	ns
			400 kHz mode	$2(T_{osc})(BRG + 1)$	—	

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B