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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km102t-i-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km102t-i-ss</a>

# PIC24FV16KM204 FAMILY

## Peripheral Features

- High-Current Sink/Source, 18 mA/18 mA All Ports
- Independent Ultra Low-Power, 32 kHz Timer Oscillator
- Up to Two Master Synchronous Serial Ports (MSSPs) with SPI and I<sup>2</sup>C™ modes:
  - In SPI mode:
    - User-configurable SCKx and SDOx pin outputs
    - Daisy-chaining of SPI slave devices
  - In I<sup>2</sup>C mode:
    - Serial clock synchronization (clock stretching)
    - Bus collision detection and will arbitrate accordingly
    - Support for 16-bit read/write interface
- Up to Two Enhanced Addressable UARTs:
  - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect, Break character support)
  - High and low speed (SCI)
  - IrDA® mode (hardware encoder/decoder function)
- Two External Interrupt Pins
- Hardware Real-Time Clock and Calendar (RTCC)
- Configurable Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLC)
- Up to Two Single Output Capture/Compare/PWM (SCCP) modules and up to Three Multiple Output Capture/Compare/PWM (MCCP) modules

## Special Microcontroller Features

- Wide Operating Voltage Range Options:
  - 1.8V to 3.6V (PIC24F devices)
  - 2.0V to 5.0V (PIC24FV devices)
- Selectable Power Management modes:
  - Idle: CPU shuts down, allowing for significant power reduction
  - Sleep: CPU and peripherals shut down for substantial power reduction and fast wake-up
  - Retention Sleep mode: PIC24FV devices can enter Sleep mode, employing the Retention Regulator, further reducing power consumption
  - Doze: CPU can run at a lower frequency than peripherals, a user-programmable feature
  - Alternate Clock modes allow on-the-fly switching to a lower clock speed for selective power reduction
- Fail-Safe Clock Monitor:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Ultra Low-Power Wake-up Pin Provides an External Trigger for Wake from Sleep
- 10,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- 100,000 Erase/Write Cycle Endurance Data EEPROM, Typical
- Flash and Data EEPROM Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its Own On-Chip RC Oscillator for Reliable Operation
- On-Chip Regulator for 5V Operation
- Selectable Windowed WDT Feature
- Selectable Oscillator Options including:
  - 4x Phase Locked Loop (PLL)
- 8 MHz (FRC) Internal RC Oscillator:
  - HS/EC, High-Speed Crystal/Resonator Oscillator or External Clock
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) – via Two Pins
- In-Circuit Debugging
- Programmable High/Low-Voltage Detect (HLVD) module
- Programmable Brown-out Reset (BOR):
  - Software enable feature
  - Configurable shutdown in Sleep
  - Auto-configures power mode and sensitivity based on device operating speed
  - LPBOR available for re-arming of the POR

# PIC24FV16KM204 FAMILY

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## 1.1.4 EASY MIGRATION

The PIC24FV16KM204 family devices have two variants. The KM20X variant provides the full feature set of the device, while the KM10X offers a reduced peripheral set, allowing for the balance of features and cost (refer to Table 1-1). Both variants allow for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, different die variants, or even moving from 20-pin or 28-pin devices to 44-pin/48-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple to the powerful and complex, yet still selecting a Microchip device.

## 1.2 Other Special Features

- **Communications:** The PIC24FV16KM204 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an MSSP module which implements both SPI and I<sup>2</sup>C™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- **Analog Features:** Select members of the PIC24FV16KM204 family include two 8-bit Digital-to-Analog Converters which offer support in Idle mode, and left and right justified input data, as well as up to two operational amplifiers with selectable power and speed modes.
- **Real-Time Clock/Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep, to reduce power, or in Active mode to improve throughput.
- **Charge Time Measurement Unit (CTMU) Interface:** The PIC24FV16KM204 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing, and also for precision time measurement and pulse generation. The CTMU can also be connected to the operational amplifiers to provide active guarding, which provides increased robustness in the presence of noise in capacitive touch applications.

## 1.3 Details on Individual Family Members

Devices in the PIC24FV16KM204 family are available in 20-pin, 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

Members of the PIC24FV16KM204 family are available as both standard and high-voltage devices. High-voltage devices, designated with an “FV” in the part number (such as PIC24FV16KM204), accommodate an operating VDD range of 2.0V to 5.5V and have an on-board voltage regulator that powers the core. Peripherals operate at VDD.

Standard devices, designated by “F” (such as PIC24F16KM204), function over a lower VDD range of 1.8V to 3.6V. These parts do not have an internal regulator, and both the core and peripherals operate directly from VDD.

The PIC24FV16KM204 family may be thought of as two different device groups, both offering slightly different sets of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The number of external analog channels available
- The number of Digital-to-Analog Converters
- The number of operational amplifiers
- The number of analog comparators
- The presence of a Real-Time Clock and Calendar (RTCC)
- The number and type of CCP modules (i.e., MCCP vs. SCCP)
- The number of serial communication modules (both MSSPs and UARTs)
- The number of Configurable Logic Cell (CLC) modules

The general differences between the different sub-families are shown in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FV16KM204 family devices, sorted by function, is provided in Table 1-5.

# PIC24FV16KM204 FAMILY

## 2.2 Power Supply Pins

### 2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1  $\mu\text{F}$  (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu\text{F}$  to 0.001  $\mu\text{F}$ . Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1  $\mu\text{F}$  in parallel with 0.001  $\mu\text{F}$ ).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

### 2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7  $\mu\text{F}$  to 47  $\mu\text{F}$ .

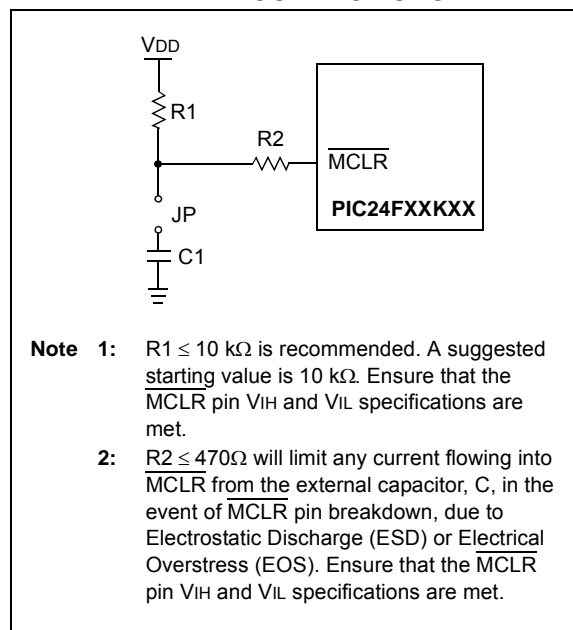
## 2.3 Master Clear ( $\overline{\text{MCLR}}$ ) Pin

The  $\overline{\text{MCLR}}$  pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels ( $V_{IH}$  and  $V_{IL}$ ) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the  $\overline{\text{MCLR}}$  pin should be placed within 0.25 inch (6 mm) of the pin.

**FIGURE 2-2: EXAMPLE OF  $\overline{\text{MCLR}}$  PIN CONNECTIONS**



**TABLE 4-15: UART1 REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	220h	UARTEN	—	USIDL	IREN	RTSMO	—	UEN1	UEN0	WAKE	LPBACK	ABAUO	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	222h	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	224h	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	226h	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	228h	Baud Rate Generator Prescaler																0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**TABLE 4-16: UART2 REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U2MODE <sup>(1)</sup>	230h	UARTEN	—	USIDL	IREN	RTSMO	—	UEN1	UEN0	WAKE	LPBACK	ABAUO	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA <sup>(1)</sup>	232h	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG <sup>(1)</sup>	234h	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG <sup>(1)</sup>	236h	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG <sup>(1)</sup>	238h	Baud Rate Generator Prescaler																0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These registers are available only on PIC24F(V)16KM2XX devices.

# PIC24FV16KM204 FAMILY

## 5.5.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time by erasing the programmable row. The general process is:

1. Read a row of program memory (32 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase a row (see Example 5-1):
  - a) Set the NVMOPx bits (NVMCON<5:0>) to '011000' to configure for row erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
  - b) Write the starting address of the block to be erased into the TBLPAG and W registers.
  - c) Write 55h to NVMKEY.
  - d) Write AAh to NVMKEY.
  - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 32 instructions from data RAM into the program memory buffers (see Example 5-1).
5. Write the program block to Flash memory:
  - a) Set the NVMOPx bits to '000100' to configure for row programming. Clear the ERASE bit and set the WREN bit.
  - b) Write 55h to NVMKEY.
  - c) Write AAh to NVMKEY.
  - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS, as displayed in Example 5-5.

### EXAMPLE 5-1: ERASING A PROGRAM MEMORY ROW – ASSEMBLY LANGUAGE CODE

```
; Set up NVMCON for row erase operation
    MOV    #0x4058, W0          ;
    MOV    W0, NVMCON           ; Initialize NVMCON
; Init pointer to row to be ERASED
    MOV    #tblpage(PROG_ADDR), W0 ;
    MOV    W0, TBLPAG           ; Initialize PM Page Boundary SFR
    MOV    #tbloffset(PROG_ADDR), W0 ; Initialize in-page EA[15:0] pointer
    TBLWTL W0, [W0]             ; Set base address of erase block
    DISI    #5                  ; Block all interrupts
                                ; for next 5 instructions

    MOV    #0x55, W0
    MOV    W0, NVMKEY           ; Write the 55 key
    MOV    #0xAA, W1
    MOV    W1, NVMKEY           ; Write the AA key
    BSET    NVMCON, #WR         ; Start the erase sequence
    NOP                                ; Insert two NOPs after the erase
    NOP                                ; command is asserted
```

### EXAMPLE 5-2: ERASING A PROGRAM MEMORY ROW – 'C' LANGUAGE CODE

```
// C example using MPLAB C30

int __attribute__((space(auto_psv))) progAddr = 0x1234; // Variable located in Pgm Memory, declared as a
                                                         // global variable

unsigned int offset;

//Set up pointer to the first memory location to be written

TBLPAG = __builtin_tblpage(&progAddr); // Initialize PM Page Boundary SFR
offset = __builtin_tbloffset(&progAddr); // Initialize lower word of address

__builtin_tblwtl(offset, 0x0000); // Set base address of erase block
                                   // with dummy latch write

NVMCON = 0x4058; // Initialize NVMCON

asm("DISI #5"); // Block all interrupts for next 5 instructions
__builtin_write_NVM(); // C30 function to perform unlock
                       // sequence and set WR
```

# PIC24FV16KM204 FAMILY

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## 6.4.3 READING THE DATA EEPROM

To read a word from data EEPROM, the Table Read instruction is used. Since the EEPROM array is only 16 bits wide, only the TBLRD instruction is needed. The read operation is performed by loading TBLPAG and WREG with the address of the EEPROM location, followed by a TBLRD instruction.

A typical read sequence, using the Table Pointer management (`builtin_tblpage` and `builtin_tbloffset`) and Table Read (`builtin_tblrld`) procedures from the C30 compiler library, is provided in Example 6-5.

Program Space Visibility (PSV) can also be used to read locations in the data EEPROM.

### EXAMPLE 6-5: READING THE DATA EEPROM USING THE TBLRD COMMAND

```
int __attribute__((space(eedata))) eeData = 0x1234;
int data;                                     // Data read from EEPROM
/*-----
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the read
-----
*/
    unsigned int offset;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);           // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);          // Initizlize lower word of address
    data = __builtin_tblrld(offset);                 // Write EEPROM data to write latch
```

# PIC24FV16KM204 FAMILY

## REGISTER 8-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCP5IP2	CCP5IP1	CCP5IP0
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7					bit 0		

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCP5IP<2:0>:** Capture/Compare 5 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled



# PIC24FV16KM204 FAMILY

## REGISTER 8-26: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP2	INT2IP1	INT2IP0	—	CCT4IP2	CCT4IP1	CCT4IP0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CCT4IP<2:0>:** Capture/Compare 4 Timer Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

# PIC24FV16KM204 FAMILY

## REGISTER 8-27: IPC10: INTERRUPT PRIORITY CONTROL REGISTER 10

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CCT5IP2	CCT5IP1	CCT5IP0	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CCT5IP<2:0>:** Capture/Compare 5 Timer Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

# PIC24FV16KM204 FAMILY

## REGISTER 8-30: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—
bit 7						bit 0	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

# PIC24FV16KM204 FAMILY

## REGISTER 8-31: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3

**Unimplemented:** Read as '0'

bit 2-0

**HLVDIP<2:0>:** High/Low-Voltage Detect Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

- 
- 
- 

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

# PIC24FV16KM204 FAMILY

## REGISTER 14-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE <sup>(1)</sup>	D/ $\overline{A}$	P	S	R/ $\overline{W}$	UA	BF
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **SMP:** Sample bit

SPI Master mode:

1 = Input data is sampled at the end of data output time

0 = Input data is sampled at the middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit<sup>(1)</sup>

1 = Transmit occurs on transition from active to Idle clock state

0 = Transmit occurs on transition from Idle to active clock state

bit 5 **D/ $\overline{A}$ :** Data/Address bit

Used in I<sup>2</sup>C™ mode only.

bit 4 **P:** Stop bit

Used in I<sup>2</sup>C mode only. This bit is cleared when the MSSPx module is disabled; SSPEN bit is cleared.

bit 3 **S:** Start bit

Used in I<sup>2</sup>C mode only.

bit 2 **R/ $\overline{W}$ :** Read/Write Information bit

Used in I<sup>2</sup>C mode only.

bit 1 **UA:** Update Address bit

Used in I<sup>2</sup>C mode only.

bit 0 **BF:** Buffer Full Status bit

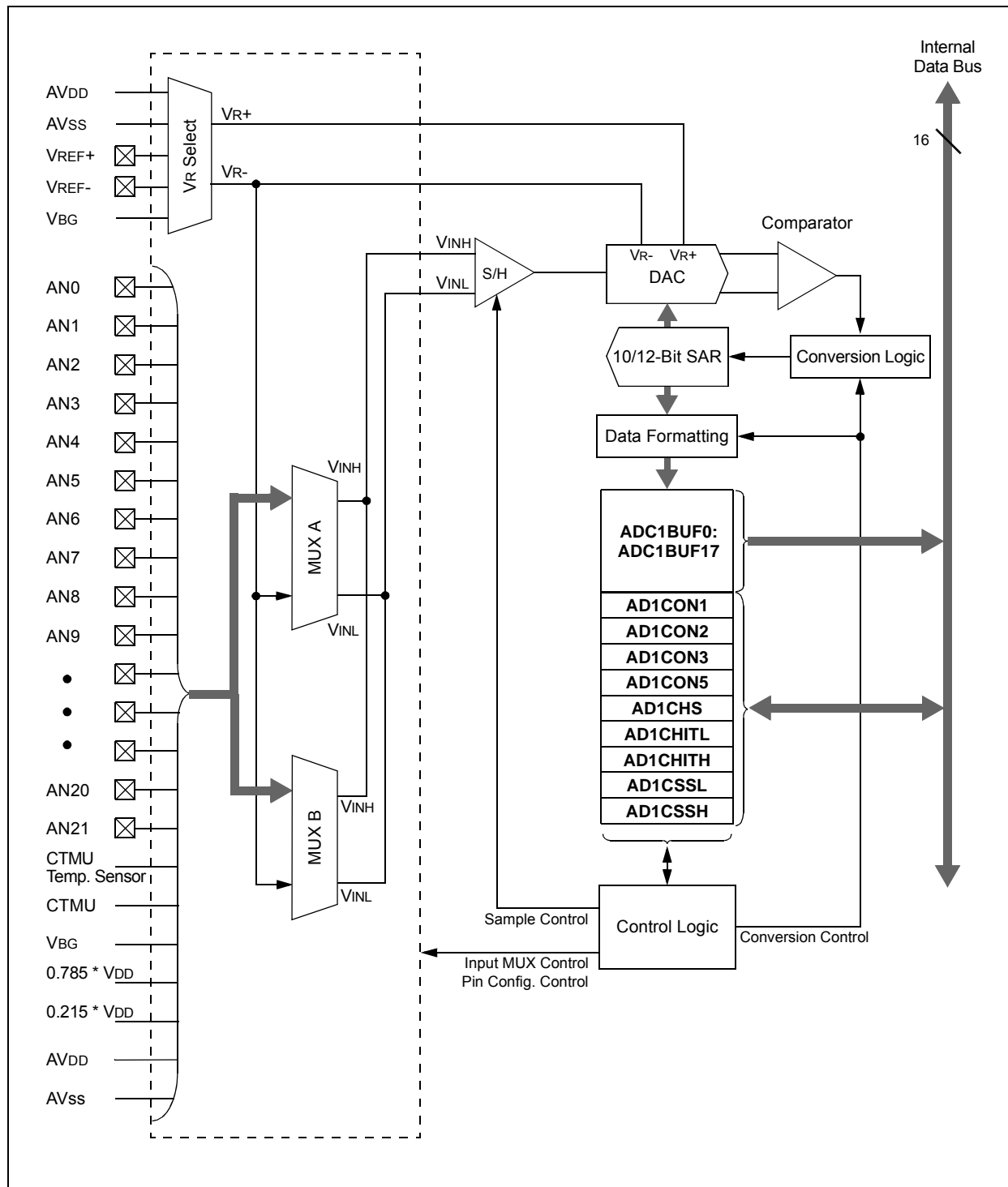
1 = Receive is complete, SSPxBUF is full

0 = Receive is not complete, SSPxBUF is empty

**Note 1:** Polarity of clock state is set by the CKP bit (SSPxCON1<4>).

# PIC24FV16KM204 FAMILY

**FIGURE 19-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM**



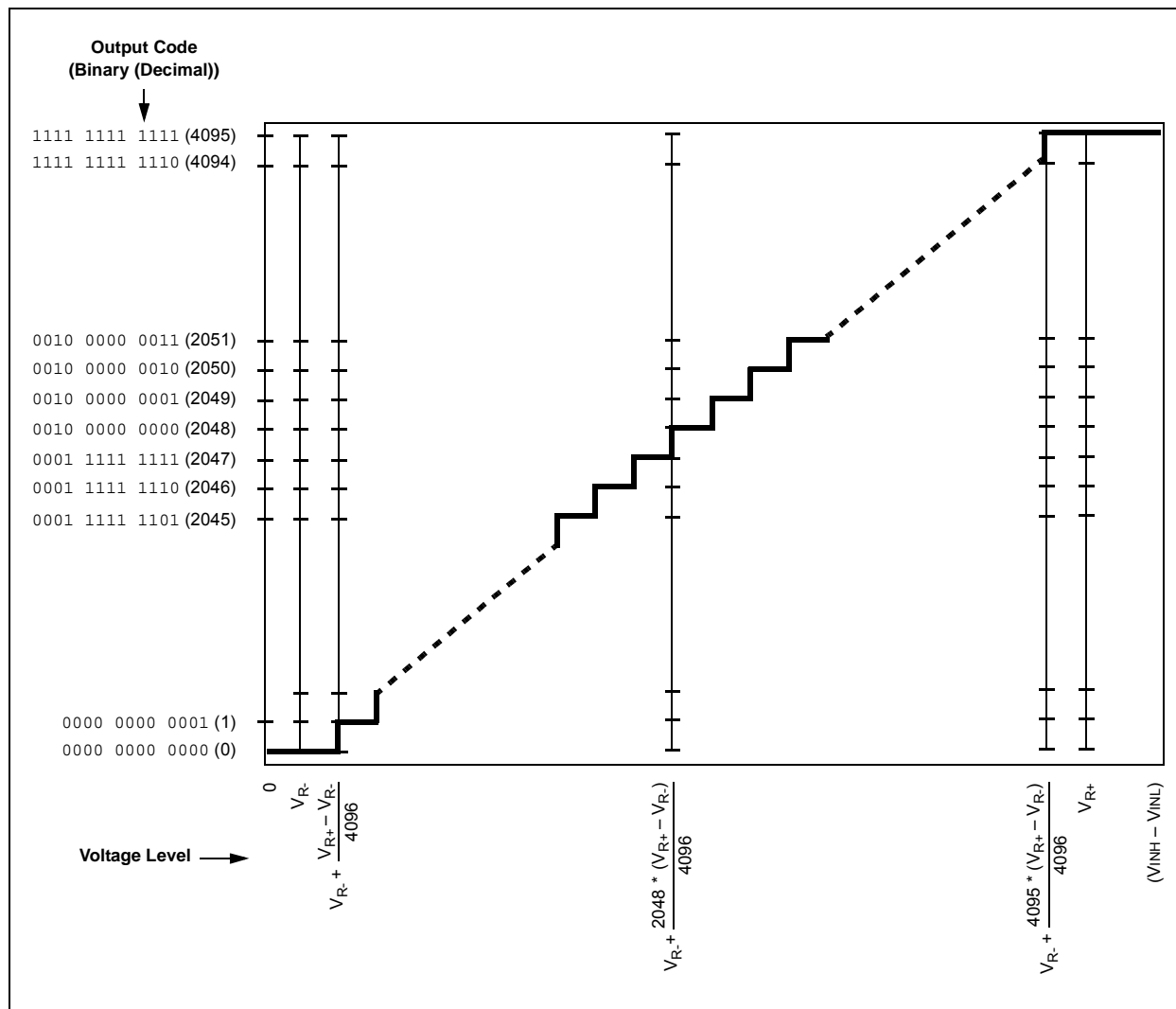
# PIC24FV16KM204 FAMILY

## 19.3 Transfer Function

The transfer functions of the A/D Converter in 12-bit resolution are shown in Figure 19-3. The difference of the input voltages ( $V_{INH} - V_{INL}$ ) is compared to the reference ( $(V_{R+}) - (V_{R-})$ ).

- The first code transition occurs when the input voltage is  $((V_{R+}) - (V_{R-}))/4096$  or 1.0 LSB.
- The '0000 0000 0001' code is centered at  $V_{R-} + (1.5 * ((V_{R+}) - (V_{R-}))/4096)$ .
- The '0010 0000 0000' code is centered at  $V_{REFL} + (2048.5 * ((V_{R+}) - (V_{R-}))/4096)$ .
- An input voltage less than  $V_{R-} + (((V_{R-}) - (V_{R-}))/4096)$  converts as '0000 0000 0000'.
- An input voltage greater than  $(V_{R-}) + (4095 * ((V_{R+}) - (V_{R-}))/4096)$  converts as '1111 1111 1111'.

FIGURE 19-3: 12-BIT A/D TRANSFER FUNCTION



# PIC24FV16KM204 FAMILY

## REGISTER 21-1: AMPxCON: OP AMP x CONTROL REGISTER<sup>(1)</sup>

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—
bit 15				bit 8			

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **AMPEN:** Op Amp x Control Module Enable bit  
               1 = Module is enabled  
               0 = Module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **AMPSIDL:** Op Amp x Peripheral Stop in Idle Mode bit  
               1 = Discontinues module operation when device enters Idle mode  
               0 = Continues module operation in Idle mode
- bit 12      **AMPSLP:** Op Amp x Peripheral Enabled in Sleep Mode bit  
               1 = Continues module operation when device enters Sleep mode  
               0 = Discontinues module operation in Sleep mode
- bit 11-8    **Unimplemented:** Read as '0'
- bit 7        **SPDSEL:** Op Amp x Power/Speed Select bit  
               1 = Higher power and bandwidth (faster response time)  
               0 = Lower power and bandwidth (slower response time)
- bit 6        **Unimplemented:** Read as '0'
- bit 5-3     **NINSEL<2:0>:** Negative Op Amp Input Select bits  
               111 = Reserved; do not use  
               110 = Reserved; do not use  
               101 = Op amp negative input is connected to the op amp output (voltage follower)  
               100 = Reserved; do not use  
               011 = Reserved; do not use  
               010 = Op amp negative input is connected to the OAxIND pin  
               001 = Op amp negative input is connected to the OAxINB pin  
               000 = Op amp negative input is connected to AVss
- bit 2-0     **PINSEL<2:0>:** Positive Op Amp Input Select bits  
               111 = Op amp positive input is connected to the output of the A/D input multiplexer  
               110 = Reserved; do not use  
               101 = Op amp positive input is connected to the DAC1 output for OA1 (DAC2 output for OA2)  
               100 = Reserved; do not use  
               011 = Reserved; do not use  
               010 = Op amp positive input is connected to the OAxINC pin  
               001 = Op amp positive input is connected to the OAxINA pin  
               000 = Op amp positive input is connected to AVss

**Note 1:** This register is available only on PIC24F(V)16KM2XX devices.



# PIC24FV16KM204 FAMILY

## REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS (CONTINUED)

- bit 2      **Unimplemented:** Read as '0'
- bit 1-0      **CCH<1:0>:** Comparator x Channel Select bits  
               11 = Inverting input of the comparator connects to BGBUF1<sup>(1)</sup>  
               10 = Inverting input of the comparator connects to the CxIND pin  
               01 = Inverting input of the comparator connects to the CxINC pin  
               00 = Inverting input of the comparator connects to the CxINB pin

- Note 1:** BGBUF1 voltage is configured by BUFREF1<1:0> (BUFCON0<1:0>).
- 2:** If the EVPOL<1:0> bits are set to a value other than '00', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

## REGISTER 22-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	C3EVT <sup>(1)</sup>	C2EVT <sup>(1)</sup>	C1EVT
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC
—	—	—	—	—	C3OUT <sup>(1)</sup>	C2OUT <sup>(1)</sup>	C1OUT
bit 7				bit 0			

<b>Legend:</b>	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **CMIDL:** Comparator x Stop in Idle Mode bit  
               1 = Comparator interrupts are disabled in Idle mode; enabled comparators remain operational  
               0 = Continues operation of all enabled comparators in Idle mode
- bit 14-11      **Unimplemented:** Read as '0'
- bit 10      **C3EVT:** Comparator 3 Event Status bit (read-only)<sup>(1)</sup>  
               Shows the current event status of Comparator 3 (CM3CON<9>).
- bit 9      **C2EVT:** Comparator 2 Event Status bit (read-only)<sup>(1)</sup>  
               Shows the current event status of Comparator 2 (CM2CON<9>).
- bit 8      **C1EVT:** Comparator 1 Event Status bit (read-only)  
               Shows the current event status of Comparator 1 (CM1CON<9>).
- bit 7-3      **Unimplemented:** Read as '0'
- bit 2      **C3OUT:** Comparator 3 Output Status bit (read-only)<sup>(1)</sup>  
               Shows the current output of Comparator 3 (CM3CON<8>).
- bit 1      **C2OUT:** Comparator 2 Output Status bit (read-only)<sup>(1)</sup>  
               Shows the current output of Comparator 2 (CM2CON<8>).
- bit 0      **C1OUT:** Comparator 1 Output Status bit (read-only)  
               Shows the current output of Comparator 1 (CM1CON<8>).

- Note 1:** Comparator 2 and Comparator 3 are only available on PIC24F(V)16KM2XX devices.

# PIC24FV16KM204 FAMILY

## REGISTER 25-5: FWDT: WATCHDOG TIMER CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN1	WINDIS	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

### Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7,5 **FWDTEN<1:0>**: Watchdog Timer Enable bits

11 = WDT is enabled in hardware

10 = WDT is controlled with the SWDTEN bit setting

01 = WDT is enabled only while the device is active, WDT is disabled in Sleep; SWDTEN bit is disabled

00 = WDT is disabled in hardware; SWDTEN bit is disabled

bit 6 **WINDIS**: Windowed Watchdog Timer Disable bit

1 = Standard WDT is selected; windowed WDT is disabled

0 = Windowed WDT is enabled; note that executing a **CLRWDT** instruction while the WDT is disabled in hardware and software (FWDTEN<1:0> = 00 and SWDTEN (RCON<5>) = 0) will not cause a device Reset

bit 4 **FWPSA**: WDT Prescaler bit

1 = WDT prescaler ratio of 1:128

0 = WDT prescaler ratio of 1:32

bit 3-0 **WDTPS<3:0>**: Watchdog Timer Postscale Select bits

1111 = 1:32,768

1110 = 1:16,384

1101 = 1:8,192

1100 = 1:4,096

1011 = 1:2,048

1010 = 1:1,024

1001 = 1:512

1000 = 1:256

0111 = 1:128

0110 = 1:64

0101 = 1:32

0100 = 1:16

0011 = 1:8

0010 = 1:4

0001 = 1:2

0000 = 1:1

# PIC24FV16KM204 FAMILY

## REGISTER 25-6: FPOR: RESET CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE <sup>(2)</sup>	BORV1 <sup>(3)</sup>	BORV0 <sup>(3)</sup>	I2C1SEL <sup>(1)</sup>	PWRTEN	RETCFG <sup>(1)</sup>	BOREN1	BOREN0
bit 7							bit 0

### Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **MCLRE:** MCLR Pin Enable bit<sup>(2)</sup>

1 = MCLR pin is enabled; RA5 input pin is disabled

0 = RA5 input pin is enabled; MCLR is disabled

bit 6-5 **BORV<1:0>:** Brown-out Reset Enable bits<sup>(3)</sup>

11 = Brown-out Reset is set to the lowest voltage

10 = Brown-out Reset is set to the middle voltage

01 = Brown-out Reset is set to the highest voltage

00 = Downside protection on POR is enabled – Low-Power BOR (LPBOR) is selected

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit<sup>(1)</sup>

1 = Default location for SCL1/SDA1 pins

0 = Alternate location for SCL1/SDA1 pins

bit 3 **PWRTEN:** Power-up Timer Enable bit

1 = PWRT is enabled

0 = PWRT is disabled

bit 2 **RETCFG:** Retention Regulator Configuration bit<sup>(1)</sup>

1 = Low-voltage regulator is not available

0 = Low-voltage regulator is available and controlled by the RETEN bit (RCON<12>) during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits

11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled

10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled

01 = Brown-out Reset is controlled with the SBOREN bit setting

00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

**Note 1:** This setting only applies to the “FV” devices. This bit is reserved and should be maintained as ‘1’ on “F” devices.

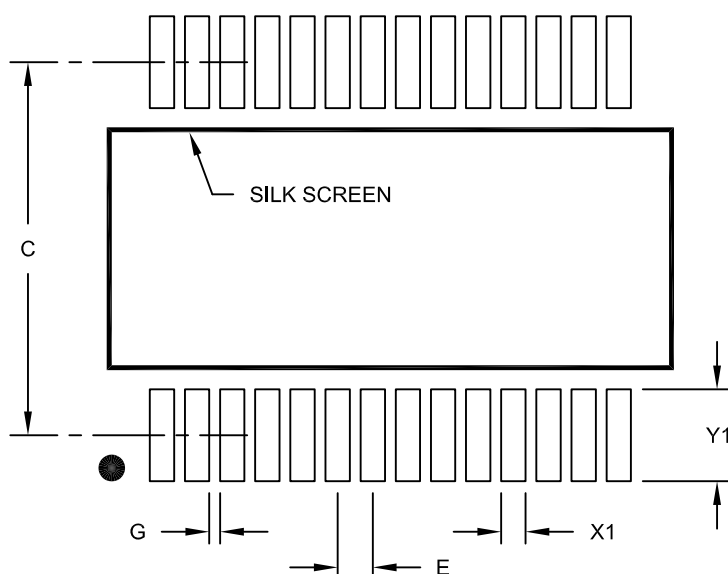
**2:** The MCLRE fuse can only be changed when using the VPP-based ICSP™ mode entry. This prevents a user from accidentally locking out the device from the low-voltage test entry.

**3:** Refer to **Section 27.0 “Electrical Characteristics”** for BOR voltages.

# PIC24FV16KM204 FAMILY

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

# PIC24FV16KM204 FAMILY

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NOTES: