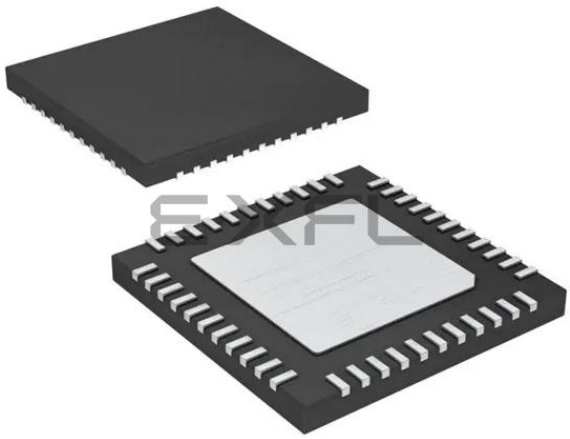

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km104-e-ml

TABLE 4-25: A/D REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	300h	A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF1	302h	A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF2	304h	A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF3	306h	A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF4	308h	A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF5	30Ah	A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF6	30Ch	A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF7	30Eh	A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF8	310h	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF9	312h	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF10	314h	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF11	316h	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare																xxxx
ADC1BUF12	318h	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF13	31Ah	A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF14	31Ch	A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF15	31Eh	A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF16	320h	A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF17	322h	A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF18	324h	A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF19	326h	A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF20	328h	A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF21	32Ah	A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF22	32Ch	A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF23	32Eh	A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare																xxxx
AD1CON1	340h	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	342h	PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	344h	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	348h	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	34Eh	—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—	CSS23	CSS22	CSS21	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16	0000
AD1CSSL	350h	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(1,2)	CSS7(1,2)	CSS6(1,2)	CSS5(1)	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON5	354h	ASEN	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	356h	—	—	—	—	—	—	—	—	CHH23	CHH22	CHH21	CHH20(1)	CHH19(1)	CHH18	CHH17	CHH16	0000
AD1CHITL	358h	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8(1,2)	CHH7(1,2)	CHH6(1,2)	CHH5(1)	CHH4	CHH3	CHH2	CHH1	CHH0	0000
AD1CTMENH	360h	—	—	—	—	—	—	—	—	CTMEN23	CTMEN22	CTMEN21	CTMEN20(1)	CTMEN19(1)	CTMEN18	CTMEN17	CTMEN16	0000
AD1CTMENL	362h	CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8((1,2)	CTMEN7(1,2)	CTMEN6(1,2)	CTMEN5(1)	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Flash programming, refer to the *"PIC24F Family Reference Manual"*, **"Program Memory"** (DS39715).

The PIC24FV16KM204 family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with VDD over 1.8V.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FXXXXX device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (which are named PGECx and PGEDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear/Program Mode Entry Voltage (MCLR/VPP). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or custom firmware to be programmed.

Run-Time Self-Programming (RTSP) is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 32 instructions (96 bytes) at a time, and erase program memory in blocks of 32, 64 and 128 instructions (96,192 and 384 bytes) at a time.

The NVMOP<1:0> (NVMCON<1:0>) bits decide the erase block size.

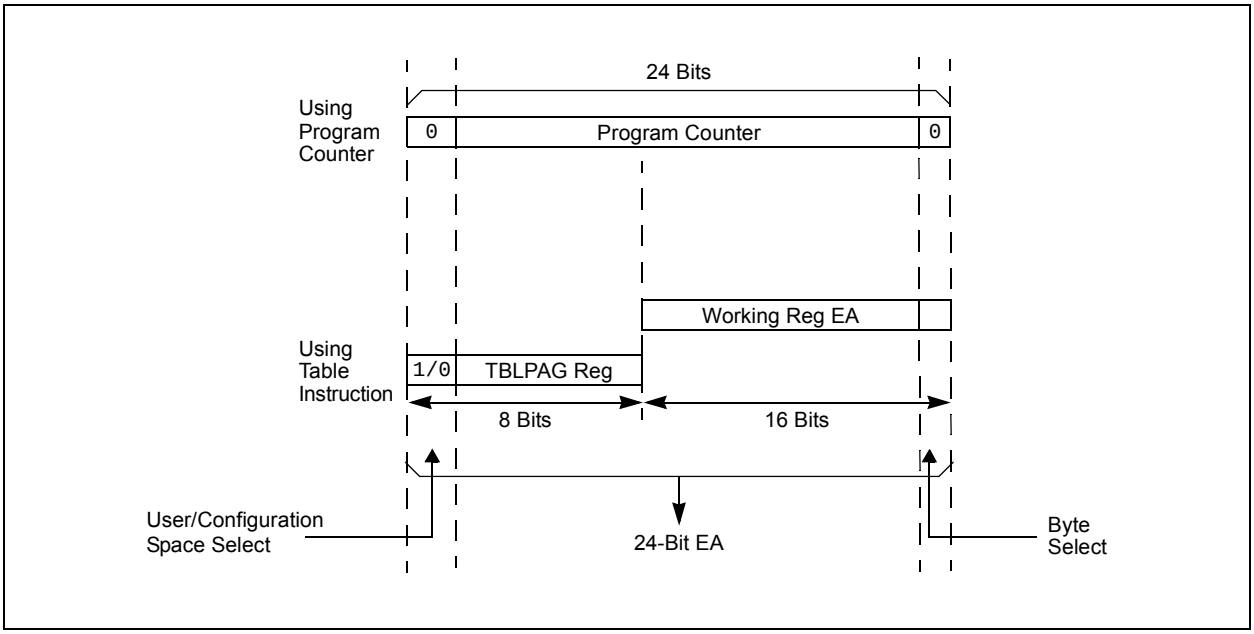
5.1 Table Instructions and Flash Programming

Regardless of the method used, Flash memory programming is done with the Table Read and Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as depicted in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table (AIVT)
0 = Uses standard (default) Interrupt Vector Table (IVT)

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

REGISTER 8-20: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP4IP2	CCP4IP1	CCP4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCT1IP<2:0>:** Capture/Compare 1 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP4IP<2:0>:** Capture/Compare 4 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCP3IP<2:0>:** Capture/Compare 3 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **NVMIP<2:0>:** NVM Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** A/D Conversion Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-33: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	ULPWUIP2	ULPWUIP1	ULPWUIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ULPWUIP<2:0>:** Ultra Low-Power Wake-up Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-34: IPC24: INTERRUPT PRIORITY CONTROL REGISTER 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CLC2IP2	CLC2IP1	CLC2IP0	—	CLC1IP2	CLC1IP1	CLC1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CLC2IP<2:0>:** CLC2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CLC1IP<2:0>:** CLC1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

12.0 TIMER1

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on timers, refer to the *"PIC24F Family Reference Manual"*, **"Timers"** (DS39704).

The Timer1 module is a 16-bit timer which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running, interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

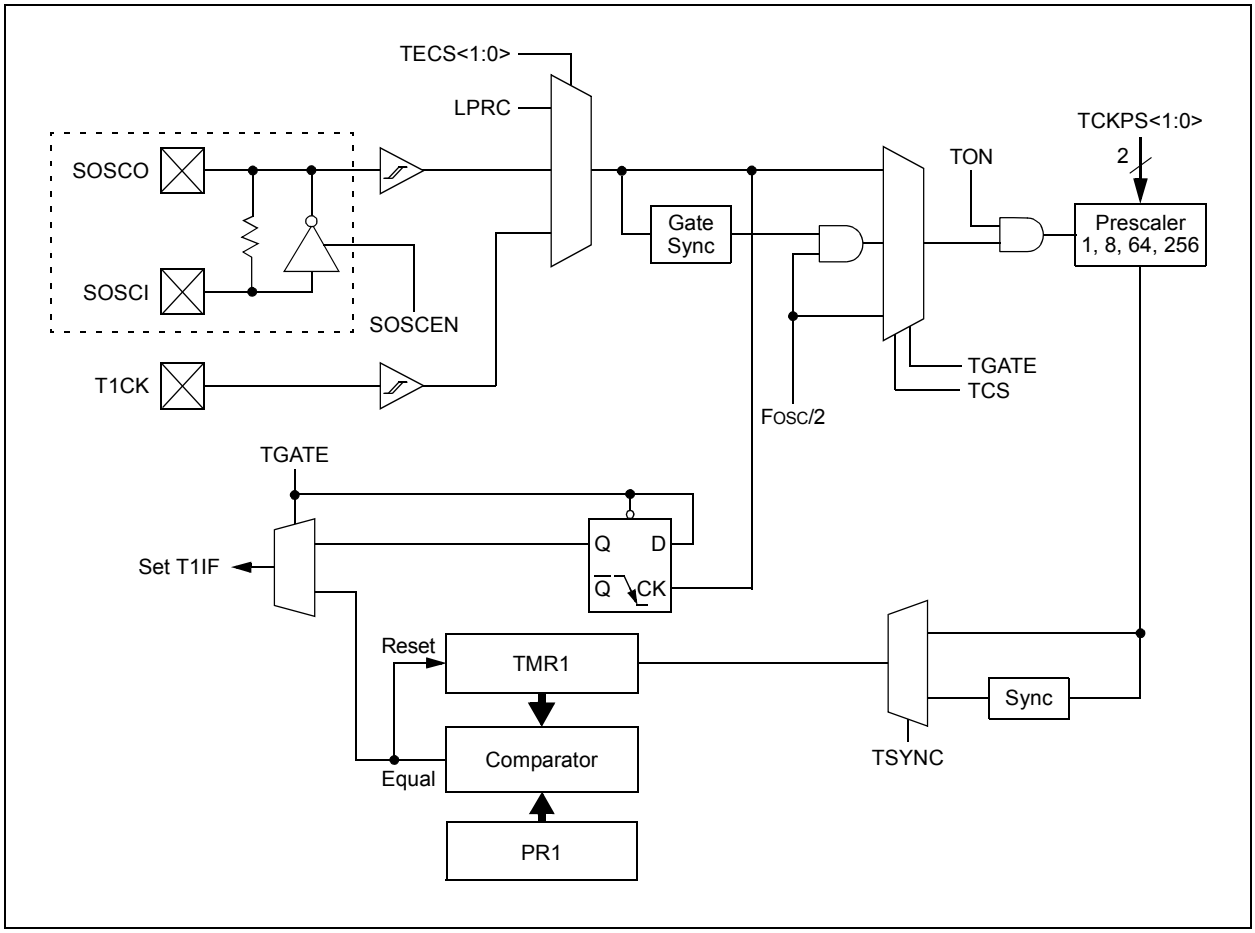
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation During CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 illustrates a block diagram of the 16-bit Timer1 module.

To configure Timer1 for operation:

1. Set the TON bit (= 1).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
5. Load the timer period value into the PR1 register.
6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



REGISTER 14-8: SSPxADD: MSSPx SLAVE ADDRESS/BAUD RATE GENERATOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **ADD<7:0>:** Slave Address/Baud Rate Generator Value bits

SPI Master and I²C™ Master modes:
Reload value for the Baud Rate Generator. Clock period is (([SPxADD] + 1) * 2)/FOSC.

I²C Slave modes:
Represents 7 or 8 bits of the slave address, depending on the addressing mode used:

7-Bit mode: Address is ADD<7:1>; ADD<0> is ignored.

10-Bit LSb mode: ADD<7:0> are the Least Significant bits of the address.

10-Bit MSb mode: ADD<2:1> are the two Most Significant bits of the address; ADD<7:3> are always '11110' as a specification requirement; ADD<0> is ignored.

REGISTER 14-9: SSPxMSK: I²C™ SLAVE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **MSK<7:0>:** Slave Address Mask Select bits(1)

1 = Masking of corresponding bit of SSPxADD is enabled
0 = Masking of corresponding bit of SSPxADD is disabled

Note 1: MSK0 is not used as a mask bit in 7-bit addressing.

16.3 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value, loaded into the lower half of RCFGCAL, is multiplied by four and will be either added or subtracted from the RTCC timer, once every minute. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute.
3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGCAL register value must be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

   b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGCAL register value must be positive. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

EQUATION 16-1:

(Ideal Frequency† – Measured Frequency) *
60 = Clocks per Minute

† Ideal Frequency = 32,768 Hz

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse, except when SECONDS = 00, 15, 30 or 45. This is due to the auto-adjust of the RTCC at 15 second intervals.

Note:	It is up to the user to include, in the error value, the initial error of the crystal: drift due to temperature and drift due to crystal aging.

16.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>)
- One-time alarm and repeat alarm options are available

16.4.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 16-2, the interval selection of the alarm is configured through the AMASKx bits (ALCFGRPT<13:10>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT<7:0> bits (ALCFGRPT<7:0>). When the value of the ARPTx bits equals 00h and the CHIME bit (ALCFGRPT<14>) is cleared, the repeat function is disabled, and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT<7:0> with FFh.

After each alarm is issued, the value of the ARPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ARPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

16.4.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to other peripherals.

Note:	Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers, and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

REGISTER 20-1: DACxCON: DACx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DACEN:** DACx Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **DACSIDL:** DACx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **DACSLP:** DACx Enable Peripheral During Sleep bit
1 = DACx continues to output the most recent value of DACxDAT during Sleep mode
0 = DACx is powered down in Sleep mode; DACxOUT pin is controlled by the TRISx and LATx bits

bit 11 **DACFM:** DACx Data Format Select bit
1 = Data is left justified (data stored in DACxDAT<15:8>)
0 = Data is right justified (data stored in DACxDAT<7:0>)

bit 10 **Unimplemented:** Read as ‘0’

bit 9 **SRDIS:** Soft Reset Disable bit
1 = DACxCON and DACxDAT SFRs reset only on a POR or BOR Reset
0 = DACxCON and DACxDAT SFRs reset on any type of device Reset

bit 8 **DACTRIG:** DACx Trigger Input Enable bit
1 = Analog output value updates when the selected (by DACTSEL<4:0>) event occurs
0 = Analog output value updates as soon as DACxDAT is written (DAC Trigger is ignored)

bit 7 **DACOE:** DACx Output Enable bit
1 = DACx output pin is enabled and driven on the DACxOUT pin
0 = DACx output pin is disabled, DACx output is available internally to other peripherals only

Note 1: BGBUF1 voltage is configured by BUFREF<1:0> (BUFCON0<1:0>).

REGISTER 20-1: DACxCON: DACx CONTROL REGISTER (CONTINUED)

bit 6-2 **DACTSEL<4:0>:** DACx Trigger Source Select bits
11101-11111 = Unused
11100 = CTMU
11011 = A/D
11010 = Comparator 3
11001 = Comparator 2
11000 = Comparator 1
10011 to 10111 = Unused
10010 = CLC2 output
10001 = CLC1 output
01100 to 10000 = Unused
01011 = Timer1 Sync output
01010 = External Interrupt 2
01001 = External Interrupt 1
01000 = External Interrupt 0
0011x = Unused
00101 = MCCP5 or SCCP5 Sync output
00100 = MCCP4 or SCCP4 Sync output
00011 = MCCP3 or SCCP3 Sync output
00010 = MCCP2 or SCCP2 Sync output
00001 = MCCP1 or SCCP1 Sync output
00000 = Unused

bit 1-0 **DACREF<1:0>:** DACx Reference Source Select bits
11 = Internal Band Gap Buffer 1 (BGBUF1)**(1)**
10 = AV_{DD}
01 = DV_{REF+}
00 = Reference is not connected (lowest power but no DAC functionality)

Note 1: BGBUF1 voltage is configured by BUFREF<1:0> (BUFCON0<1:0>).

REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER (CONTINUED)

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge
0 = Edge 2 is programmed for a negative edge

bit 5-2 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = Edge 2 source is the Comparator 3 output
1110 = Edge 2 source is the Comparator 2 output
1101 = Edge 2 source is the Comparator 1 output
1100 = Unimplemented; do not use
1011 = Edge 2 source is CLC1
1010 = Edge 2 source is the MCCP2 Compare Event (CCP2IF)
1001 = Unimplemented; do not use
1000 = Edge 2 source is CTED13
0111 = Edge 2 source is CTED12
0110 = Edge 2 source is CTED11**(2)**
0101 = Edge 2 source is CTED10
0100 = Edge 2 source is CTED9**(2)**
0011 = Edge 2 source is CTED1
0010 = Edge 2 source is CTED2
0001 = Edge 2 source is the MCCP1 Compare Event (CCP1IF)
0000 = Edge 2 source is Timer1

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

REGISTER 24-3: CTMUCON2L: CTMU CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DISCHS2	DISCHS1	DISCHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **IRSTEN:** CTMU Current Source Reset Enable bit
1 = Signal selected by the DISCHS<2:0> bits or the IDISSEN control bit will reset the CTMU edge detect logic
0 = CTMU edge detect logic will not occur

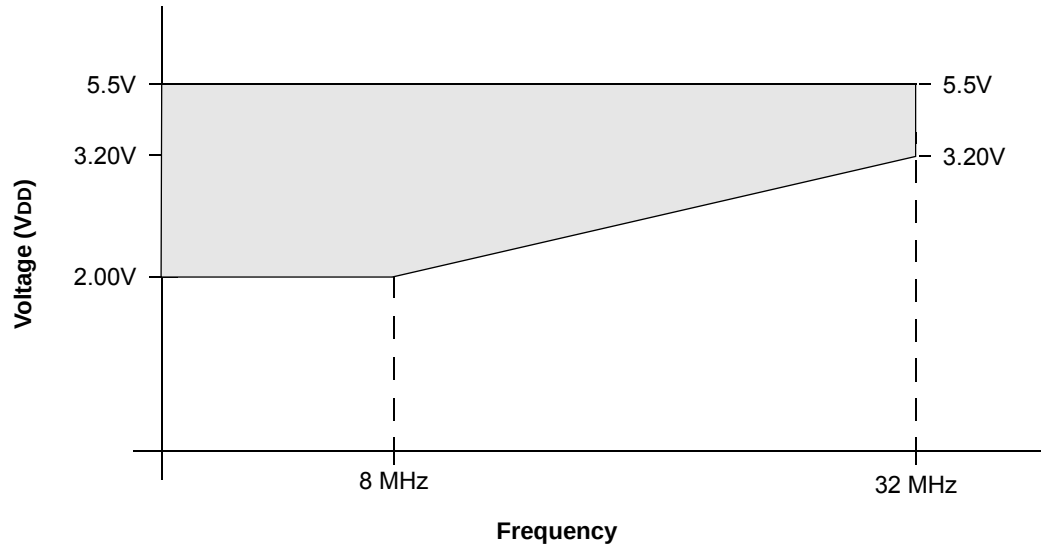
bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DISCHS<2:0>:** Discharge Source Select bits
111 = CLC2 output
110 = CLC1 output
101 = Reserved; do not use.
100 = A/D end of conversion signal
011 = SCCP5 auxiliary output
110 = MCCP2 auxiliary output
001 = MCCP1 auxiliary output
000 = No discharge source selected, use the IDISSEN bit

NOTES:

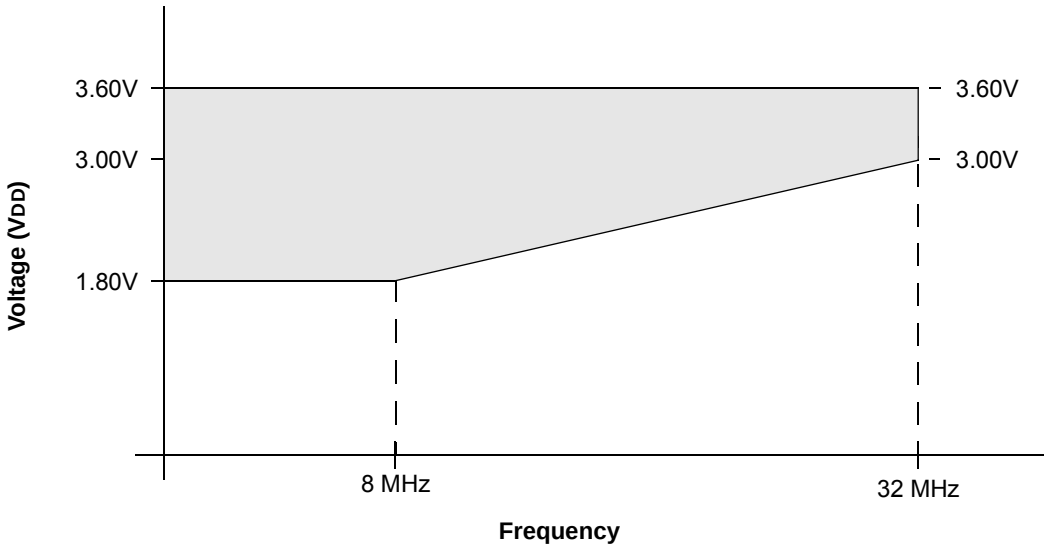
27.1 DC Characteristics

FIGURE 27-1: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 2.0) + 8 MHz.

FIGURE 27-2: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 1.8) + 8 MHz.

TABLE 27-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 27-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 20-Pin PDIP	θ_{JA}	62.4	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	60	—	°C/W	**1**
Package Thermal Resistance, 20-Pin SSOP	θ_{JA}	108	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SSOP	θ_{JA}	71	—	°C/W	**1**
Package Thermal Resistance, 20-Pin SOIC	θ_{JA}	75	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	80.2	—	°C/W	**1**
Package Thermal Resistance, 20-Pin QFN	θ_{JA}	43	—	°C/W	**1**
Package Thermal Resistance, 28-Pin QFN	θ_{JA}	32	—	°C/W	**1**
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	29	—	°C/W	**1**
Package Thermal Resistance, 44-Pin TQFP	θ_{JA}	40	—	°C/W	**1**
Package Thermal Resistance, 48-Pin UQFN	θ_{JA}	41	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

TABLE 27-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX)** **2.0V to 5.5V (PIC24FV16KMXXX)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DC10	V_{DD}	**Supply Voltage**	1.8	—	3.6	V	For PIC24F devices
			2.0	—	5.5	V	For PIC24FV devices
DC12	V_{DR}	**RAM Data Retention Voltage(2)**	1.6	—	—	V	For PIC24F devices
			1.8	—	—	V	For PIC24FV devices
DC16	V_{POR}	**V_{DD} Start Voltage** to Ensure Internal Power-on Reset Signal	V_{SS}	—	0.7	V	
DC17	SV_{DD}	**V_{DD} Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which V_{DD} can be lowered without losing RAM data.

TABLE 27-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(4)**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I2C™ Buffer	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage(4,5)**					
DI20		I/O Pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	
		Digital Only	0.8 VDD	—	VDD	V	
DI25		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I2C Buffer:					
		with Analog Functions	0.7 VDD	—	VDD	V	
		Digital Only	0.7 VDD	—	VDD	V	
DI29		I/O Pins with SMBus	2.1	—	VDD	V	2.5V ≤ VPIN ≤ VDD
DI30	ICNPU	**CNx Pull-up Current**	50	250	500	μA	VDD = 3.3V, VPIN = VSS
DI31	IPU	**Maximum Load Current for Digital High Detection w/Internal Pull-up**	—	—	30	μA	VDD = 2.0V
			—	—	1000	μA	VDD = 3.3V
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Ports	—	0.050	±0.100	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Pins with OAxOUT Functions (RB15 and RB3)	—	0.100	±0.200	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

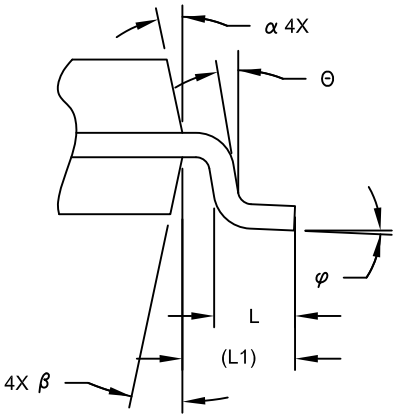
3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-4 and Table 1-5 for I/O pin buffer types.

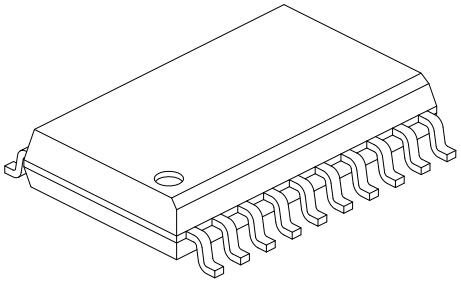
5: VIH requirements are met when the internal pull-ups are enabled.

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

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NOTES: