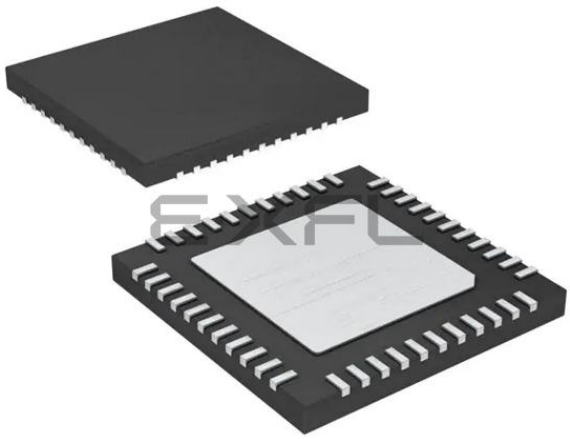


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

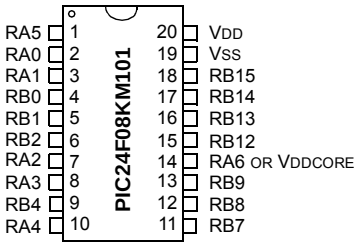
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 16KB (5.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 22x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km104-i-ml |

## Pin Diagrams

**20-Pin PDIP/SSOP/SOIC**




| Pin | Pin Features | |
|---|---|---|
| | PIC24F08KM101 | PIC24FVKM08KM101 |
| 1 | $\overline{\text{MCLR}}$/VPP/RA5 | |
| 2 | PGEC2/CVREF+/VREF+/AN0/CN2/RA0 | |
| 3 | PGED2/CVREF-/VREF-/AN1/CN3/RA1 | |
| 4 | PGED1/AN2/CTCMP/ULPWU/C1IND/OC2A/CN4/RB0 | |
| 5 | PGEC1/AN3/C1INC/CTED12/CN5/RB1 | |
| 6 | AN4/U1RX/TCKIB/CTED13/CN6/RB2 | |
| 7 | OSCI/CLKI/AN13/C1INB/CN30/RA2 | |
| 8 | OSCO/CLKO/AN14/C1INA/CN29/RA3 | |
| 9 | PGED3/SOSCI/AN15/CLCINA/CN1/RB4 | |
| 10 | PGEC3/SOSCO/SCLKI/AN16/PWRLCLK/CLCINB/CN0/RA4 | |
| 11 | AN19/U1TX/CTED1/INT0/CN23/RB7 | AN19/U1TX/IC1/OC1A/CTED1/INT0/CN23/RB7 |
| 12 | AN20/SCL1/$\overline{\text{U1CTS}}$/OC1B/CTED10/CN22/RB8 | |
| 13 | AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/CLC1O/CTED4/CN21/RB9 | |
| 14 | IC1/OC1A/INT2/CN8/RA6 | VCAP OR VDDCORE |
| 15 | AN12/HLVDIN/SCK1/OC1C/CTED2/CN14/RB12 | AN12/HLVDIN/SCK1/OC1C/CTED2/INT2/CN14/RB12 |
| 16 | AN11/SDO1/OCFB/OC1D/CTPLS/CN13/RB13 | |
| 17 | CVREF/AN10/SDI1/C1OUT/OCFA/CTED5/INT1/CN12/RB14 | |
| 18 | AN9/REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15 | |
| 19 | VSS/AVSS | |
| 20 | VDD/AVDD | |

**TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION**

| Function | F | | | | | FV | | | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin Number | | | | | Pin Number | | | | | | | |
| | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | | | |
| AN0 | 2 | 2 | 27 | 19 | 21 | 2 | 2 | 27 | 19 | 21 | I | ANA | A/D Analog Inputs |
| AN1 | 3 | 3 | 28 | 20 | 22 | 3 | 3 | 28 | 20 | 22 | I | ANA | A/D Analog Inputs |
| AN2 | 4 | 4 | 1 | 21 | 23 | 4 | 4 | 1 | 21 | 23 | I | ANA | A/D Analog Inputs |
| AN3 | 5 | 5 | 2 | 22 | 24 | 5 | 5 | 2 | 22 | 24 | I | ANA | A/D Analog Inputs |
| AN4 | 6 | 6 | 3 | 23 | 25 | 6 | 6 | 3 | 23 | 25 | I | ANA | A/D Analog Inputs |
| AN5 | — | 7 | 4 | 24 | 26 | — | 7 | 4 | 24 | 26 | I | ANA | A/D Analog Inputs |
| AN6 | — | — | — | 25 | 27 | — | — | — | 25 | 27 | I | ANA | A/D Analog Inputs |
| AN7 | — | — | — | 26 | 28 | — | — | — | 26 | 28 | I | ANA | A/D Analog Inputs |
| AN8 | — | — | — | 27 | 29 | — | — | — | 27 | 29 | I | ANA | A/D Analog Inputs |
| AN9 | 18 | 26 | 23 | 15 | 16 | 18 | 26 | 23 | 15 | 16 | I | ANA | A/D Analog Inputs |
| AN10 | 17 | 25 | 22 | 14 | 15 | 17 | 25 | 22 | 14 | 15 | I | ANA | A/D Analog Inputs |
| AN11 | 16 | 24 | 21 | 11 | 12 | 16 | 24 | 21 | 11 | 12 | I | ANA | A/D Analog Inputs |
| AN12 | 15 | 23 | 20 | 10 | 11 | 15 | 23 | 20 | 10 | 11 | I | ANA | A/D Analog Inputs |
| AN13 | 7 | 9 | 6 | 30 | 33 | 7 | 9 | 6 | 30 | 33 | I | ANA | A/D Analog Inputs |
| AN14 | 8 | 10 | 7 | 31 | 34 | 8 | 10 | 7 | 31 | 34 | I | ANA | A/D Analog Inputs |
| AN15 | 9 | 11 | 8 | 33 | 36 | 9 | 11 | 8 | 33 | 36 | I | ANA | A/D Analog Inputs |
| AN16 | 10 | 12 | 9 | 34 | 37 | 10 | 12 | 9 | 34 | 37 | I | ANA | A/D Analog Inputs |
| AN17 | — | 14 | 11 | 41 | 45 | — | 14 | 11 | 41 | 45 | I | ANA | A/D Analog Inputs |
| AN18 | — | 15 | 12 | 42 | 46 | — | 15 | 12 | 42 | 46 | I | ANA | A/D Analog Inputs |
| AN19 | 11 | 16 | 13 | 43 | 47 | 11 | 16 | 13 | 43 | 47 | I | ANA | A/D Analog Inputs |
| AN20 | 12 | 17 | 14 | 44 | 48 | 12 | 17 | 14 | 44 | 48 | I | ANA | A/D Analog Inputs |
| AN21 | 13 | 18 | 15 | 1 | 1 | 13 | 18 | 15 | 1 | 1 | I | ANA | A/D Analog Inputs |
| ASCL1 | — | 15 | 12 | 42 | 46 | — | 15 | 12 | 42 | 46 | I/O | $I^2C$™ | Alternate I2C1 Clock Input/Output |
| ASDA1 | — | 14 | 11 | 41 | 45 | — | 14 | 11 | 41 | 45 | I/O | $I^2C$ | Alternate I2C1 Data Input/Output |
| AVDD | 20 | 28 | 25 | 17 | 18 | 20 | 28 | 25 | 17 | 18 | P | — | A/D Supply Pins |
| AVSS | 19 | 27 | 24 | 16 | 17 | 19 | 27 | 24 | 16 | 17 | P | — | A/D Supply Pins |
| C1INA | 8 | 7 | 4 | 24 | 26 | 8 | 7 | 4 | 24 | 26 | I | ANA | Comparator 1 Input A (+) |
| C1INB | 7 | 6 | 3 | 23 | 25 | 7 | 6 | 3 | 23 | 25 | I | ANA | Comparator 1 Input B (-) |
| C1INC | 5 | 5 | 2 | 22 | 24 | 5 | 5 | 2 | 22 | 24 | I | ANA | Comparator 1 Input C (+) |
| C1IND | 4 | 4 | 1 | 21 | 23 | 4 | 4 | 1 | 21 | 23 | I | ANA | Comparator 1 Input D (-) |

**Legend:** ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C$™ = $I^2C$/SMBus input buffer

**TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Function | F | | | | | FV | | | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin Number | | | | | Pin Number | | | | | | | |
| | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | | | |
| CTED1 | 11 | 20 | 17 | 7 | 7 | 11 | 2 | 27 | 19 | 21 | I | ST | CTMU Trigger Edge Inputs |
| CTED2 | 15 | 23 | 20 | 10 | 11 | 15 | 23 | 20 | 10 | 11 | I | ST | CTMU Trigger Edge Inputs |
| CTED3 | — | 19 | 16 | 6 | 6 | — | 19 | 16 | 6 | 6 | I | ST | CTMU Trigger Edge Inputs |
| CTED4 | 13 | 18 | 15 | 1 | 1 | 13 | 18 | 15 | 1 | 1 | I | ST | CTMU Trigger Edge Inputs |
| CTED5 | 17 | 25 | 22 | 14 | 15 | 17 | 25 | 22 | 14 | 15 | I | ST | CTMU Trigger Edge Inputs |
| CTED6 | 18 | 26 | 23 | 15 | 16 | 18 | 26 | 23 | 15 | 16 | I | ST | CTMU Trigger Edge Inputs |
| CTED7 | — | — | — | 5 | 5 | — | — | — | 5 | 5 | I | ST | CTMU Trigger Edge Inputs |
| CTED8 | — | — | — | 13 | 14 | — | — | — | 13 | 14 | I | ST | CTMU Trigger Edge Inputs |
| CTED9 | — | 22 | 19 | 9 | 10 | — | 22 | 19 | 9 | 10 | I | ST | CTMU Trigger Edge Inputs |
| CTED10 | 12 | 17 | 14 | 44 | 48 | 12 | 17 | 14 | 44 | 48 | I | ST | CTMU Trigger Edge Inputs |
| CTED11 | — | 21 | 18 | 8 | 9 | — | 21 | 18 | 8 | 9 | I | ST | CTMU Trigger Edge Inputs |
| CTED12 | 5 | 5 | 2 | 22 | 24 | 5 | 5 | 2 | 22 | 24 | I | ST | CTMU Trigger Edge Inputs |
| CTED13 | 6 | 6 | 3 | 23 | 25 | 6 | 6 | 3 | 23 | 25 | I | ST | CTMU Trigger Edge Inputs |
| CTPLS | 16 | 24 | 21 | 11 | 12 | 16 | 24 | 21 | 11 | 12 | O | — | CTMU Pulse Output |
| $CV_{REF}$ | 17 | 25 | 22 | 14 | 15 | 17 | 25 | 22 | 14 | 15 | O | ANA | Comparator Voltage Reference Output |
| $CV_{REF+}$ | 2 | 2 | 27 | 19 | 21 | 2 | 2 | 27 | 19 | 21 | I | ANA | Comparator Voltage Reference Positive Input |
| $CV_{REF-}$ | 3 | 3 | 28 | 20 | 22 | 3 | 3 | 28 | 20 | 22 | I | ANA | Comparator Voltage Reference Negative Input |
| DAC1OUT | — | 23 | 20 | 10 | 11 | — | 23 | 20 | 10 | 11 | O | ANA | DAC1 Output |
| DAC1REF+ | — | 2 | 27 | 19 | 21 | — | 2 | 27 | 19 | 21 | I | ANA | DAC1 Positive Voltage Reference Input |
| DAC2OUT | — | 25 | 22 | 14 | 15 | — | 25 | 22 | 14 | 15 | O | ANA | DAC2 Output |
| DAC2REF+ | — | 26 | 23 | 15 | 16 | — | 26 | 23 | 15 | 16 | I | ANA | DAC2 Positive Voltage Reference Input |
| HLVDIN | 15 | 23 | 20 | 10 | 11 | 15 | 23 | 20 | 10 | 11 | I | ANA | External High/Low-Voltage Detect Input |
| IC1 | 14 | 19 | 16 | 6 | 6 | 11 | 19 | 16 | 6 | 6 | I | ST | MCCP1 Input Capture Input |
| IC2 | 13 | 18 | 15 | 1 | 1 | 13 | 18 | 15 | 1 | 1 | I | ST | MCCP2 Input Capture Input |
| IC3 | — | 23 | 20 | 13 | 14 | — | 23 | 20 | 13 | 14 | I | ST | MCCP3 Input Capture Input |
| IC4 | — | 14 | 11 | 5 | 5 | — | 14 | 11 | 5 | 5 | I | ST | SCCP4 Input Capture Input |
| IC5 | — | 15 | 12 | 12 | 13 | — | 15 | 12 | 12 | 13 | I | ST | SCCP5 Input Capture Input |
| INT0 | 11 | 16 | 13 | 43 | 47 | 11 | 16 | 13 | 43 | 47 | I | ST | External Interrupt 0 Input |
| INT1 | 17 | 25 | 22 | 14 | 15 | 17 | 25 | 22 | 14 | 15 | I | ST | External Interrupt 1 Input |
| INT2 | 14 | 20 | 17 | 7 | 7 | 15 | 23 | 20 | 10 | 11 | I | ST | External Interrupt 2 Input |

**Legend:** ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C$™ = $I^2C$/SMBus input buffer

**NOTES:**

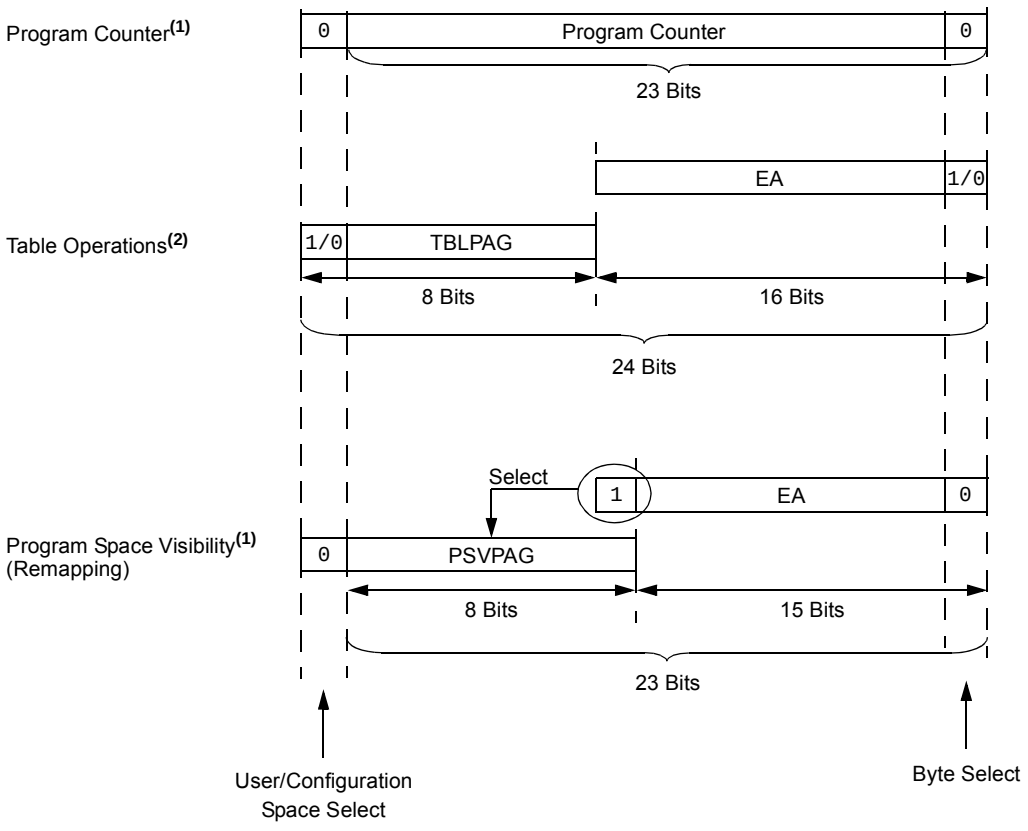
**TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | <23> | <22:16> | <15> | <14:1> | <0> |
| Instruction Access (Code Execution) | User | 0 | PC<22:1> | | | 0 |
| | | 0xx xxxx xxxx xxxx xxxx xxx0 | | | | |
| TBLRD/TBLWT (Byte/Word Read/Write) | User | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 0xxx xxxx | | xxxx xxxx xxxx xxxx | | |
| | Configuration | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 1xxx xxxx | | xxxx xxxx xxxx xxxx | | |
| Program Space Visibility (Block Remap/Read) | User | 0 | PSVPAG<7:0>(2) | | Data EA<14:0>(1) | |
| | | 0 | xxxx xxxx | | xxx xxxx xxxx xxxx | |

**Note 1:** Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

**2:** PSVPAG can have only two values ('00' to access program memory and FF to access data EEPROM) on the PIC24F16KM family.

**FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**




**Note 1:** The LSb of program space addresses is always fixed as '0' in order to maintain word alignment of data in the program and Data Spaces.

**2:** Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

### 6.4.3 READING THE DATA EEPROM

To read a word from data EEPROM, the Table Read instruction is used. Since the EEPROM array is only 16 bits wide, only the TBLRDL instruction is needed. The read operation is performed by loading TBLPAG and WREG with the address of the EEPROM location, followed by a TBLRDL instruction.

A typical read sequence, using the Table Pointer management (builtin_tblpage and builtin_tbloffset) and Table Read (builtin_tblrdl) procedures from the C30 compiler library, is provided in Example 6-5.

Program Space Visibility (PSV) can also be used to read locations in the data EEPROM.

**EXAMPLE 6-5: READING THE DATA EEPROM USING THE TBLRD COMMAND**

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
int data;                                               // Data read from EEPROM
/*-----------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the read
-----------------------------------------------------------------------------------------------
*/
    unsigned int offset;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);                // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);              // Initizlize lower word of address
    data = __builtin_tblrdl(offset);                    // Write EEPROM data to write latch
```

#### 7.2.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer (OST) has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

#### 7.2.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

### 7.3 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSCx bits in the Flash Configuration Word (FOSCSEL<2:0>); see Table 7-2. The RCFGCAL and NVMCON registers are only affected by a POR.

### 7.4 Brown-out Reset (BOR)

The PIC24FXXXXX family devices implement a BOR circuit, which provides the user several configuration and power-saving options. The BOR is controlled by the BORV<1:0> and BOREN<1:0> Configuration bits (FPOR<6:5,1:0>). There are a total of four BOR configurations, which are provided in Table 7-3.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of $V_{DD}$ below the set threshold point will reset the device. The chip will remain in BOR until $V_{DD}$ rises above the threshold.

If the Power-up Timer is enabled, it will be invoked after $V_{DD}$ rises above the threshold. Then, it will keep the chip in Reset for an additional time delay, $T_{PWRT}$, if $V_{DD}$ drops below the threshold while the Power-up Timer is running. The chip goes back into a BOR and the Power-up Timer will be initialized. Once $V_{DD}$ rises above the threshold, the Power-up Timer will execute the additional time delay.

BOR and the Power-up Timer (PWRT) are independently configured. Enabling the Brown-out Reset does not automatically enable the PWRT.

#### 7.4.1 LOW-POWER BOR (LPBOR)

The Low-Power BOR is an alternate setting for the BOR, designed to consume minimal power. In LPBOR mode, BORV<1:0> (FPOR<6:5>) = 00. The BOR trip point is approximately 2.0V. Due to the low current consumption, the accuracy of the LPBOR mode can vary.

Unlike the other BOR modes, LPBOR mode will not cause a device Reset when $V_{DD}$ drops below the trip point. Instead, it re-arms the POR circuit to ensure that the device will reset properly in the event that $V_{DD}$ continues to drop below the minimum operating voltage.

The device will continue to execute code when $V_{DD}$ is below the level of the LPBOR trip point. A device that requires falling edge BOR protection to prevent code from improperly executing should use one of the other BOR voltage settings.

**REGISTER 8-16: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DAC2IE | DAC1IE | CTMUIE | — | — | — | — | HLVDIE |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | U2ERIE | U1ERIE | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **DAC2IE:** Digital-to-Analog Converter 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **DAC1IE:** Digital-to-Analog Converter 1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

**REGISTER 8-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | NVMIP2 | NVMIP1 | NVMIP0 | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | AD1IP2 | AD1IP1 | AD1IP0 | — | U1TXIP2 | U1TXIP1 | U1TXIP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **NVMIP<2:0>:** NVM Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** A/D Conversion Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

**REGISTER 8-30: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | U2ERIP2 | U2ERIP1 | U2ERIP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | U1ERIP2 | U1ERIP1 | U1ERIP0 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

## 11.0 I/O PORTS

| | |
|---|---|
| **Note:** | This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the I/O ports, refer to the *"PIC24F Family Reference Manual"*, **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711). Note that the PIC24FV16KM204 family devices do not support Peripheral Pin Select features. |

All of the device pins (except VDD and VSS) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

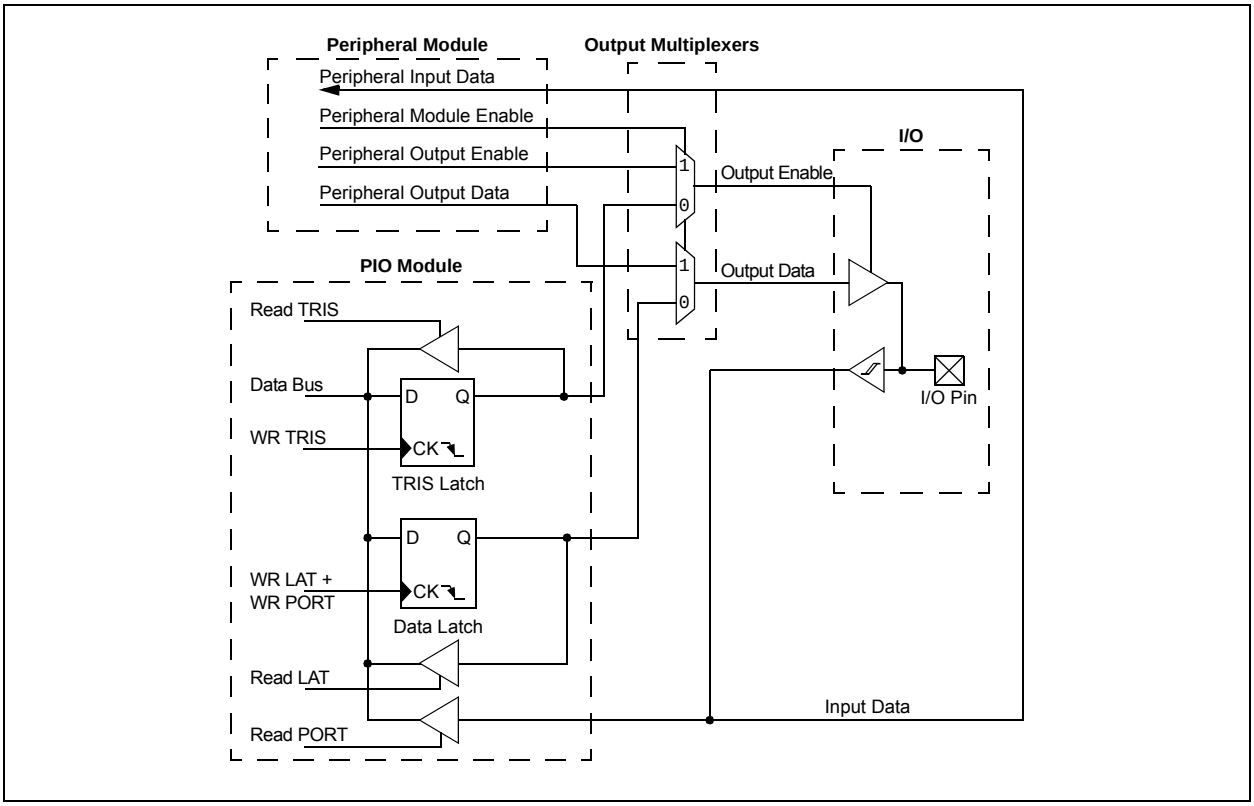
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Data Latch register (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**



## 16.3 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value, loaded into the lower half of RCFGCAL, is multiplied by four and will be either added or subtracted from the RTCC timer, once every minute. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute.
3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGCAL register value must be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

   b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGCAL register value must be positive. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

**EQUATION 16-1:**

(Ideal Frequency† – Measured Frequency) *
60 = Clocks per Minute

† Ideal Frequency = 32,768 Hz

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse, except when SECONDS = 00, 15, 30 or 45. This is due to the auto-adjust of the RTCC at 15 second intervals.

| **Note:** | It is up to the user to include, in the error value, the initial error of the crystal: drift due to temperature and drift due to crystal aging. |
|---|---|

## 16.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>)
- One-time alarm and repeat alarm options are available

### 16.4.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 16-2, the interval selection of the alarm is configured through the AMASKx bits (ALCFGRPT<13:10>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT<7:0> bits (ALCFGRPT<7:0>). When the value of the ARPTx bits equals 00h and the CHIME bit (ALCFGRPT<14>) is cleared, the repeat function is disabled, and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT<7:0> with FFh.

After each alarm is issued, the value of the ARPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

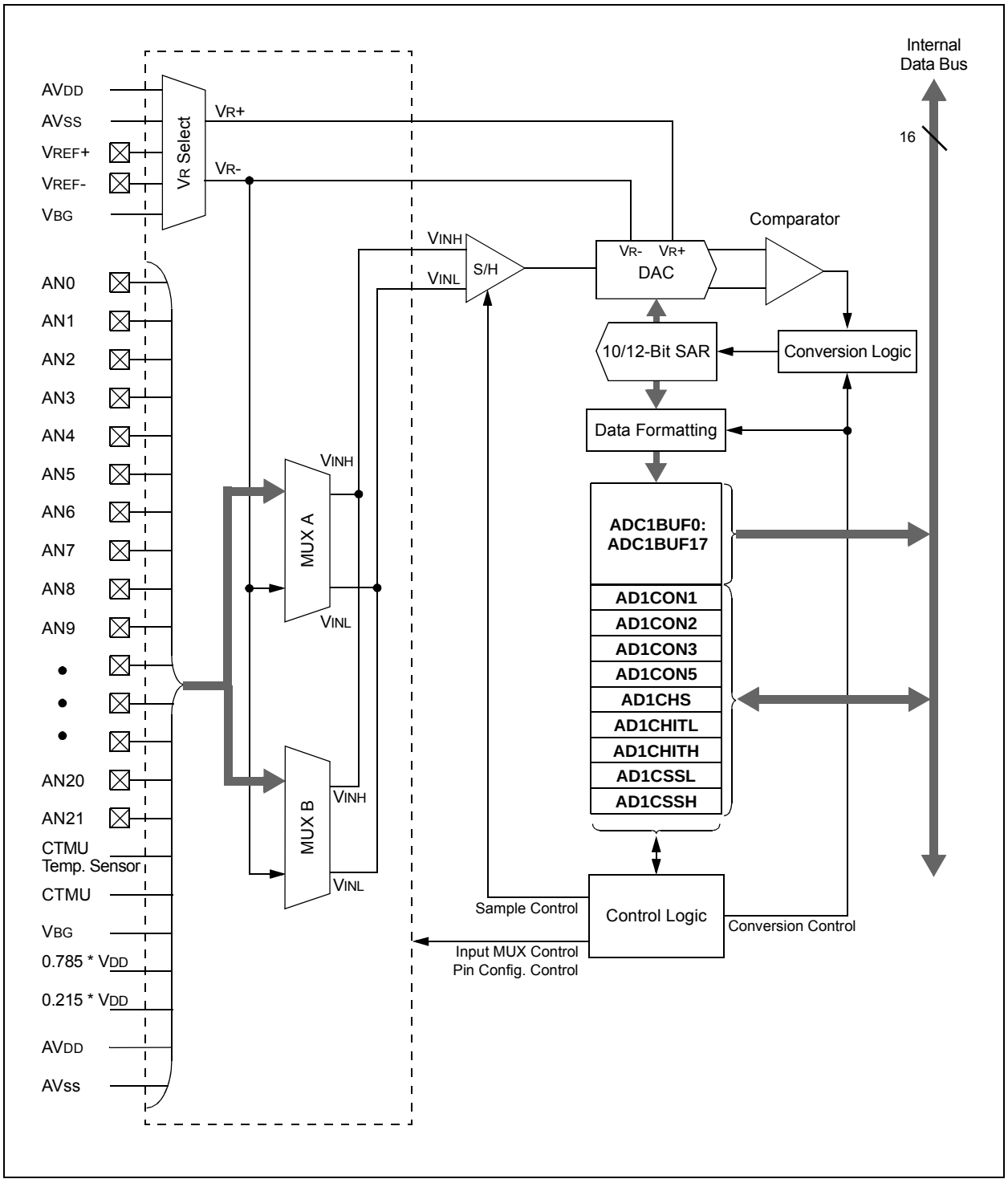
Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ARPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

### 16.4.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to other peripherals.

| **Note:** | Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers, and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0. |
|---|---|

**FIGURE 19-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM**



**REGISTER 19-1: AD1CON1: A/DA/D CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | — | — | MODE12 | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0, HSC | R/C-0, HSC |
|---|---|---|---|---|---|---|---|
| SSRC3 | SSRC2 | SSRC1 | SSRC0 | — | ASAM | SAMP | DONE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter is operating
0 = A/D Converter is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **MODE12:** 12-Bit A/D Operation Mode bit
1 = 12-bit A/D operation
0 = 10-bit A/D operation

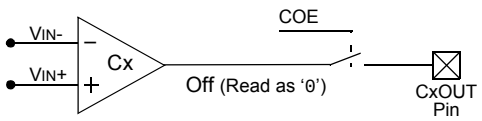
bit 9-8 **FORM<1:0>:** Data Output Format bits (see the following formats)
11 = Fractional result, signed, left justified
10 = Absolute fractional result, unsigned, left justified
01 = Decimal result, signed, right justified
00 = Absolute decimal result, unsigned, right justified

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits
1111 = Reserved
•
•
•
1101 = Reserved
1100 = CLC2 event ends sampling and starts conversion
1011 = SCCP4 Compare Event (CCP4IF) ends sampling and starts conversion
1010 = MCCP3 Compare Event (CCP3IF) ends sampling and starts conversion
1001 = MCCP2 Compare Event (CCP2IF) ends sampling and starts conversion
1000 = CLC1 event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = TMR1 Sleep mode Trigger event ends sampling and starts conversion(1)
0101 = TMR1 event ends sampling and starts conversion
0100 = CTMU event ends sampling and starts conversion
0011 = SCCP5 Compare Event (CCP5IF) ends sampling and starts conversion
0010 = MCCP1 Compare Event (CCP1IF) ends sampling and starts conversion
0001 = INT0 event ends sampling and starts conversion
0000 = Clearing the Sample bit ends sampling and starts conversion

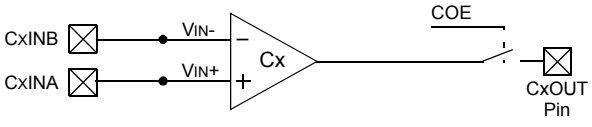
**Note 1:** This version of the TMR1 Trigger allows A/D conversions to be triggered from TMR1 while the device is operating in Sleep mode. The SSRC<3:0> = 0101 option allows conversions to be triggered in Run or Idle modes only.

**FIGURE 22-2: INDIVIDUAL COMPARATOR CONFIGURATIONS**

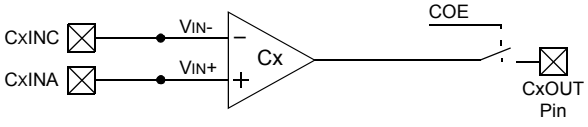
**Comparator Off**
**CON = 0, CREF<1:0> = xx, CCH<1:0> = xx**



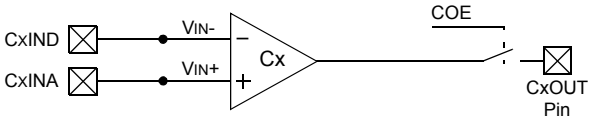

**Comparator CxINB > CxINA Compare**
**CON = 1, CREF<1:0> = 00, CCH<1:0> = 00**



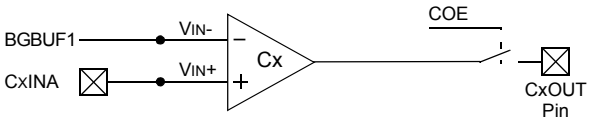

**Comparator CxINC > CxINA Compare**
**CON = 1, CREF<1:0> = 00, CCH<1:0> = 01**



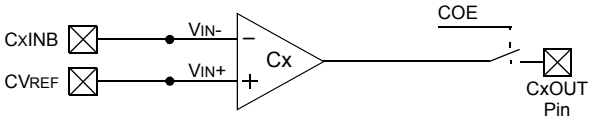

**Comparator CxIND > CxINA Compare**
**CON = 1, CREF<1:0> = 00, CCH<1:0> = 10**



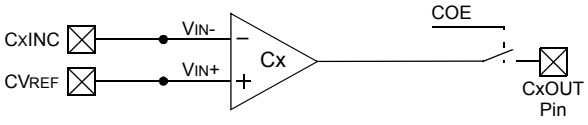

**Comparator BGBUF1 > CxINA Compare**
**CON = 1, CREF<1:0> = 00, CCH<1:0> = 11**



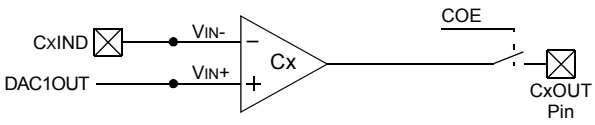

**Comparator CxINB > CVREF Compare**
**CON = 1, CREF<1:0> = 01, CCH<1:0> = 00**



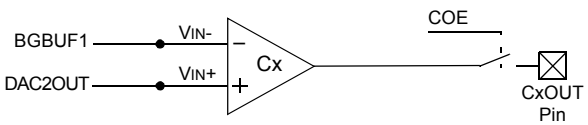

**Comparator CxINC > CVREF Compare**
**CON = 1, CREF<1:0> = 01, CCH<1:0> = 01**




**Comparator CxIND > DAC1OUT Compare**
**CON = 1, CREF<1:0> = 10, CCH<1:0> = 10**




**Comparator BGBUF1 > DAC2OUT Compare**
**CON = 1, CREF<1:0> = 11, CCH<1:0> = 11**



**REGISTER 23-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CVREN | CVROE | CVRSS | CVR4 | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = CVREF circuit is powered on
0 = CVREF circuit is powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit
1 = CVREF voltage level is output on the CVREF pin
0 = CVREF voltage level is disconnected from the CVREF pin

bit 5 **CVRSS:** Comparator VREF Source Selection bit
1 = Comparator reference source, CVRSRC = VREF+ – VREF-
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 4-0 **CVR<4:0>:** Comparator VREF Value Selection 0 ≤ CVR<4:0> ≤ 31 bits
When CVRSS = 1:
CVREF = (VREF-) + (CVR<4:0>/32) • (VREF+ – VREF-)
When CVRSS = 0:
CVREF = (AVSS) + (CVR<4:0>/32) • (AVDD – AVSS)

**TABLE 27-26: COMPARATOR TIMING REQUIREMENTS**

| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|---|
| 300 | TRESP | Response Time*(1) | — | 150 | 400 | ns | |
| 301 | TMC2OV | Comparator Mode Change to Output Valid* | — | — | 10 | μs | |

* Parameters are characterized but not tested.

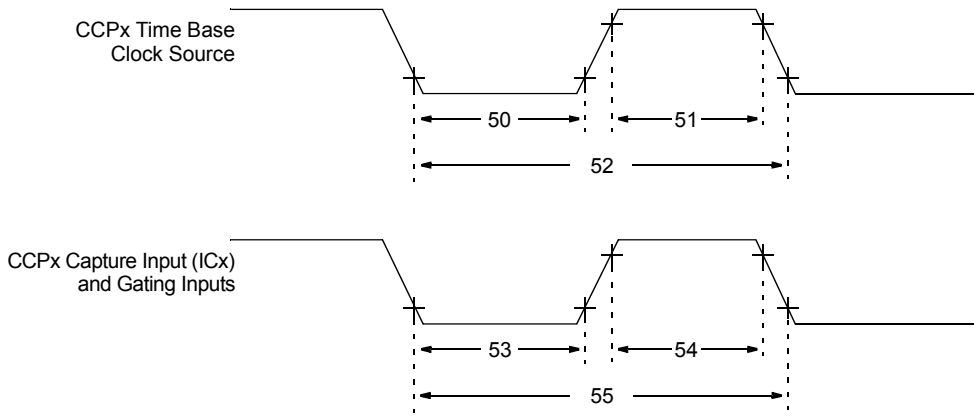
**Note 1:** Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**TABLE 27-27: COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS**

| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|---|
| VR310 | TSET | Settling Time(1) | — | — | 10 | μs | |

**Note 1:** Settling time is measured while CVRSS = 1 and the CVR<3:0> bits transition from '0000' to '1111'.

**FIGURE 27-10: CAPTURE/COMPARE/PWM TIMINGS (MCCPx, SCCPx MODULES)**

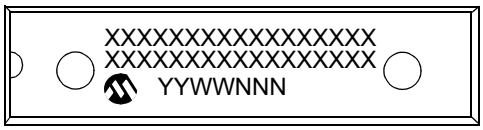



**Note:** Refer to Figure 27-5 for load conditions.

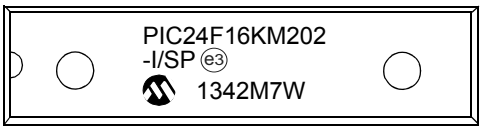
**TABLE 27-28: CAPTURE/COMPARE/PWM REQUIREMENTS (MCCPx, SCCPx MODULES)**

| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 50 | TCLKL | CCPx Time Base Clock Source Low Time | TCY/2 | — | ns | |
| 51 | TCLKH | CCPx Time Base Clock Source High Time | TCY/2 | — | ns | |
| 52 | TCLK | CCPx Time Base Clock Source Period | TCY | — | ns | |
| 53 | TCCL | CCPx Capture or Gating Input Low Time | TCLK | — | ns | |
| 54 | TCCH | CCPx Capture or Gating Input High Time | TCLK | — | ns | |
| 55 | TCCP | CCPx Capture or Gating Input Period | 2 * TCLK/N | — | ns | N = Prescale Value (1, 4 or 16) |

28-Lead SPDIP (.300")

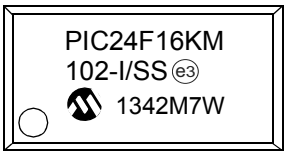



Example

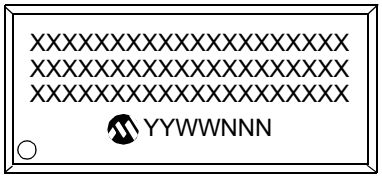



28-Lead SSOP (5.30 mm)

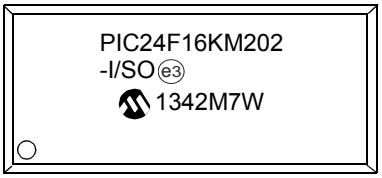

Example



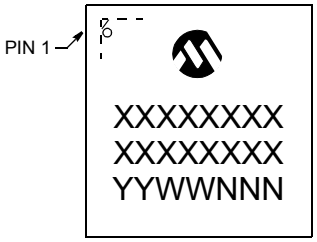

28-Lead SOIC (7.50 mm)



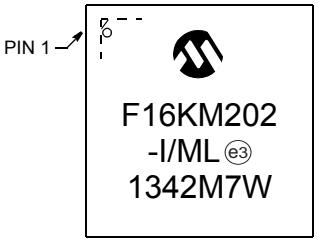

Example



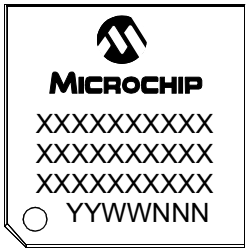

28-Lead QFN (6x6 mm)



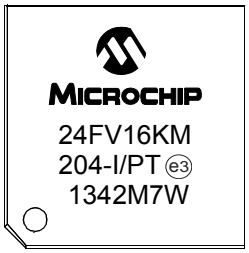

Example




44-Lead TQFP (10x10x1 mm)

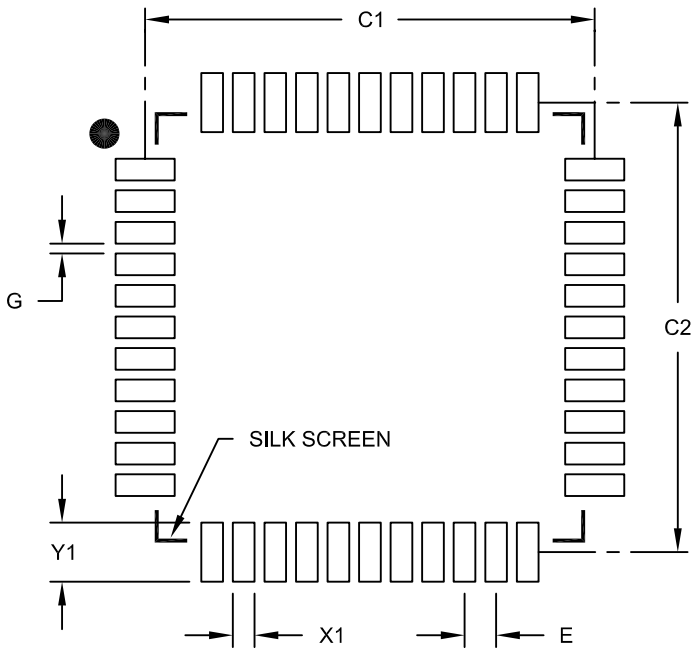



Example



44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.80 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X44) | X1 | | | 0.55 |
| Contact Pad Length (X44) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

# Worldwide Sales and Service

## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Cleveland**
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

**Indianapolis**
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

**Santa Clara**
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

**Toronto**
Mississauga, Ontario, Canada
Tel: 905-673-0699
Fax: 905-673-6509

## ASIA/PACIFIC

**Asia Pacific Office**
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

**Australia - Sydney**
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

**China - Beijing**
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

**China - Chengdu**
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

**China - Chongqing**
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

**China - Hangzhou**
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

**China - Hong Kong SAR**
Tel: 852-2943-5100
Fax: 852-2401-3431

**China - Nanjing**
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

**China - Qingdao**
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

**China - Shanghai**
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

**China - Shenyang**
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

**China - Shenzhen**
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

**China - Wuhan**
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

**China - Xian**
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

**China - Xiamen**
Tel: 86-592-2388138
Fax: 86-592-2388130

**China - Zhuhai**
Tel: 86-756-3210040
Fax: 86-756-3210049

## ASIA/PACIFIC

**India - Bangalore**
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

**India - New Delhi**
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

**India - Pune**
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

**Japan - Osaka**
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

**Japan - Tokyo**
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

**Korea - Daegu**
Tel: 82-53-744-4301
Fax: 82-53-744-4302

**Korea - Seoul**
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

**Malaysia - Kuala Lumpur**
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

**Malaysia - Penang**
Tel: 60-4-227-8870
Fax: 60-4-227-4068

**Philippines - Manila**
Tel: 63-2-634-9065
Fax: 63-2-634-9069

**Singapore**
Tel: 65-6334-8870
Fax: 65-6334-8850

**Taiwan - Hsin Chu**
Tel: 886-3-5778-366
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**
Tel: 886-7-213-7828
Fax: 886-7-330-9305

**Taiwan - Taipei**
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

**Thailand - Bangkok**
Tel: 66-2-694-1351
Fax: 66-2-694-1350

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4450-2828
Fax: 45-4485-2829

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**UK - Wokingham**
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/12