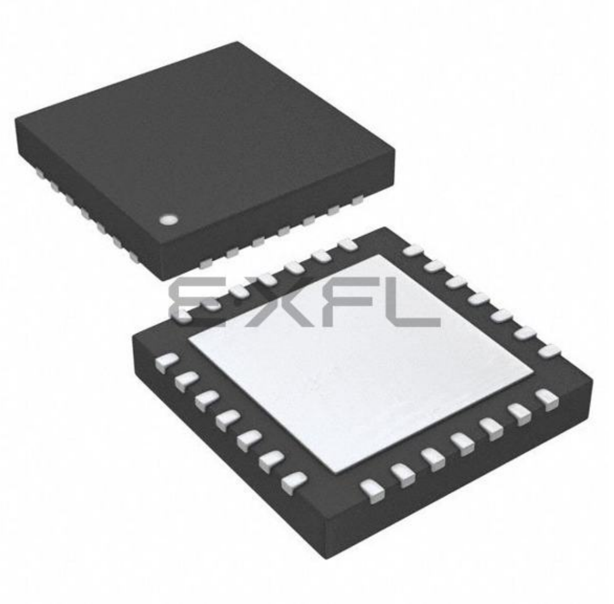


Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km202-i-ml

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Analog Inputs
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	A/D Analog Inputs
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	A/D Analog Inputs
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	A/D Analog Inputs
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	A/D Analog Inputs
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	A/D Analog Inputs
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	A/D Analog Inputs
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	A/D Analog Inputs
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	A/D Analog Inputs
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	A/D Analog Inputs
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	A/D Analog Inputs
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	A/D Analog Inputs
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	A/D Analog Inputs
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	A/D Analog Inputs
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	A/D Analog Inputs
AN16	10	12	9	34	37	10	12	9	34	37	I	ANA	A/D Analog Inputs
AN17	—	14	11	41	45	—	14	11	41	45	I	ANA	A/D Analog Inputs
AN18	—	15	12	42	46	—	15	12	42	46	I	ANA	A/D Analog Inputs
AN19	11	16	13	43	47	11	16	13	43	47	I	ANA	A/D Analog Inputs
AN20	12	17	14	44	48	12	17	14	44	48	I	ANA	A/D Analog Inputs
AN21	13	18	15	1	1	13	18	15	1	1	I	ANA	A/D Analog Inputs
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I^2C™	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I^2C	Alternate I2C1 Data Input/Output
AVDD	20	28	25	17	18	20	28	25	17	18	P	—	A/D Supply Pins
AVSS	19	27	24	16	17	19	27	24	16	17	P	—	A/D Supply Pins
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

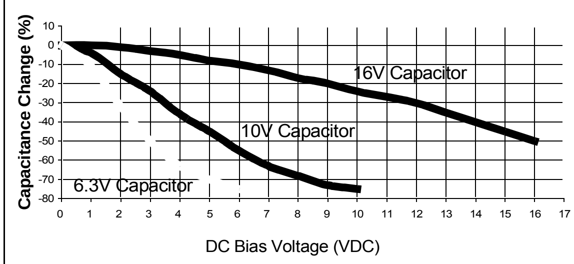
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 3.3V or 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pins, Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 26.0 "Development Support"**.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	80h	NSTDIS	—	—	—	—	—	—	—	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	82h	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	84h	NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	CCT2IF	CCT1IF	CCP4IF	CCP3IF	—	T1IF	CCP2IF	CCP1IF	INT0IF	0000
IFS1	86h	U2TXIF	U2RXIF	INT2IF	CCT4IF	CCT3IF	—	—	—	—	CCP5IF	—	INT1IF	CNIF	CMIF	BCL1IF	SSP1IF	0000
IFS2	88h	—	—	—	—	—	—	CCT5IF	—	—	—	—	—	—	—	—	—	0000
IFS3	8Ah	—	RTCIF	—	—	—	—	—	—	—	—	—	—	—	BCL2IF	SSP2IF	—	0000
IFS4	8Ch	DAC2IF	DAC1IF	CTMUIF	—	—	—	—	HLVDIF	—	—	—	—	—	U2ERIF	U1ERIF	—	0000
IFS5	8Eh	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIF	0000
IFS6	90h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC2IF	CLC1IF	0000
IEC0	94h	NVMIE	—	AD1IE	U1TXIE	U1RXIE	—	—	CCT2IE	CCT1IE	CCP4IE	CCP3IE	—	T1IE	CCP2IE	CCP1IE	INT0IE	0000
IEC1	96h	U2TXIE	U2RXIE	INT2IE	CCT4IE	CCT3IE	—	—	—	—	CCP5IE	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE	0000
IEC2	98h	—	—	—	—	—	—	CCT5IE	—	—	—	—	—	—	—	—	—	0000
IEC3	9Ah	—	RTCIE	—	—	—	—	—	—	—	—	—	—	—	BCL2IE	SSP2IE	—	0000
IEC4	9Ch	DAC2IE	DAC1IE	CTMUIE	—	—	—	—	HLVDIE	—	—	—	—	—	U2ERIE	U1ERIE	—	0000
IEC5	9Eh	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIE	0000
IEC6	A0h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLC2IE	CLC1IE	0000
IPC0	A4h	—	T1IP2	T1IP1	T1IP0	—	CCP2IP2	CCP2IP1	CCP2IP0	—	CCP1IP2	CCP1IP1	CCP1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	A6h	—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP4IP2	CCP4IP1	CCP4IP0	—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—	4440
IPC2	A8h	—	U1RXIP2	U1RXIP1	U1RXIP0	—	—	—	—	—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0	4004
IPC3	AAh	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	ACh	—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0	—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0	4444
IPC5	AEh	—	—	—	—	—	CCP5IP2	CCP5IP1	CCP5IP0	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0404
IPC6	B0h	—	CCT3IP2	CCT3IP1	CCT3IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC7	B2h	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	CCT4IP2	CCT4IP1	CCT4IP0	4444
IPC10	B8h	—	—	—	—	—	—	—	—	—	CCT5IP2	CCT5IP1	CCT5IP0	—	—	—	—	0040
IPC12	BCh	—	—	—	—	—	BCL2IP2	BCL2IP1	BCL2IP0	—	SSP2IP2	SSP2IP1	SSP2IP0	—	—	—	—	0440
IPC15	C2h	—	—	—	—	—	RTCIP2	RTCIP1	RTCIP0	—	—	—	—	—	—	—	—	0400
IPC16	C4h	—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0	—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—	0440
IPC18	C8h	—	—	—	—	—	—	—	—	—	—	—	—	—	HLVDIP2	HLVDIP1	HLVDIP0	0004
IPC19	CAh	—	DAC2IP2	DAC2IP1	DAC2IP0	—	DAC1IP2	DAC1IP1	DAC1IP0	—	CTMUIP2	CTMUIP1	CTMUIP0	—	—	—	—	4440
IPC20	CCh	—	—	—	—	—	—	—	—	—	—	—	—	—	ULPWUIP2	ULPWUIP1	ULPWUIP0	0004
IPC24	D4h	—	—	—	—	—	—	—	—	—	CLC2IP2	CLC2IP1	CLC2IP0	—	CLC1IP2	CLC1IP1	CLC1IP0	0044
INTTREG	E0h	CPUIRQ	—	VHOLD	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 – ADC1 Convert Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
CLC1	96	0000D4h	0001D4h	IFS6<0>	IEC6<0>	IPC24<2:0>
CLC2	97	0000D6h	0001D6h	IFS6<1>	IEC6<1>	IPC24<6:4>
Comparator Interrupt	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>
CTMU	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
DAC1 – Buffer Update	78	0000B0h	0001B0h	IFS4<14>	IEC4<14>	IPC19<10:8>
DAC2 – Buffer Update	79	0000B2h	0001B2h	IFS4<15>	IEC4<15>	IPC19<14:12>
HLVD – High/Low-Voltage Detect	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC18<2:0>
ICN – Input Change Notification	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
INT0 – External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>
INT1 – External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
INT2 – External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
MCCP1 – Capture/Compare	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>
MCCP1 – Time Base	7	000022h	000122h	IFS0<7>	IEC0<7>	IPC1<14:12>
MCCP2 – Capture/Compare	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>
MCCP2 – Time Base	8	000024h	000124h	IFS0<8>	IEC0<8>	IPC2<2:0>
MCCP3 – Capture/Compare	5	00001Eh	00011Eh	IFS0<5>	IEC0<5>	IPC1<6:4>
MCCP3 – Time Base	27	00004Ah	00014Ah	IFS1<11>	IEC1<11>	IPC6<14:12>
MSSP1 – Bus Collision Interrupt	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>
MSSP1 – I^{2}C™/SPI Interrupt	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>
MSSP2 – Bus Collision Interrupt	50	000078h	000178h	IFS3<2>	IEC3<2>	IPC12<10:8>
MSSP2 – I^{2}C/SPI Interrupt	49	000076h	000176h	IFS3<1>	IEC3<1>	IPC12<6:4>
NVM – NVM Write Complete	15	000032h	000132h	IFS0<15>	IEC0<15>	IPC3<14:12>
RTCC – Real-Time Clock/Calendar	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>
SCCP4 – Capture/Compare	6	000020h	000120h	IFS0<6>	IEC0<6>	IPC1<10:8>
SCCP4 – Time Base	28	00004Ch	00014Ch	IFS1<12>	IEC1<12>	IPC7<2:0>
SCCP5 – Capture/Compare	22	000040h	000140h	IFS1<6>	IEC1<6>	IPC5<10:8>
SCCP5 – Time Base	41	000066h	000166h	IFS2<9>	IEC2<9>	IPC10<6:4>
TMR1 – Timer1	3	00001Ah	00011Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
UART1 Error	65	000096h	000196h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART2 Error	66	000098h	000198h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART1RX – UART1 Receiver	11	00002Ah	00012Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1TX – UART1 Transmitter	12	00002Ch	00012Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2RX – UART2 Receiver	30	000050h	000150h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2TX – UART2 Transmitter	31	000052h	000152h	IFS1<15>	IEC1<15>	IPC7<14:12>
ULPWU – Ultra Low-Power Wake-up	80	0000B4h	0001B4h	IFS5<0>	IEC5<0>	IPC20<2:0>

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table (AIVT)
0 = Uses standard (default) Interrupt Vector Table (IVT)

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

REGISTER 8-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCP5IP2	CCP5IP1	CCP5IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

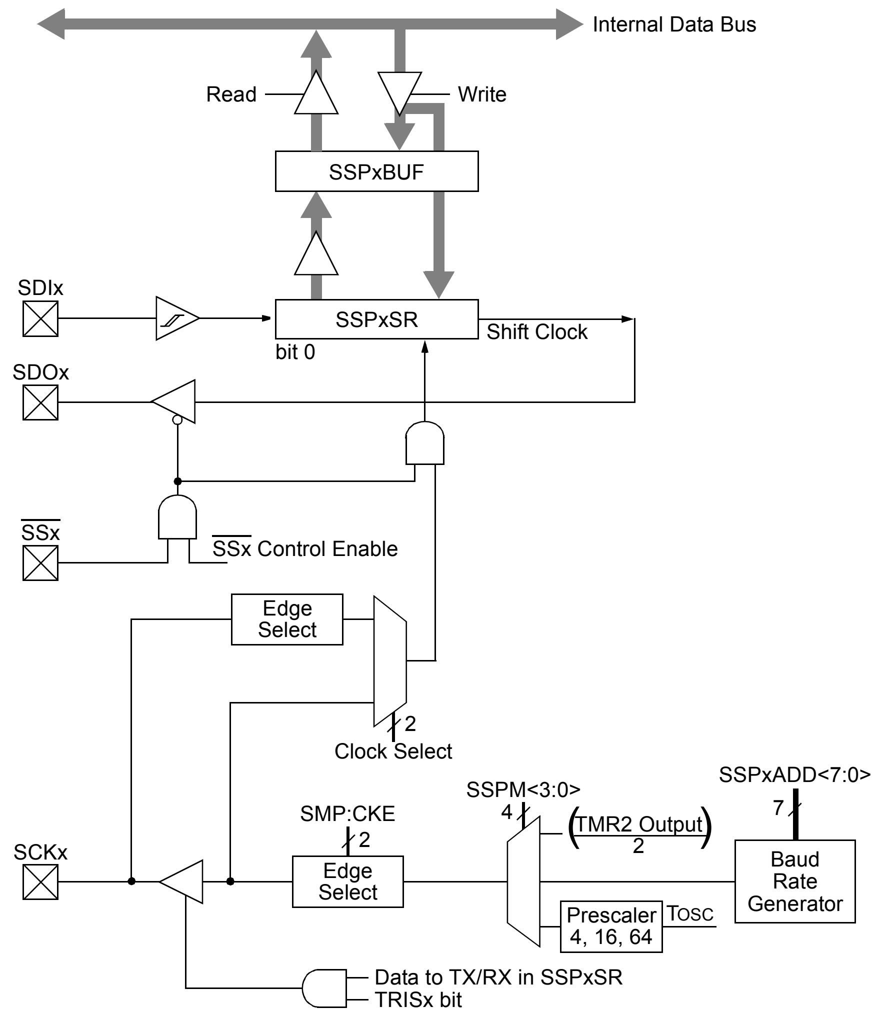
bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP5IP<2:0>:** Capture/Compare 5 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

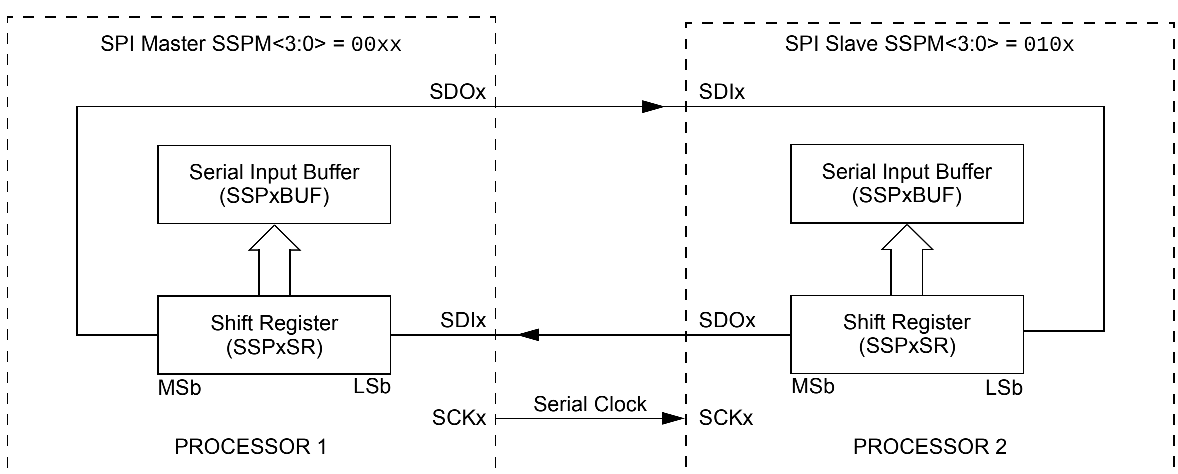
bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

FIGURE 14-1: MSSPx BLOCK DIAGRAM (SPI MODE)



Note: Refer to the device data sheet for pin multiplexing.

FIGURE 14-2: SPI MASTER/SLAVE CONNECTION

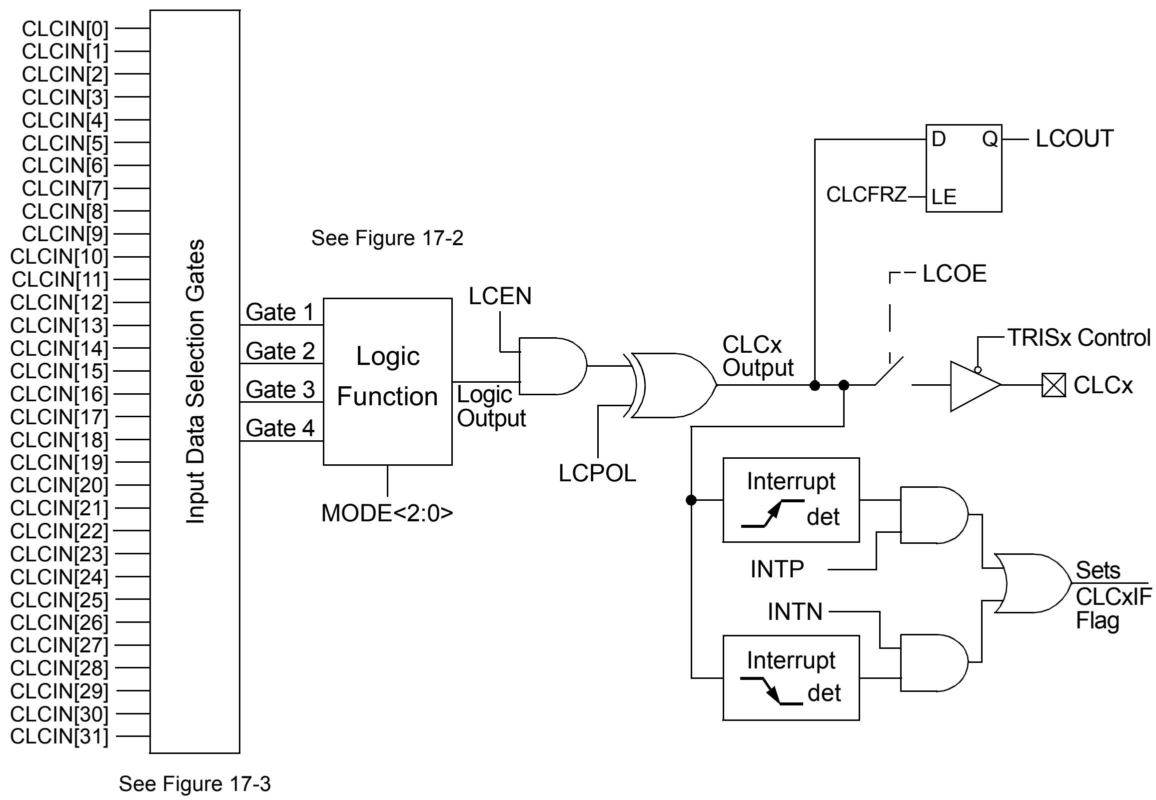


17.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 17-1 shows an overview of the module. Figure 17-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 17-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCONL register.

18.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

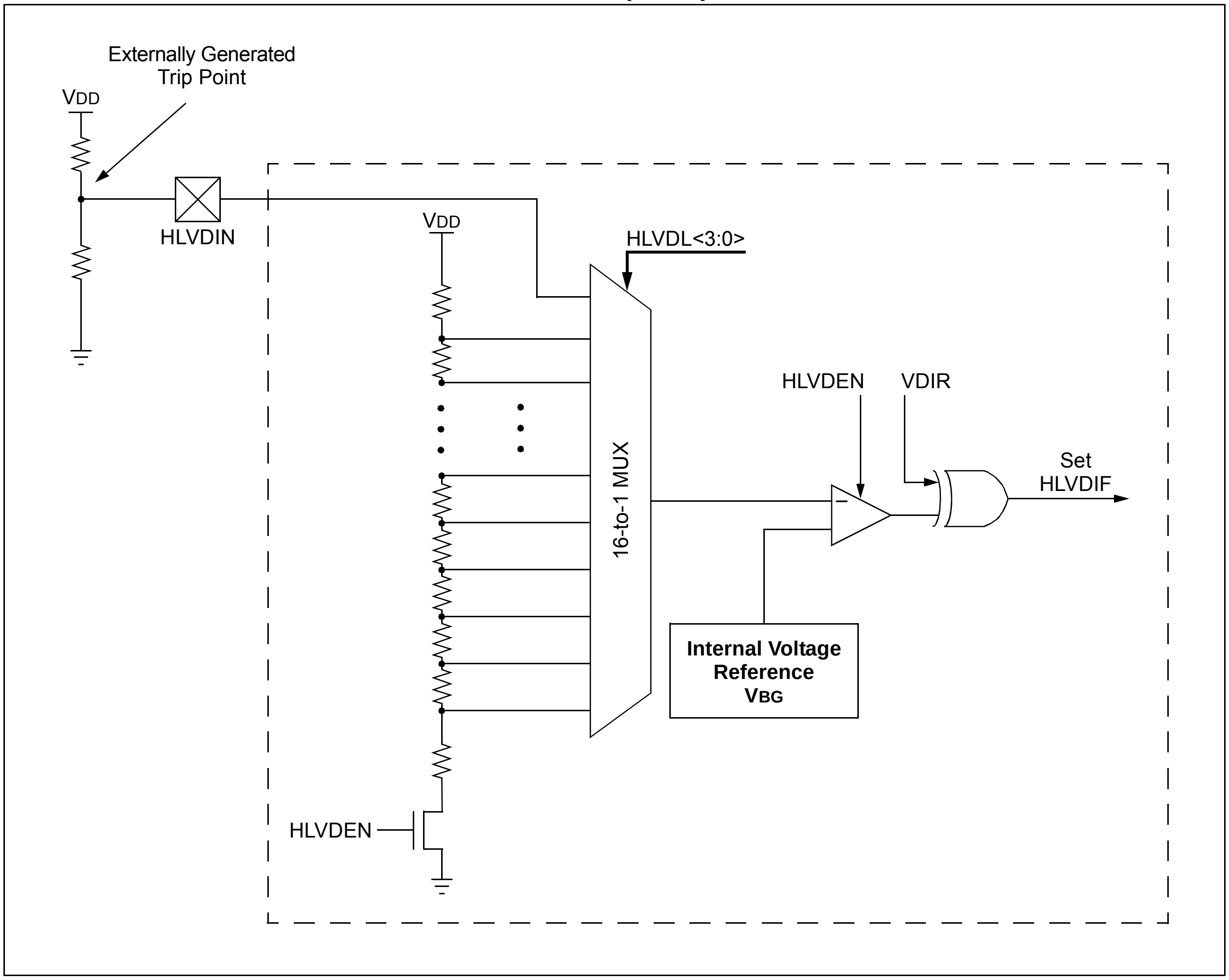
Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the *"PIC24F Family Reference Manual"*, **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725).

The High/Low-Voltage Detect module (HLVD) is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

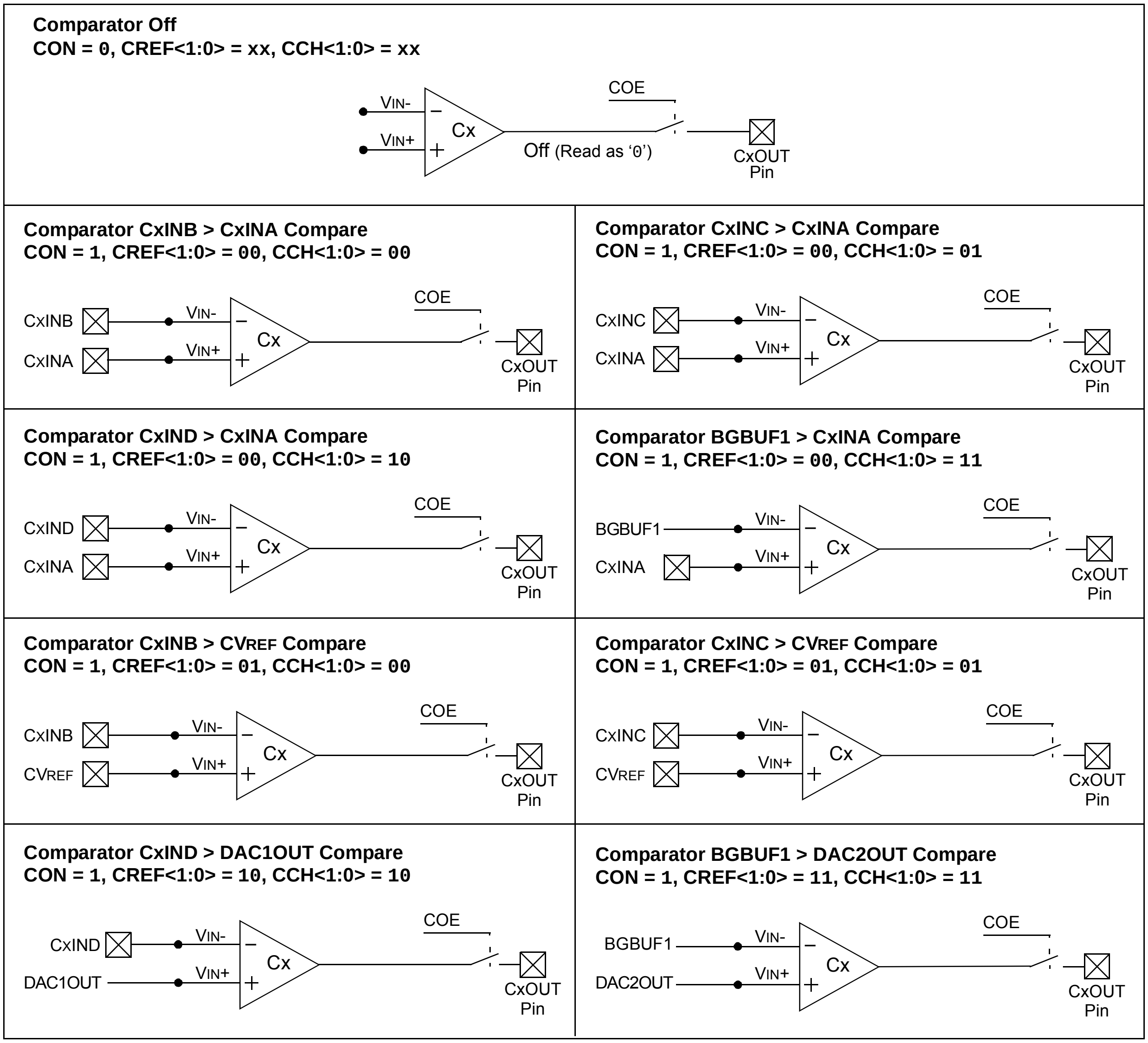
The HLVD Control register (see Register 18-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 18-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



NOTES:

FIGURE 22-2: INDIVIDUAL COMPARATOR CONFIGURATIONS



23.0 COMPARATOR VOLTAGE REFERENCE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to the *"PIC24F Family Reference Manual"*, **"Comparator Voltage Reference Module"** (DS39709).

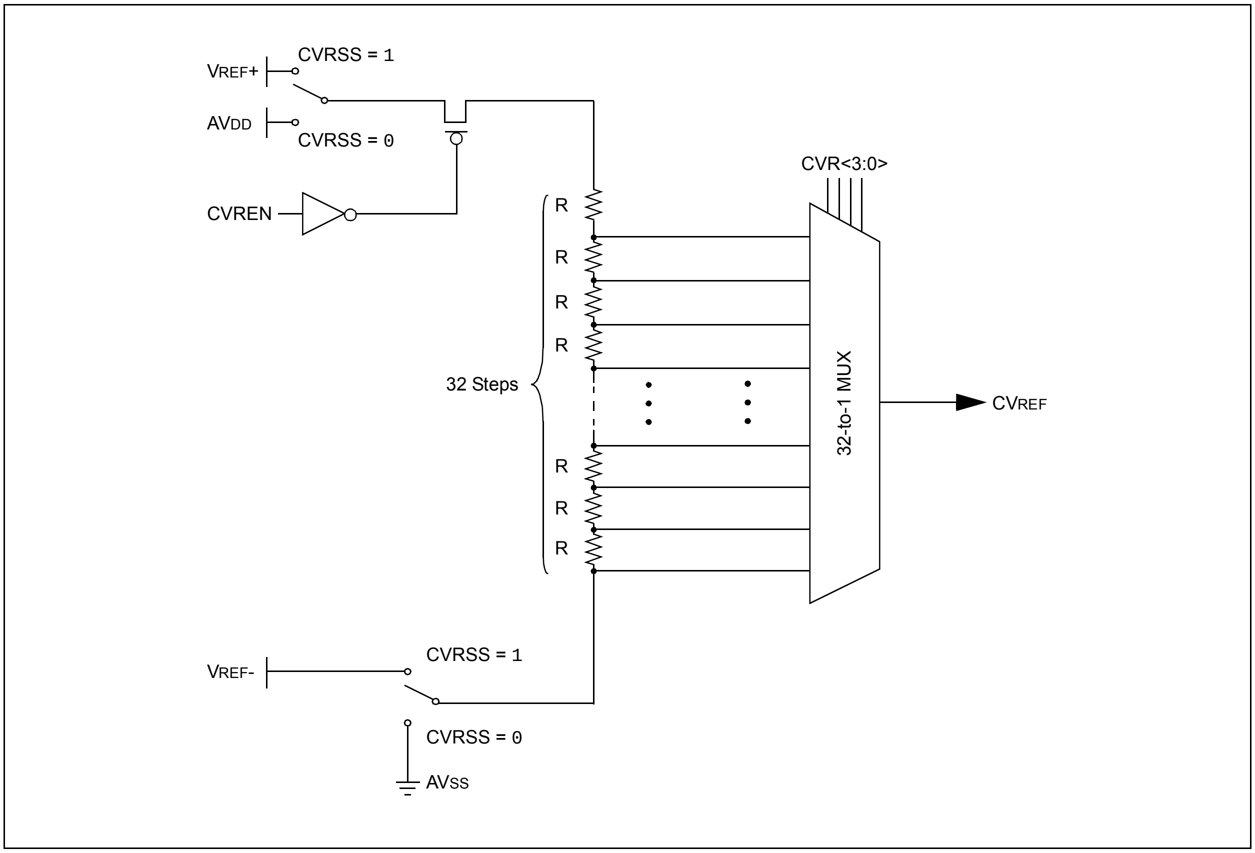
23.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 23-1). The comparator voltage reference provides a range of output voltages with 32 distinct levels.

The comparator voltage reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Edge 1 source is the Comparator 3 output
1110 = Edge 1 source is the Comparator 2 output
1101 = Edge 1 source is the Comparator 1 output
1100 = Edge 1 source is CLC2
1011 = Edge 1 source is CLC1
1010 = Edge 1 source is the MCCP2 Compare Event (CCP2IF)
1001 = Edge 1 source is CTED8(1)
1000 = Edge 1 source is CTED7(1)
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3(2)
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is the MCCP1 Compare Event (CCP1IF)
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

REGISTER 25-8: DEVID: DEVICE ID REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits

01000101 = PIC24FV16KM204 family

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits

00011111 = PIC24FV16KM204
00011011 = PIC24FV16KM202
00010111 = PIC24FV08KM204
00010011 = PIC24FV08KM202
00001111 = PIC24FV16KM104
00001011 = PIC24FV16KM102
00000011 = PIC24FV08KM102
00000001 = PIC24FV08KM101

00011110 = PIC24F16KM204
00011010 = PIC24F16KM202
00010110 = PIC24F08KM204
00010010 = PIC24F08KM202
00001110 = PIC24F16KM104
00001010 = PIC24F16KM102
00000010 = PIC24F08KM102
00000000 = PIC24F08KM101

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled in hardware (FWDTEN<1:0> = 11), it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) will need to be cleared in software after the device wakes up.

The WDT Flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

25.3.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

Windowed WDT mode is enabled by programming the Configuration bit, WINDIS (FWDT<6>), to ‘0’.

25.3.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN<1:0> Configuration bits. When both of the FWDTEN<1:0> Configuration bits are set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN<1:0> Configuration bits have been programmed to ‘10’. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments, and disable the WDT during non-critical segments, for maximum power savings. When the FWDTEN<1:0> bits are set to ‘01’, the WDT is only enabled in Run and Idle modes, and is disabled in Sleep. Software control of the SWDTEN bit (RCON<5>) is disabled with this setting.

FIGURE 25-2: WDT BLOCK DIAGRAM

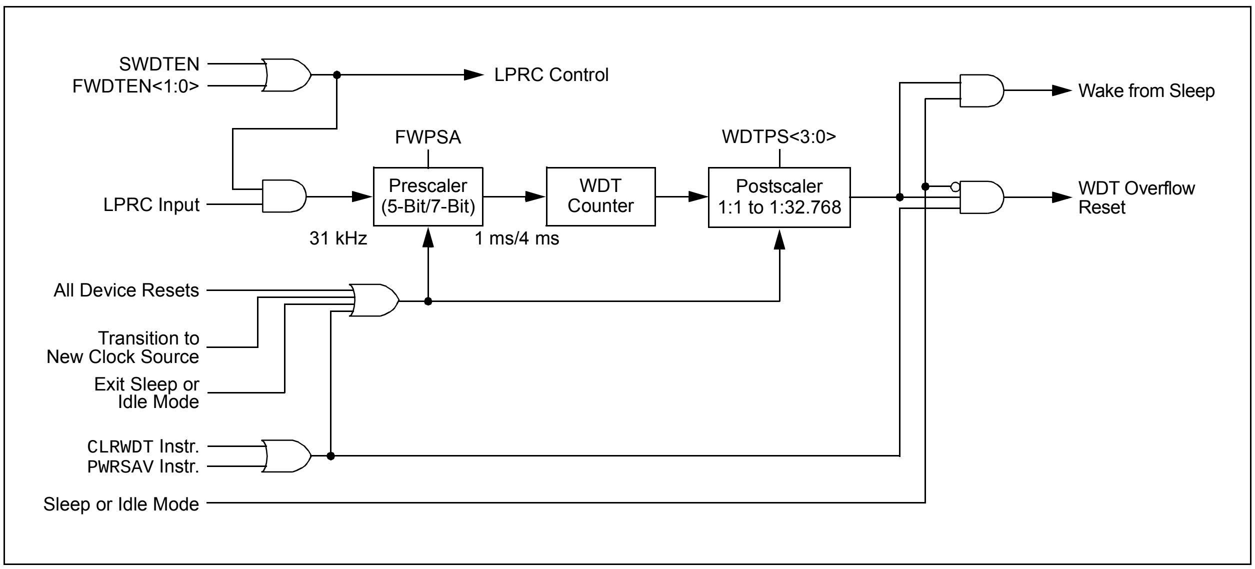


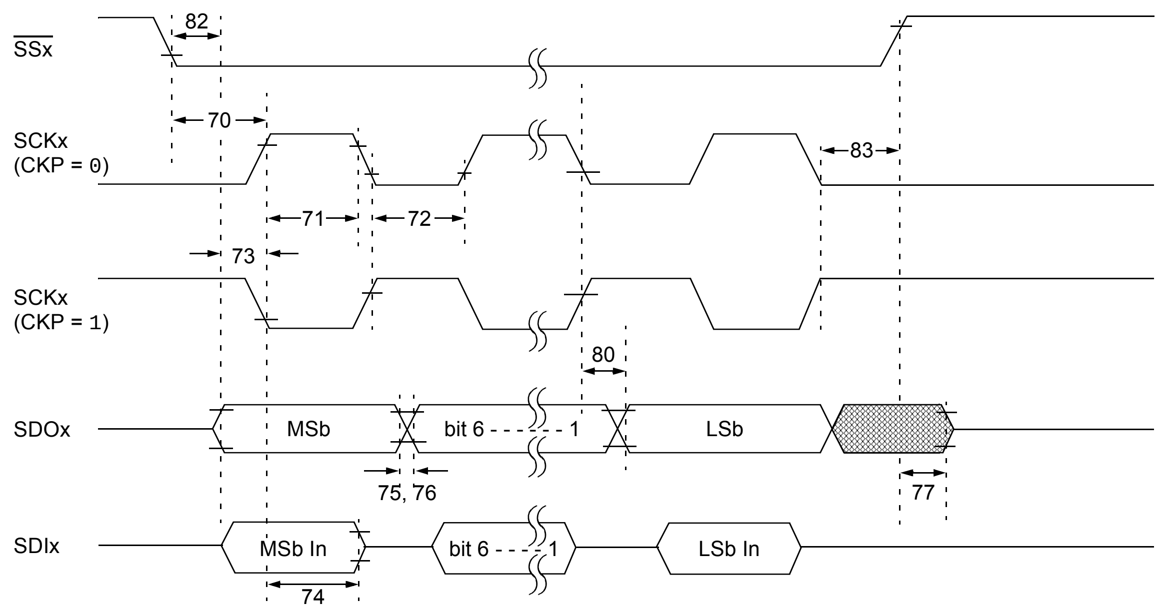
TABLE 27-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX) 2.0V to 5.5V (PIC24FV16KMXXX) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Device**	**Typical**	**Max**	**Units**	**Conditions**	
IDD Current						
D20	PIC24FV16KMXXX	269	450	µA	2.0V	0.5 MIPS, FOSC = 1 MHz(1)
		465	830	µA	5.0V	
	PIC24F16KMXXX	200	330	µA	1.8V	
		410	750	µA	3.3V	
DC22	PIC24FV16KMXXX	490	—	µA	2.0V	1 MIPS, FOSC = 2 MHz(1)
		880	—	µA	5.0V	
	PIC24F16KMXXX	407	—	µA	1.8V	
		800	—	µA	3.3V	
DC24	PIC24FV16KMXXX	13.0	15.0	mA	5.0V	16 MIPS, FOSC = 32 MHz(1)
	PIC24F16KMXXX	12.0	13.0	mA	3.3V	
DC26	PIC24FV16KMXXX	2.0	—	mA	2.0V	FRC (4 MIPS), FOSC = 8 MHz
		3.5	—	mA	5.0V	
	PIC24F16KMXXX	1.80	—	mA	1.8V	
		3.40	—	mA	3.3V	
DC30	PIC24FV16KMXXX	48.0	250	µA	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
		75.0	275	µA	5.0V	
	PIC24F16KMXXX	8.1	28.0	µA	1.8V	
		13.50	55.00	µA	3.3V	

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: The oscillator is in External Clock mode (FOSCSEL<2:0> = `010`, FOSC<1:0> = `00`).

FIGURE 27-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-32: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

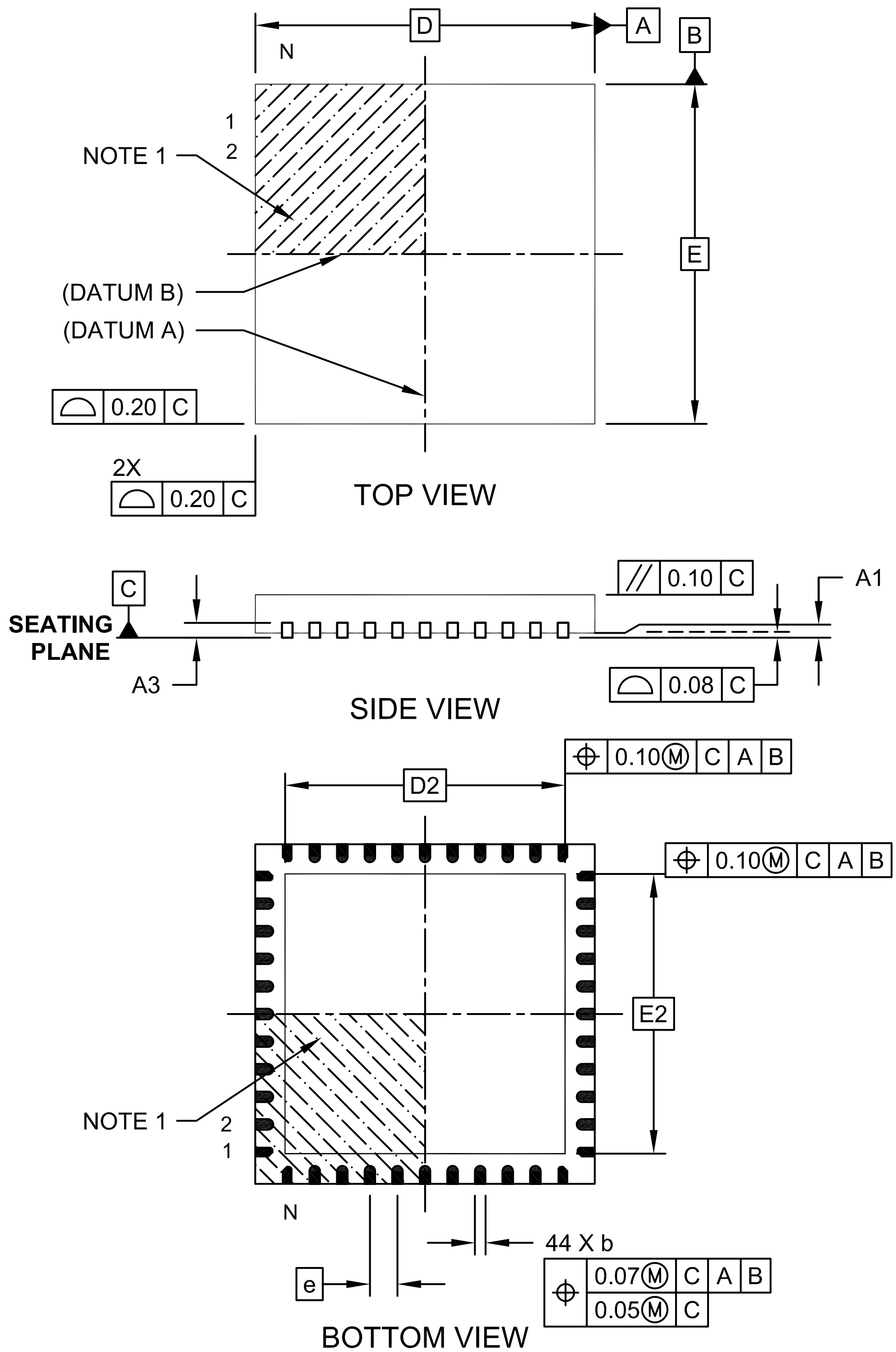
Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 TCY	—	ns	
70A	TssL2WB	$\overline{SSx}$ to Write to SSPxBUF		3 TCY	—	ns	
71	TscH	SCKx Input High Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
71A			Single Byte	40	—	ns	**(Note 1)**
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 TCY + 30	—	ns	
72A			Single Byte	40	—	ns	**(Note 1)**
73A	TB2B	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 TCY + 40	—	ns	**(Note 2)**
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time		—	25	ns	
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
82	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ ↓ Edge		—	50	ns	
83	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge		1.5 TCY + 40	—	ns	
	FSCK	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103C Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (February 2013)

Original data sheet for the PIC24FV16KM204 family of devices.

Revision B (July 2013)

Updates all references to PGCx and PGDx pin functions throughout the document to PGECx and PGEDx.

Updates **Section 4.0 "Memory Organization"** to change bit 12 in the following registers to reserved ("r" designation):

- CCP1CON1L (Table 4-8)
- CCP2CON1L (Table 4-9)
- CCP3CON1L (Table 4-10)
- CCP4CON1L (Table 4-11)
- CCP5CON1L (Table 4-12)

Updates **Section 13.0 "Capture/Compare/PWM/ Timer Modules (MCCP and SCCP)"**:

- Replaces bit 12 of CCPxCON1L (CCPSLP) and its description with a reserved bit
- Removes references to asynchronous operation in Sleep mode (and in other occurrences throughout the document)
- Modifies **Section 13.1 "Time Base Generator"** to add synchronous operation limitations; adds Table 13-1 to list valid clock options for all operating modes
- Removes the system clock as a time base input option
- Removes external input sources, comparators and CTMU as synchronization sources in Table 13-6; clarifies that other selected sources must be synchronous

Removes the input buffer from the band gap reference input in Figure 20-1.

Adds BUFCON0 register description (Register 20-2) to **Section 20.0 "8-Bit Digital-to-Analog Converter (DAC)"**.

Changes references to internal band gap voltages (V_{BG}, $V_{BG}/2$ and BGBUF0) in **Section 20.0 "8-Bit Digital-to-Analog Converter (DAC)"** and **Section 22.0 "Comparator Module"** to BGBUF1.

Adds minimum V_{DD} conditions for V_{BG} specification in Table 27-15 (Internal Voltage Regulator Specifications).

Other minor typographical corrections throughout the document.

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