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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km202-i-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km202-i-ss</a>

# PIC24FV16KM204 FAMILY

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- |                  |                 |
|------------------|-----------------|
| • PIC24FV08KM101 | • PIC24F08KM101 |
| • PIC24FV08KM102 | • PIC24F08KM102 |
| • PIC24FV16KM102 | • PIC24F16KM102 |
| • PIC24FV16KM104 | • PIC24F16KM104 |
| • PIC24FV08KM202 | • PIC24F08KM202 |
| • PIC24FV08KM204 | • PIC24F08KM204 |
| • PIC24FV16KM202 | • PIC24F16KM202 |
| • PIC24FV16KM204 | • PIC24F16KM204 |

The PIC24FV16KM204 family introduces many new analog features to the extreme low-power Microchip devices. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSC).

### 1.1 Core Features

#### 1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers. The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear Addressing of up to 16 Mbytes (program space) and 16 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32-bit by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as C
- Operational performance up to 16 MIPS

#### 1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FV16KM204 family incorporate a range of features that can significantly reduce power consumption during operation. Key features include:

- On-the-Fly Clock Switching, to allow the device clock to be changed under software control to the Timer1 source or the internal, low-power RC Oscillator during operation, allowing users to incorporate power-saving ideas into their software designs.
- Doze Mode Operation, when timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- Instruction-Based Power-Saving Modes, to allow the microcontroller to suspend all operations or selectively shut down its core while leaving its peripherals active with a single instruction in software.

#### 1.1.3 OSCILLATOR OPTIONS AND FEATURES

The PIC24FV16KM204 family offers five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock (EC) modes offering the option of a divide-by-2 clock output.
- Two Fast Internal Oscillators (FRCs), one with a nominal 8 MHz output and the other with a nominal 500 kHz output. These outputs can also be divided under software control to provide clock speed as low as 31 kHz or 2 kHz.
- A Phase Locked Loop (PLL) frequency multiplier, available to the external oscillator modes and the 8 MHz FRC Oscillator, which allows clock speeds of up to 32 MHz.
- A separate internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

**TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION**

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Analog Inputs
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	A/D Analog Inputs
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	A/D Analog Inputs
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	A/D Analog Inputs
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	A/D Analog Inputs
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	A/D Analog Inputs
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	A/D Analog Inputs
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	A/D Analog Inputs
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	A/D Analog Inputs
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	A/D Analog Inputs
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	A/D Analog Inputs
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	A/D Analog Inputs
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	A/D Analog Inputs
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	A/D Analog Inputs
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	A/D Analog Inputs
AN16	10	12	9	34	37	10	12	9	34	37	I	ANA	A/D Analog Inputs
AN17	—	14	11	41	45	—	14	11	41	45	I	ANA	A/D Analog Inputs
AN18	—	15	12	42	46	—	15	12	42	46	I	ANA	A/D Analog Inputs
AN19	11	16	13	43	47	11	16	13	43	47	I	ANA	A/D Analog Inputs
AN20	12	17	14	44	48	12	17	14	44	48	I	ANA	A/D Analog Inputs
AN21	13	18	15	1	1	13	18	15	1	1	I	ANA	A/D Analog Inputs
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I <sup>2</sup> C™	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I <sup>2</sup> C	Alternate I2C1 Data Input/Output
AVDD	20	28	25	17	18	20	28	25	17	18	P	—	A/D Supply Pins
AVSS	19	27	24	16	17	19	27	24	16	17	P	—	A/D Supply Pins
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)

**Legend:** ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)**

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
C1OUT	17	25	22	14	15	17	25	22	14	15	O	—	Comparator 1 Output
C2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Comparator 2 Input A (+)
C2INB	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 2 Input B (-)
C2INC	—	7	4	24	26	—	7	4	24	26	I	ANA	Comparator 2 Input C (+)
C2IND	—	6	3	23	25	—	6	3	23	25	I	ANA	Comparator 2 Input D (-)
C2OUT	—	20	17	7	7	—	16	13	43	47	O	—	Comparator 2 Output
C3INA	—	26	23	15	16	—	26	23	15	16	I	ANA	Comparator 3 Input A (+)
C3INB	—	25	22	14	15	—	25	22	14	15	I	ANA	Comparator 3 Input B (-)
C3INC	—	2	27	19	21	—	2	27	19	21	I	ANA	Comparator 3 Input C (+)
C3IND	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 3 Input D (-)
C3OUT	—	17	14	44	48	—	17	14	44	48	O	—	Comparator 3 Output
CLC1O	13	18	15	1	1	13	18	15	1	1	O	—	CLC 1 Output
CLC2O	—	19	16	6	6	—	19	16	6	6	O	—	CLC 2 Output
CLCINA	9	14	11	41	45	9	14	11	41	45	I	ST	CLC External Input A
CLCINB	10	15	12	42	46	10	15	12	42	46	I	ST	CLC External Input B
CLKI	7	9	6	30	33	7	9	6	30	33	I	ANA	Primary Clock Input
CLKO	8	10	7	31	34	8	10	7	31	34	O	—	System Clock Output
CN0	10	12	9	34	37	10	12	9	34	37	I	ST	Interrupt-on-Change Inputs
CN1	9	11	8	33	36	9	11	8	33	36	I	ST	Interrupt-on-Change Inputs
CN2	2	2	27	19	21	2	2	27	19	21	I	ST	Interrupt-on-Change Inputs
CN3	3	3	28	20	22	3	3	28	20	22	I	ST	Interrupt-on-Change Inputs
CN4	4	4	1	21	23	4	4	1	21	23	I	ST	Interrupt-on-Change Inputs
CN5	5	5	2	22	24	5	5	2	22	24	I	ST	Interrupt-on-Change Inputs
CN6	6	6	3	23	25	6	6	3	23	25	I	ST	Interrupt-on-Change Inputs
CN7	—	7	4	24	26	—	7	4	24	26	I	ST	Interrupt-on-Change Inputs
CN8	14	20	17	7	7	—	—	—	—	—	I	ST	Interrupt-on-Change Inputs
CN9	—	19	16	6	6	—	19	16	6	6	I	ST	Interrupt-on-Change Inputs
CN10	—	—	—	27	29	—	—	—	27	29	I	ST	Interrupt-on-Change Inputs
CN11	18	26	23	15	16	18	26	23	15	16	I	ST	Interrupt-on-Change Inputs
CN12	17	25	22	14	15	17	25	22	14	15	I	ST	Interrupt-on-Change Inputs

**Legend:** ANA = Analog level input/output, ST = Schmitt Trigger input buffer,  $I^2C^{TM} = I^2C/SMBus$  input buffer

**TABLE 4-31: CLOCK CONTROL REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	740h	TRAPR	IOPUWR	SBOREN	RETEN	—	—	CM	PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	(Note 1)
OSCCON	742h	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN	(Note 2)
CLKDIV	744h	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	—	—	—	—	—	—	—	—	0100
OSCTUN	748h	—	—	—	—	—	—	—	—	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000
REFOCON	74Eh	ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
HLVDCON	756h	HLVDEN	—	HLSIDL	—	—	—	—	—	VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** RCON register Reset values are dependent on the type of Reset.

**2:** OSCCON register Reset values are dependent on Configuration fuses and by type of Reset.

**TABLE 4-32: NVM REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	760h	WR	WREN	WRERR	PGONLY	—	—	—	—	—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMKEY	766h	—	—	—	—	—	—	—	—	NVMKEY7	NVMKEY6	NVMKEY5	NVMKEY4	NVMKEY3	NVMKEY2	NVMKEY1	NVMKEY0	0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**TABLE 4-33: ULTRA LOW-POWER WAKE-UP REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ULPWCON	768h	ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK	—	—	—	—	—	—	—	—	0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**TABLE 4-34: PMD REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	770h	—	—	—	—	T1MD	—	—	—	SSP1MD	U2MD <sup>(1)</sup>	U1MD	—	—	—	—	ADCMD	0000
PMD2	772h	—	—	—	—	—	—	—	—	—	—	—	CCP5MD <sup>(1)</sup>	CCP4MD <sup>(1)</sup>	CCP3MD <sup>(1)</sup>	CCP2MD	CCP1MD	0000
PMD3	774h	—	—	—	—	—	CMPMD	RTCCMD	—	—	DAC1MD <sup>(1)</sup>	—	—	—	—	SSP2MD <sup>(1)</sup>	—	0000
PMD4	776h	—	—	—	—	—	—	—	—	—	ULPWUMD	—	—	REFOMD	CTMUMD	HLVDM	—	0000
PMD6	77Ah	—	—	—	—	—	—	—	—	—	—	AMP1MD <sup>(1)</sup>	DAC2MD <sup>(1)</sup>	AMP2MD <sup>(1)</sup>	—	—	—	0000
PMD8	77Eh	—	—	—	—	—	—	—	—	—	—	—	—	CLC2MD <sup>(1)</sup>	CLC1MD	—	—	0000

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These bits are available only on PIC24F(V)16KM2XX devices.

# PIC24FV16KM204 FAMILY

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Flash programming, refer to the “PIC24F Family Reference Manual”, “Program Memory” (DS39715).

The PIC24FV16KM204 family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with VDD over 1.8V.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FXXXXX device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (which are named PGECx and PGEDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear/Program Mode Entry Voltage (MCLR/VPP). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or custom firmware to be programmed.

Run-Time Self-Programming (RTSP) is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 32 instructions (96 bytes) at a time, and erase program memory in blocks of 32, 64 and 128 instructions (96, 192 and 384 bytes) at a time.

The NVMOP<1:0> (NVMCON<1:0>) bits decide the erase block size.

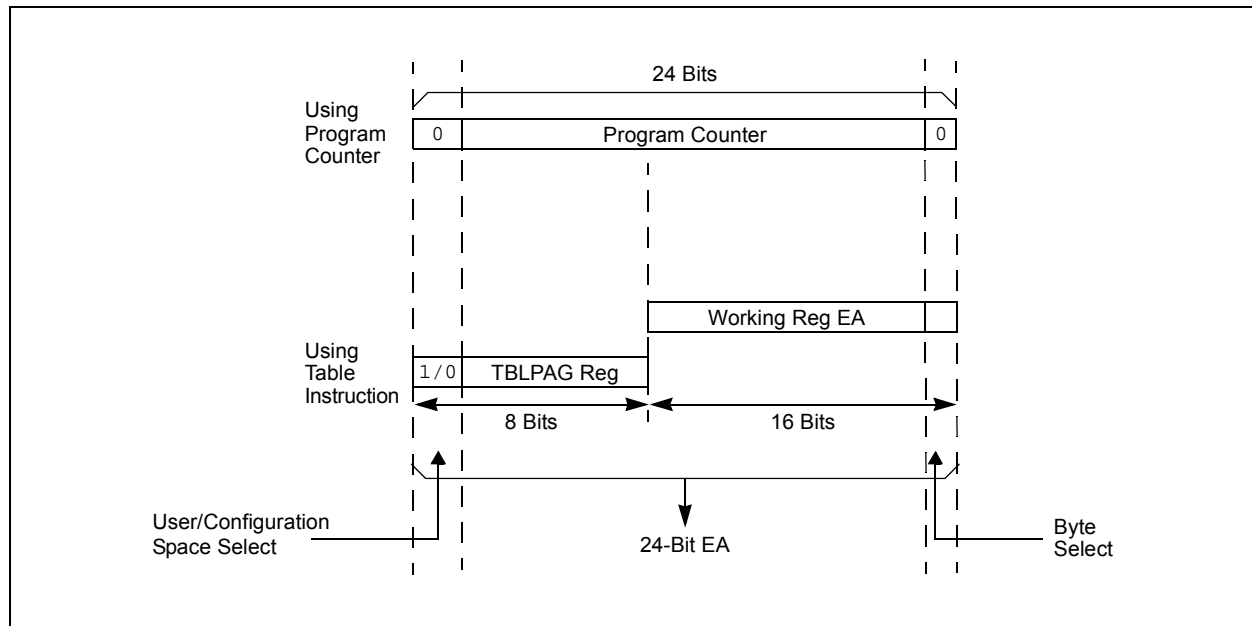
### 5.1 Table Instructions and Flash Programming

Regardless of the method used, Flash memory programming is done with the Table Read and Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as depicted in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



# PIC24FV16KM204 FAMILY

## REGISTER 8-21: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11-3 **Unimplemented:** Read as '0'

bit 2-0 **CCT2IP<2:0>:** Capture/Compare 2 Timer Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

## 10.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, “Power-Saving Features with VBAT” (DS30622).

This FRM describes some features which are not implemented in this device. Sections related to the VBAT pin and Deep Sleep do not apply to the PIC24FV16KM204 family.

The PIC24FV16KM204 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

### 10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 “Oscillator Configuration”**.

### 10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special `PWRSV` instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation.

The ‘C’ syntax of the `PWRSV` instruction is shown in Example 10-1.

**Note:** `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to “wake-up”.

#### 10.2.1 SLEEP MODE

Sleep mode includes these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The I/O pin directions and states are frozen.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT or RTCC with LPRC as the clock source is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

#### EXAMPLE 10-1: ‘C’ POWER-SAVING ENTRY

```
Sleep();           //Put the device into Sleep mode
Idle();            //Put the device into Idle mode
```



# PIC24FV16KM204 FAMILY

## 13.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 13-2.

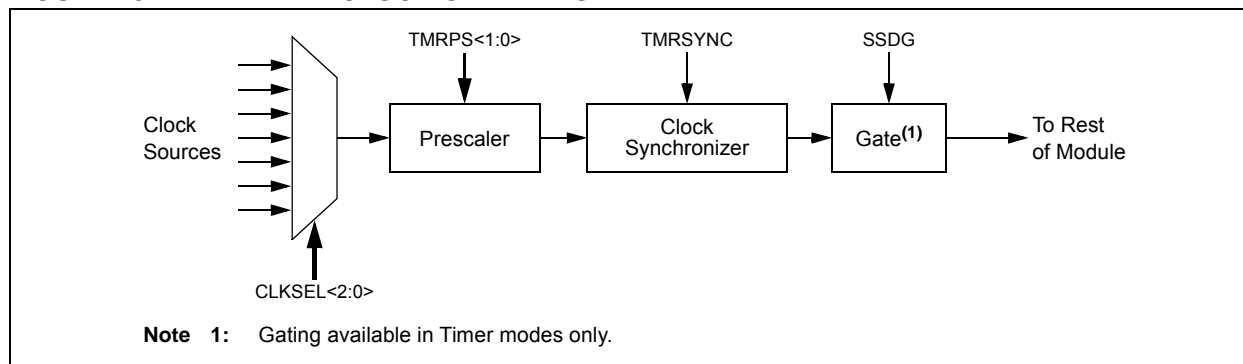
There are eight inputs available to the clock generator, which are selected using the CLKSEL<2:0> bits (CCPxCON1L<10:8>). Available sources include the FRC and LPRC, the Secondary Oscillator, and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL<2:0> = 000). On PIC24FV16KM204 family devices, clock sources to the MCCPx module must be synchronized with the system clock; as a result, when clock sources are selected, clock input timing restrictions or module operating restrictions may exist. Table 13-1 describes which time base sources are valid for the various operating modes.

**TABLE 13-1: VALID TIMER OPTIONS FOR MCCPx/SCCPx MODES**

CLKSEL<2:0> <sup>(1)</sup>	Timer		Input Capture	Output Compare
	Sync <sup>(2)</sup>	Async <sup>(3)</sup>		
111	X	—	—	—
110	X	—	—	—
101	X	—	—	—
011	X	—	—	—
010	X	—	—	—
001	X	—	—	—
000 <sup>(4)</sup>	—	X	X	X

- Note 1:** See Register 13-1 for the description of the time base sources.
- 2:** Synchronous Operation: TMRSYNC (CCPxCON1L<11>) = 1 and TRIGEN (CCPxCON1H<7>) = 0.
- 3:** Asynchronous Operation: (TMRSYNC = 0) or Triggered mode (TRIGEN = 1).
- 4:** When CLKSEL<2:0> = 000, the TMRSYNC bit must be cleared.

**FIGURE 13-2: TIMER CLOCK GENERATOR**



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# PIC24FV16KM204 FAMILY

## REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit		
HS = Hardware Settable bit	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
  - 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
  - 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
  - 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV:** IrDA® Encoder Transmit Polarity Inversion bit
- If IREN = 0:
- 1 = UxTX Idle '0'
  - 0 = UxTX Idle '1'
- If IREN = 1:
- 1 = UxTX Idle '1'
  - 0 = UxTX Idle '0'
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
  - 0 = Sync Break transmission is disabled or completed
- bit 10 **UTXEN:** UARTx Transmit Enable bit
- 1 = Transmit is enabled; UxTX pin is controlled by UARTx
  - 0 = Transmit is disabled; any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT register
- bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
  - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and the transmit buffer is empty (the last transmission has completed)
  - 0 = Transmit Shift Register is not empty; a transmission is in progress or queued
- bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on an RSR transfer, making the receive buffer full (i.e., has 4 data characters)
  - 10 = Interrupt is set on an RSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
  - 0x = Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

## 18.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

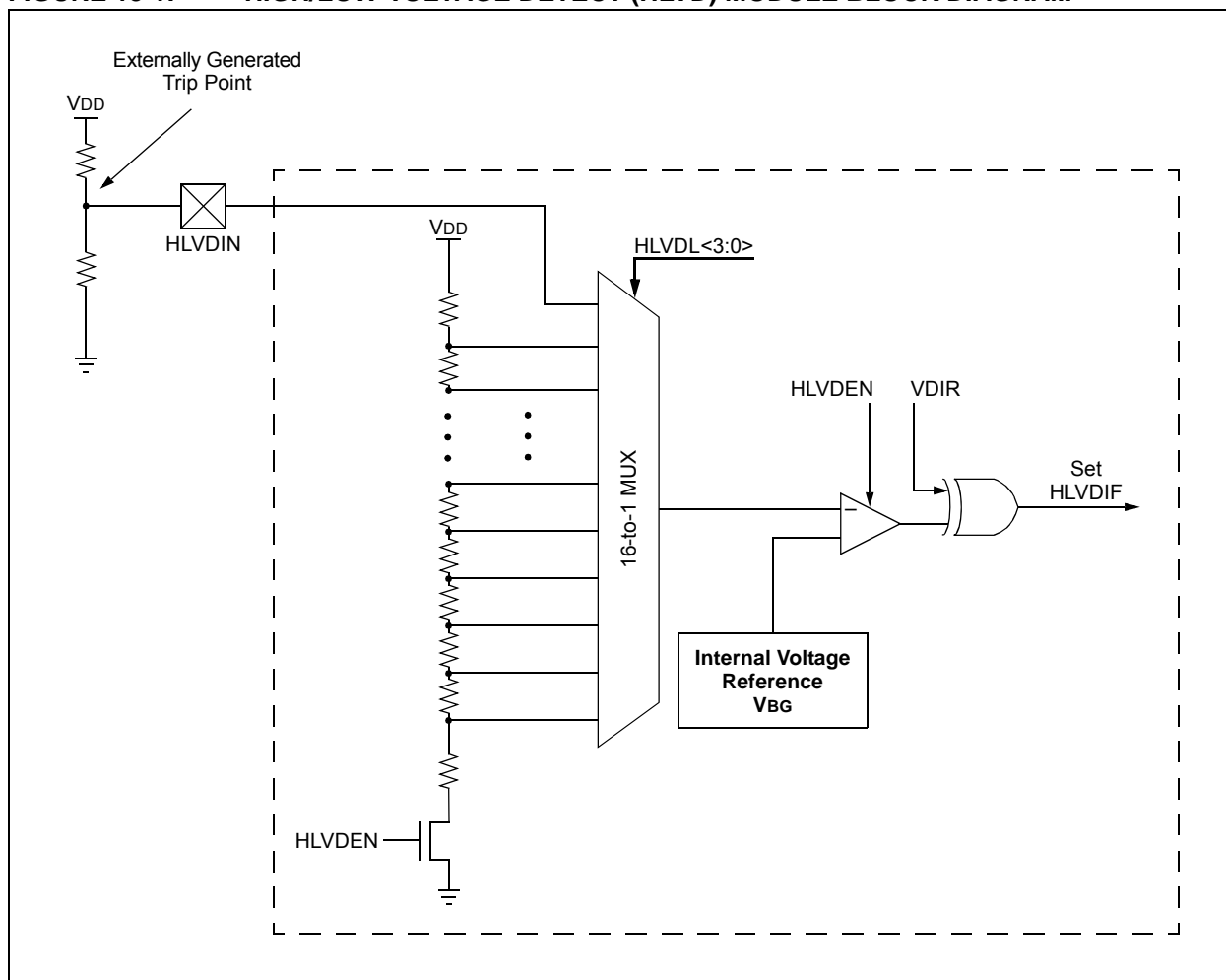
**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the “PIC24F Family Reference Manual”, “High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)” (DS39725).

The High/Low-Voltage Detect module (HLVD) is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 18-1) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

**FIGURE 18-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM**



# PIC24FV16KM204 FAMILY

## 21.0 DUAL OPERATIONAL AMPLIFIER MODULE

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “PIC24F Family Reference Manual”, “Operational Amplifier (Op Amp)” (DS30505). Device-specific information in this data sheet supersedes the information in the “PIC24F Family Reference Manual”.

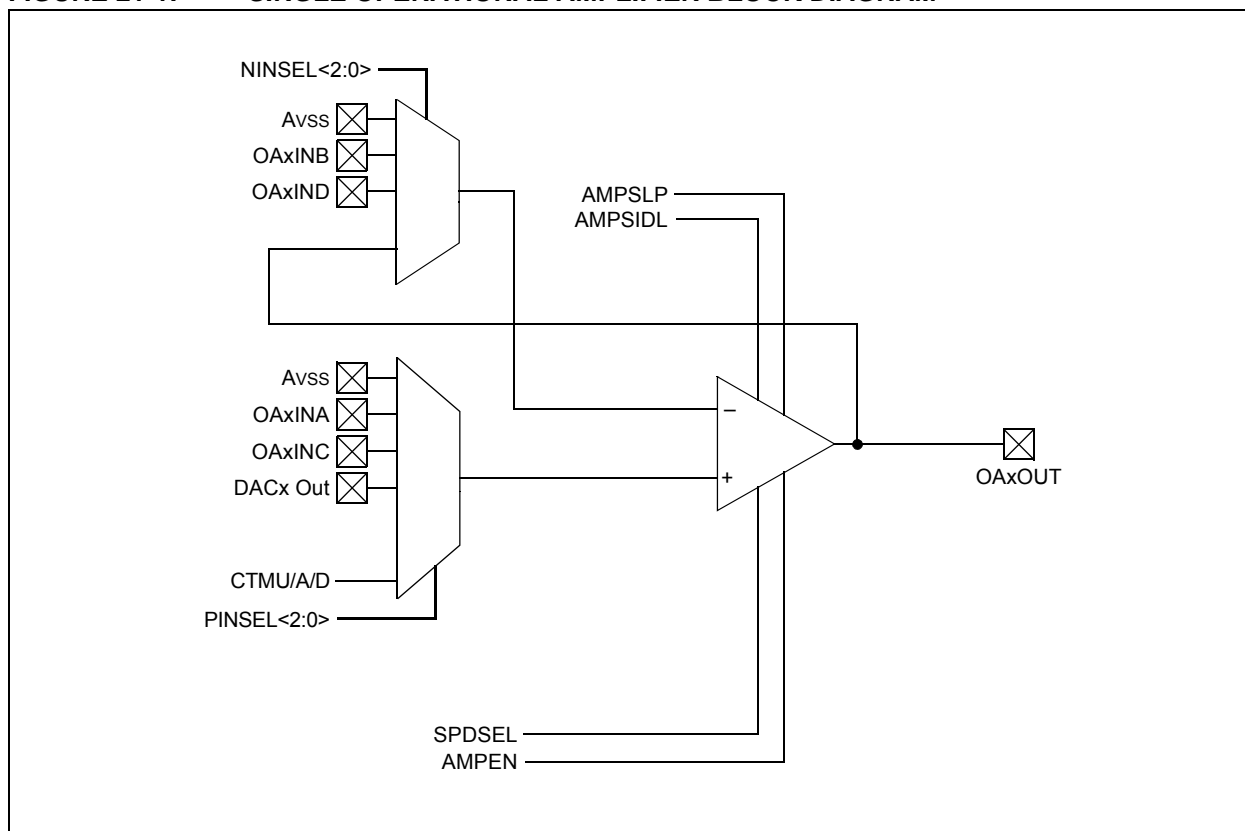
PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal unity-gain buffer option
- Multiple input options each on the inverting and non-inverting amplifier inputs
- Rail-to-rail input and output capabilities
- User-selectable option for regular or low-power operation
- User-selectable operation in Idle and Sleep modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 “Configuring Analog Port Pins”** for more information.

**FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM**



# PIC24FV16KM204 FAMILY

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC<sub>x</sub> bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled in hardware (FWDTEN<1:0> = 11), it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) will need to be cleared in software after the device wakes up.

The WDT Flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

## 25.3.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

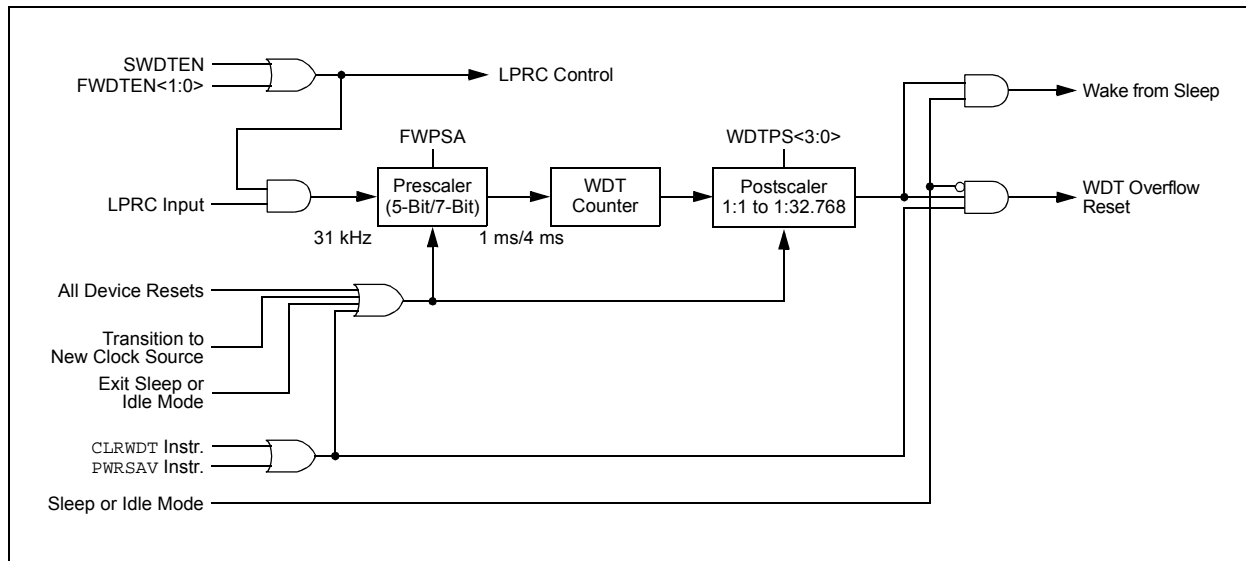
Windowed WDT mode is enabled by programming the Configuration bit, WINDIS (FWDT<6>), to '0'.

## 25.3.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN<1:0> Configuration bits. When both of the FWDTEN<1:0> Configuration bits are set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN<1:0> Configuration bits have been programmed to '10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments, and disable the WDT during non-critical segments, for maximum power savings. When the FWDTEN<1:0> bits are set to '01', the WDT is only enabled in Run and Idle modes, and is disabled in Sleep. Software control of the SWDTEN bit (RCON<5>) is disabled with this setting.

**FIGURE 25-2: WDT BLOCK DIAGRAM**



# PIC24FV16KM204 FAMILY

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## 26.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

## 26.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

# PIC24FV16KM204 FAMILY

**TABLE 27-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS**

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204)								
Operating temperature			-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000 <sup>(2)</sup>	—	—	1.90	V	
			HLVDL<3:0> = 0001	1.88	—	2.13	V	
			HLVDL<3:0> = 0010	2.09	—	2.35	V	
			HLVDL<3:0> = 0011	2.25	—	2.53	V	
			HLVDL<3:0> = 0100	2.35	—	2.62	V	
			HLVDL<3:0> = 0101	2.55	—	2.84	V	
			HLVDL<3:0> = 0110	2.80	—	3.10	V	
			HLVDL<3:0> = 0111	2.95	—	3.25	V	
			HLVDL<3:0> = 1000	3.09	—	3.41	V	
			HLVDL<3:0> = 1001	3.27	—	3.59	V	
			HLVDL<3:0> = 1010 <sup>(1)</sup>	3.46	—	3.79	V	
			HLVDL<3:0> = 1011 <sup>(1)</sup>	3.62	—	4.01	V	
			HLVDL<3:0> = 1100 <sup>(1)</sup>	3.91	—	4.26	V	
			HLVDL<3:0> = 1101 <sup>(1)</sup>	4.18	—	4.55	V	
			HLVDL<3:0> = 1110 <sup>(1)</sup>	4.49	—	4.87	V	

**Note 1:** These trip points should not be used on PIC24FXXKMXXX devices.

**Note 2:** This trip point should not be used on PIC24FVXXKMXXX devices.

**TABLE 27-5: BOR TRIP POINTS**

Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204)								
Operating temperature			-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC15		BOR Hysteresis		—	5	—	mV	
DC19		BOR Voltage on VDD Transition	BORV<1:0> = 00	—	—	—	—	Valid for LPBOR ( <b>Note 1</b> )
			BORV<1:0> = 01	2.90	3	3.38	V	
			BORV<1:0> = 10	2.53	2.7	3.07	V	
			BORV<1:0> = 11	1.75	1.85	2.05	V	( <b>Note 2</b> )
			BORV<1:0> = 11	1.95	2.05	2.16	V	( <b>Note 3</b> )

**Note 1:** LPBOR re-arms the POR circuit but does not cause a BOR.

**Note 2:** This is valid for PIC24F (3.3V) devices.

**Note 3:** This is valid for PIC24FV (5V) devices.



# PIC24FV16KM204 FAMILY

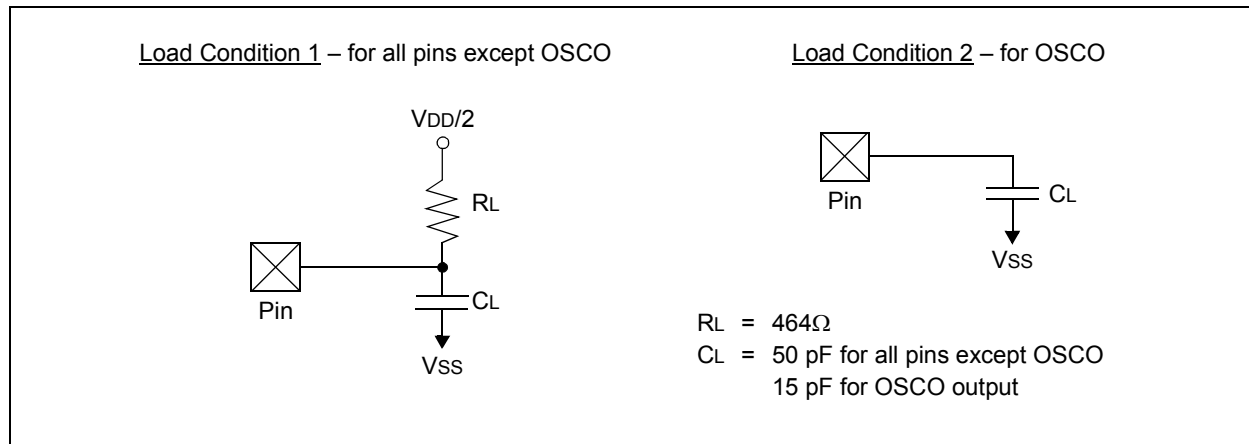
## 27.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FV16KM204 family AC characteristics and timing parameters.

**TABLE 27-18: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

<b>AC CHARACTERISTICS</b>	<b>Standard Operating Conditions: 1.8V to 3.6V</b>	
	Operating temperature	-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended
	Operating voltage VDD range as described in Section 27.1 “DC Characteristics”.	

**FIGURE 27-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**



**TABLE 27-19: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
DO50	Cosc2	OSCO/CLKO Pin	—	—	15	pF	In XT and HS modes when External Clock is used to drive OSCI
DO56	CIO	All I/O Pins and OSCO	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I <sup>2</sup> C™ mode

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

# PIC24FV16KM204 FAMILY

**TABLE 27-21: PLL CLOCK TIMING SPECIFICATIONS**

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range	4	—	8	MHz	ECPLL, HSPLL modes, -40°C ≤ TA ≤ +85°C
OS51	FSYS	PLL Output Frequency Range	16	—	32	MHz	-40°C ≤ TA ≤ +85°C
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	1	2	ms	
OS53	DCLK	CLKO Stability (Jitter)	-2	1	2	%	Measured over 100 ms period

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 27-22: INTERNAL RC OSCILLATOR ACCURACY**

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
F20	FRC @ 8 MHz <sup>(1)</sup>	-2	—	+2	%	+25°C	3.0V ≤ VDD ≤ 3.6V, F device 3.2V ≤ VDD ≤ 5.5V, FV device
		-5	—	+5	%	-40°C ≤ TA ≤ +125°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device
F21	LPRC @ 31 kHz <sup>(2)</sup>	-15	—	+15	%	-40°C ≤ TA ≤ +125°C	1.8V ≤ VDD ≤ 3.6V, F device 2.0V ≤ VDD ≤ 5.5V, FV device

**Note 1:** The frequency is calibrated at +25°C and 3.3V. The OSCTUN bits can be used to compensate for temperature drift.

**2:** The change of LPRC frequency as VDD changes.

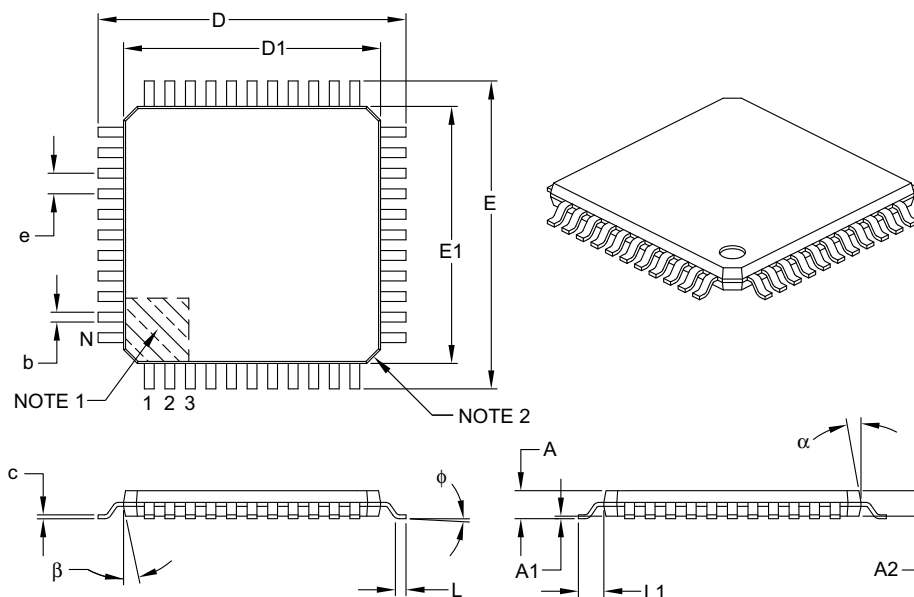
**TABLE 27-23: INTERNAL RC OSCILLATOR SPECIFICATIONS**

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
	TFRC	FRC Start-up Time	—	5	—	μs	
	TLPRC	LPRC Start-up Time	—	70	—	μs	

# PIC24FV16KM204 FAMILY

## 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	$\phi$	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	$\alpha$	11°	12°	13°
Mold Draft Angle Bottom	$\beta$	11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

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NOTES: