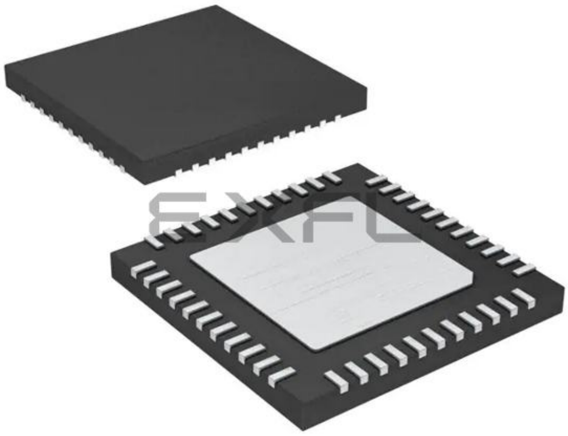

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Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f16km204t-i-ml

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TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CTED1	11	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	CTMU Trigger Edge Inputs
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	CTMU Trigger Edge Inputs
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	CTMU Trigger Edge Inputs
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	CTMU Trigger Edge Inputs
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	CTMU Trigger Edge Inputs
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	CTMU Trigger Edge Inputs
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	CTMU Trigger Edge Inputs
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	CTMU Trigger Edge Inputs
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	CTMU Trigger Edge Inputs
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	CTMU Trigger Edge Inputs
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	CTMU Trigger Edge Inputs
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	CTMU Trigger Edge Inputs
CTPLS	16	24	21	11	12	16	24	21	11	12	O	—	CTMU Pulse Output
CVREF	17	25	22	14	15	17	25	22	14	15	O	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Voltage Reference Positive Input
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Voltage Reference Negative Input
DAC1OUT	—	23	20	10	11	—	23	20	10	11	O	ANA	DAC1 Output
DAC1REF+	—	2	27	19	21	—	2	27	19	21	I	ANA	DAC1 Positive Voltage Reference Input
DAC2OUT	—	25	22	14	15	—	25	22	14	15	O	ANA	DAC2 Output
DAC2REF+	—	26	23	15	16	—	26	23	15	16	I	ANA	DAC2 Positive Voltage Reference Input
HLVDIN	15	23	20	10	11	15	23	20	10	11	I	ANA	External High/Low-Voltage Detect Input
IC1	14	19	16	6	6	11	19	16	6	6	I	ST	MCCP1 Input Capture Input
IC2	13	18	15	1	1	13	18	15	1	1	I	ST	MCCP2 Input Capture Input
IC3	—	23	20	13	14	—	23	20	13	14	I	ST	MCCP3 Input Capture Input
IC4	—	14	11	5	5	—	14	11	5	5	I	ST	SCCP4 Input Capture Input
IC5	—	15	12	12	13	—	15	12	12	13	I	ST	SCCP5 Input Capture Input
INT0	11	16	13	43	47	11	16	13	43	47	I	ST	External Interrupt 0 Input
INT1	17	25	22	14	15	17	25	22	14	15	I	ST	External Interrupt 1 Input
INT2	14	20	17	7	7	15	23	20	10	11	I	ST	External Interrupt 2 Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

TABLE 4-25: A/D REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	300h	A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF1	302h	A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF2	304h	A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF3	306h	A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF4	308h	A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF5	30Ah	A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF6	30Ch	A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF7	30Eh	A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF8	310h	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF9	312h	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF10	314h	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF11	316h	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare																xxxx
ADC1BUF12	318h	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF13	31Ah	A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF14	31Ch	A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF15	31Eh	A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF16	320h	A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF17	322h	A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF18	324h	A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF19	326h	A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF20	328h	A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF21	32Ah	A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF22	32Ch	A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF23	32Eh	A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare																xxxx
AD1CON1	340h	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	342h	PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	344h	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	348h	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	34Eh	—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—	CSS23	CSS22	CSS21	CSS20[1]	CSS19[1]	CSS18	CSS17	CSS16	0000
AD1CSSL	350h	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8[1,2]	CSS7[1,2]	CSS6[1,2]	CSS5[1]	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON5	354h	ASEN	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	356h	—	—	—	—	—	—	—	—	CHH23	CHH22	CHH21	CHH20[1]	CHH19[1]	CHH18	CHH17	CHH16	0000
AD1CHITL	358h	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8[1,2]	CHH7[1,2]	CHH6[1,2]	CHH5[1]	CHH4	CHH3	CHH2	CHH1	CHH0	0000
AD1CTMENH	360h	—	—	—	—	—	—	—	—	CTMEN23	CTMEN22	CTMEN21	CTMEN20[1]	CTMEN19[1]	CTMEN18	CTMEN17	CTMEN16	0000
AD1CTMENL	362h	CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8[(1,2]	CTMEN7[1,2]	CTMEN6[1,2]	CTMEN5[1]	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

4.2.5 SOFTWARE STACK

In addition to its use as a working register, the W15 register in PIC24F devices is also used as a Software Stack Pointer. The pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as depicted in Figure 4-4.

For a PC push during any `CALL` instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

> **Note:** A PC push during exception processing will concatenate the SRL register to the MSB of the PC prior to the push.

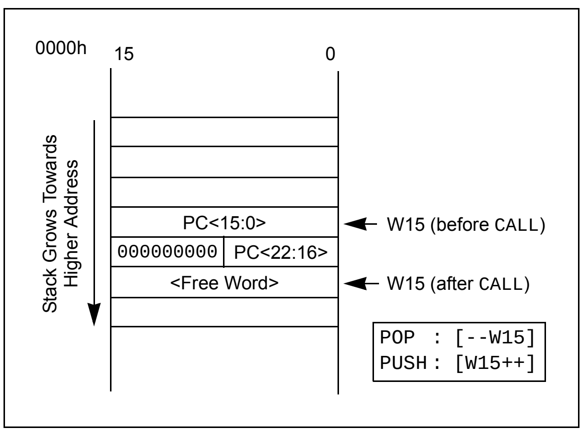
The Stack Pointer Limit Value (SPLIM) register, associated with the Stack Pointer, sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '`0`' as all stack operations must be word-aligned. Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation.

Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address, 0DF6 in RAM, initialize the SPLIM with the value, 0DF4.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0800h. This prevents the stack from interfering with the Special Function Register (SFR) space.

> **Note:** A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-4: CALL STACK FRAME



4.3 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit-wide program space and 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Apart from the normal execution, the PIC24F architecture provides two methods by which the program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space, PSV

Table instructions allow an application to read or write small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look ups from a large table of static data. It can only access the least significant word (lsw) of the program word.

4.3.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the Most Significant bit (MSb) of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = `0`) or the configuration memory (TBLPAG<7> = `1`).

For remapping operations, the 8-bit Program Space Visibility Page Address register (PSVPAG) is used to define a 16K word page in the program space. When the MSb of the EA is '`1`', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike the table operations, this limits remapping operations strictly to the user memory area.

See Table 4-35 and Figure 4-5 to know how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a Data Space word.

REGISTER 6-1: NVMCON: NONVOLATILE MEMORY CONTROL REGISTER

R/SO-0, HC	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	PGMONLY	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	S = Settable Only bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit (program or erase)
1 = Initiates a data EEPROM erase or write cycle (can be set, but not cleared in software)
0 = Write cycle is complete (cleared automatically by hardware)

bit 14 **WREN:** Write Enable bit (erase or program)
1 = Enables an erase or program operation
0 = No operation allowed (device clears this bit on completion of the write/erase operation)

bit 13 **WRERR:** Flash Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ or WDT Reset during programming operation)
0 = The write operation completed successfully

bit 12 **PGMONLY:** Program Only Enable bit
1 = Write operation is executed without erasing target address(es) first
0 = Automatic erase-before-write
Write operations are preceded automatically by an erase of the target address(es).

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6 **ERASE:** Erase Operation Select bit
1 = Performs an erase operation when WR is set
0 = Performs a write operation when WR is set

bit 5-0 **NVMOP<5:0>:** Programming Operation Command Byte bits
Erase Operations (when ERASE bit is ‘1’):
011010 = Erase 8 words
011001 = Erase 4 words
011000 = Erase 1 word
0100xx = Erase entire data EEPROM
Programming Operations (when ERASE bit is ‘0’):
0001xx = Write 1 word

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0, HSC	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	**ALTIVT:** Enable Alternate Interrupt Vector Table bit 1 = Uses Alternate Interrupt Vector Table (AIVT) 0 = Uses standard (default) Interrupt Vector Table (IVT)
bit 14	**DISI:** DISI Instruction Status bit 1 = DISI instruction is active 0 = DISI instruction is not active
bit 13-3	**Unimplemented:** Read as '0'
bit 2	**INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit 1 = Interrupt is on the negative edge 0 = Interrupt is on the positive edge
bit 1	**INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit 1 = Interrupt is on the negative edge 0 = Interrupt is on the positive edge
bit 0	**INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit 1 = Interrupt is on the negative edge 0 = Interrupt is on the positive edge

REGISTER 8-30: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

8.4 Interrupt Setup Procedures

8.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS control bit (INTCON1<15>) if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

Note:	At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to Priority Level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

8.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an ISR (Interrupt Service Routine) and initialize the IVT with the correct vector address depends on the programming language (i.e., C or assembly), and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

8.4.3 TRAP SERVICE ROUTINE (TSR)

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

8.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to Priority Level 7 by inclusive ORing the value, 0Eh, with SRL.

To enable user interrupts, the `POP` instruction may be used to restore the previous SR value.

Only user interrupts with a priority level of 7 or less can be disabled. Trap sources (Levels 8-15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of Priority Levels 1-6 for a fixed period. Level 7 interrupt sources are not disabled by the `DISI` instruction.

10.0 POWER-SAVING FEATURES

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **"Power-Saving Features with VBAT"** (DS30622).
>
> This FRM describes some features which are not implemented in this device. Sections related to the VBAT pin and Deep Sleep do not apply to the PIC24FV16KM204 family.

The PIC24FV16KM204 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation.

The 'C' syntax of the PWRSAV instruction is shown in Example 10-1.

> **Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.2.1 SLEEP MODE

Sleep mode includes these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The I/O pin directions and states are frozen.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT or RTCC with LPRC as the clock source is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification on the I/O ports or peripherals that use an External Clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: 'C' POWER-SAVING ENTRY

```
Sleep();              //Put the device into Sleep mode
Idle();               //Put the device into Idle mode
```

REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	**ADDEN:** Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	**RIDLE:** Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	**PERR:** Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	**FERR:** Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	**OERR:** Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the empty state)
bit 0	**URXDA:** UARTx Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data; at least one more characters can be read 0 = Receive buffer is empty

16.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 16-4: YEAR: YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year’s Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 16-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 17-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

111 = MCCP2 Compare Event Flag (CCP2IF)
110 = MCCP1 Compare Event Flag (CCP1IF)
101 = Digital logic low
100 = A/D end of conversion event

For CLC1:
011 = UART1 TX
010 = Comparator 1 output
001 = CLC2 output
000 = CLCINB I/O pin

For CLC2:
011 = UART2 TX
010 = Comparator 1 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

111 = SCCP5 Compare Event Flag (CCP5IF)
110 = SCCP4 Compare Event Flag (CCP4IF)
101 = Digital logic low
100 = 8 MHz FRC clock source
011 = LPRC clock source
010 = SOSC clock source
001 = System clock (T_{CY})
000 = CLCINA I/O pin

REGISTER 19-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	EXTSAM	r	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit
1 = RC clock
0 = Clock is derived from the system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **Reserved:** Maintain as ‘0’

bit 12-8 **SAMC<4:0>:** Auto-Sample Time Select bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Select bits
11111111-01000000 = Reserved
00111111 = 64 * TCY = TAD
•
•
•
00000001 = 2 * TCY = TAD
00000000 = TCY = TAD

REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER (CONTINUED)

bit 7-5	**CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits The same definitions as for CHONB<2:0>.
bit 4-0	**CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits The same definitions as for CHONA<4:0>.

Note 1: This is implemented on 44-pin devices only.
2: This is implemented on 28-pin and 44-pin devices only.
3: The band gap value used for this input is 2x or 4x the internal V_{BG}, which is selected when PVCFG<1:0> = `1x`.

REGISTER 19-6: AD1CHITH: A/D SCAN COMPARE HIT REGISTER (HIGH WORD)[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH23	CHH22	CHH21	CHH20[2]	CHH19[2]	CHH18	CHH17	CHH16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8	**Unimplemented:** Read as ‘`0`’.
bit 7-0	**CHH<23:16>:** A/D Compare Hit bits[2] <u>If CM<1:0> = `11`:</u> `1` = A/D Result Buffer x has been written with data or a match has occurred `0` = A/D Result Buffer x has not been written with data <u>For All Other Values of CM<1:0>:</u> `1` = A match has occurred on A/D Result Channel x `0` = No match has occurred on A/D Result Channel x

Note 1: Unimplemented channels are read as ‘`0`’.
2: The CHH<20:19> bits are not implemented in 20-pin devices.

NOTES:

REGISTER 25-6: FPOR: RESET CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE[2]	BORV1[3]	BORV0[3]	I2C1SEL[1]	PWRTEN	RETCFG[1]	BOREN1	BOREN0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit[2]
`1` = $\overline{\text{MCLR}}$ pin is enabled; RA5 input pin is disabled
`0` = RA5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-5 **BORV<1:0>:** Brown-out Reset Enable bits[3]
`11` = Brown-out Reset is set to the lowest voltage
`10` = Brown-out Reset is set to the middle voltage
`01` = Brown-out Reset is set to the highest voltage
`00` = Downside protection on POR is enabled – Low-Power BOR (LPBOR) is selected

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit[1]
`1` = Default location for SCL1/SDA1 pins
`0` = Alternate location for SCL1/SDA1 pins

bit 3 **PWRTEN:** Power-up Timer Enable bit
`1` = PWRT is enabled
`0` = PWRT is disabled

bit 2 **RETCFG:** Retention Regulator Configuration bit[1]
`1` = Low-voltage regulator is not available
`0` = Low-voltage regulator is available and controlled by the RETEN bit (RCON<12>) during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
`11` = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
`10` = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
`01` = Brown-out Reset is controlled with the SBOREN bit setting
`00` = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

Note 1: This setting only applies to the “FV” devices. This bit is reserved and should be maintained as ‘`1`’ on “F” devices.

2: The MCLRE fuse can only be changed when using the V_{PP}-based ICSP™ mode entry. This prevents a user from accidentally locking out the device from the low-voltage test entry.

3: Refer to **Section 27.0 “Electrical Characteristics”** for BOR voltages.

26.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

26.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

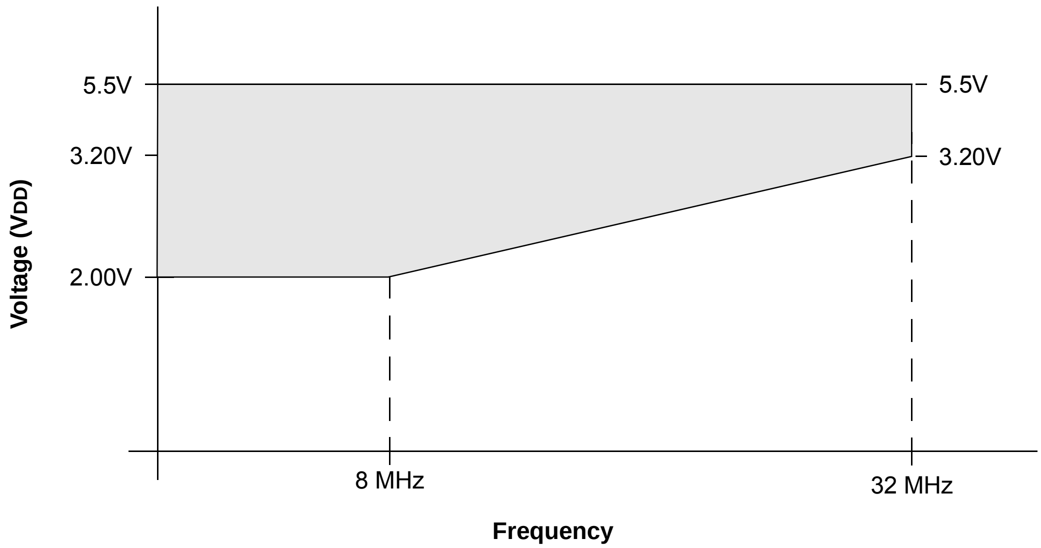
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

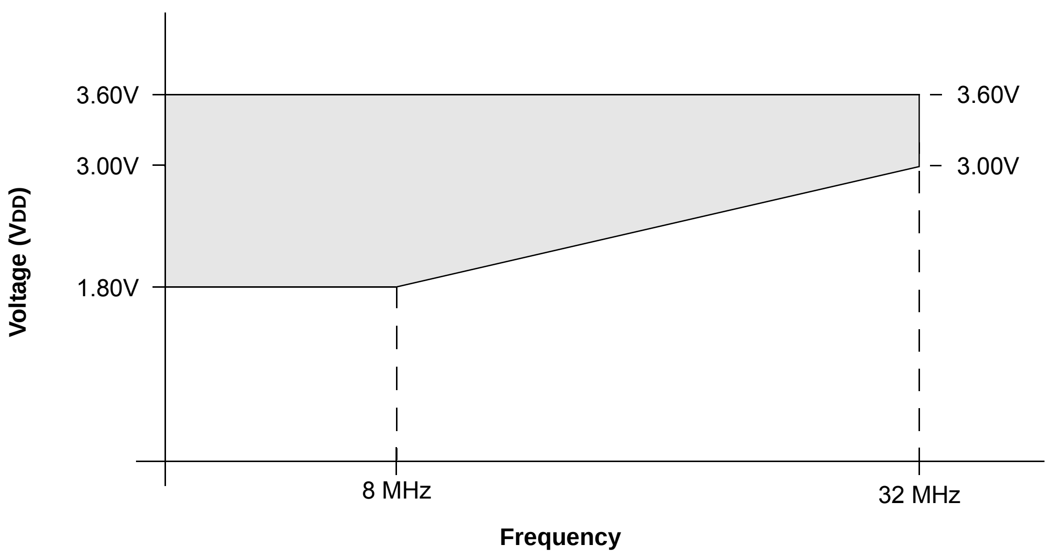
27.1 DC Characteristics

FIGURE 27-1: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, F_{MAX} = 20 MHz * (V_{DD} – 2.0) + 8 MHz.

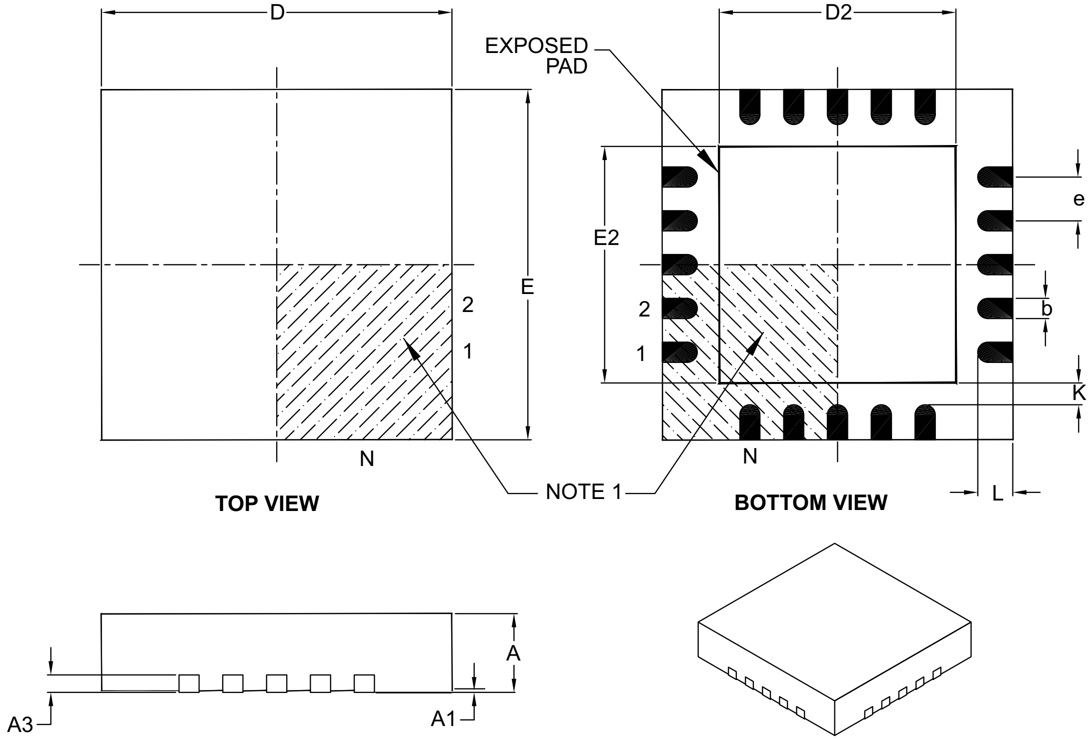
FIGURE 27-2: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, F_{MAX} = 20 MHz * (V_{DD} – 1.8) + 8 MHz.

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

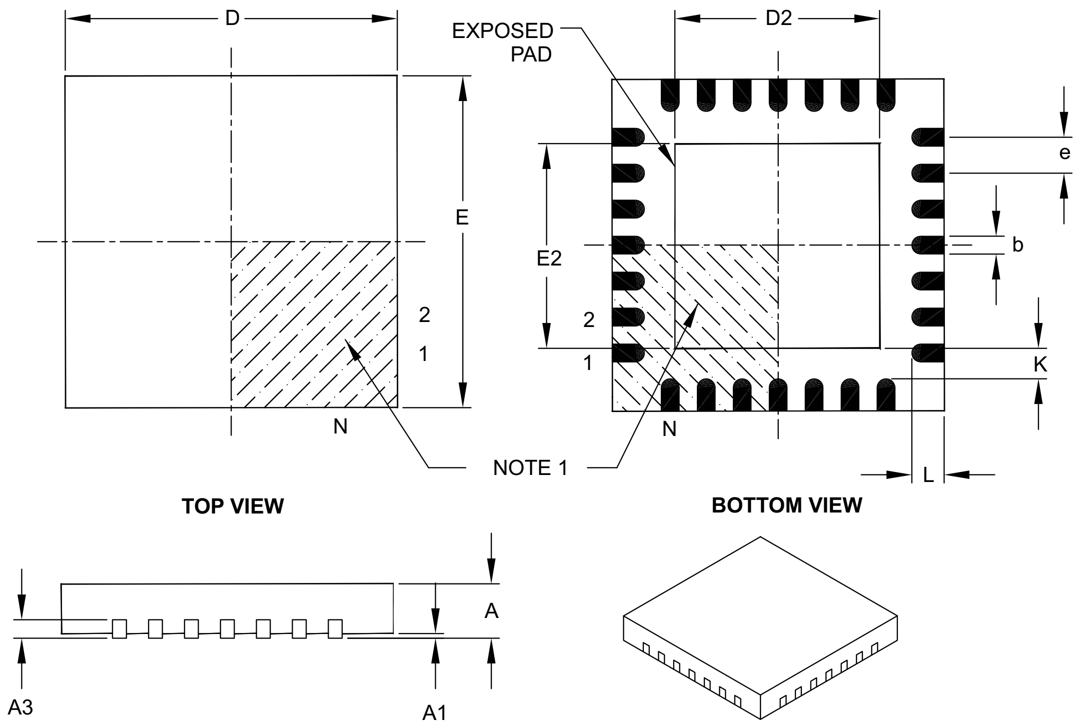
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B