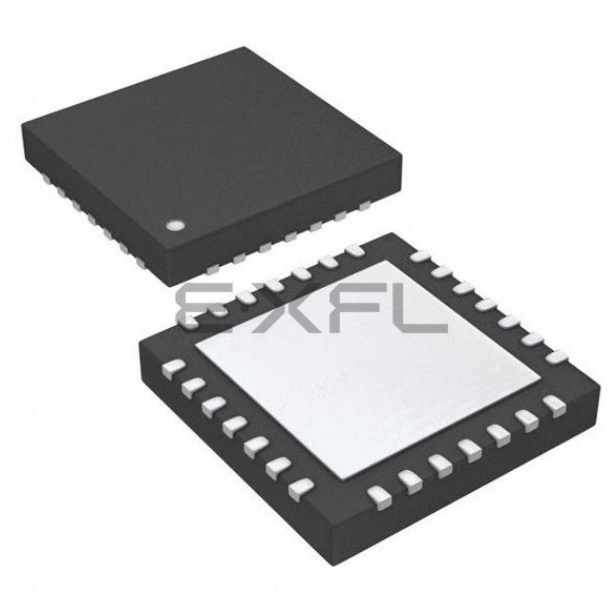
# Microchip Technology - PIC24FV08KM102-E/ML Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 8KB (2.75K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5V |
| Data Converters | A/D 19x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km102-e-ml |

**TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Function | F | | | | | FV | | | | | I/O | Buffer | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin Number | | | | | Pin Number | | | | | | | |
| | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | 20-Pin PDIP/ SSOP/ SOIC | 28-Pin PDIP/ SSOP/ SOIC | 28-Pin QFN | 44-Pin QFN/ TQFP | 48-Pin UQFN | | | |
| OSCI | 7 | 9 | 6 | 30 | 33 | 7 | 9 | 6 | 30 | 33 | I | ANA | Primary Oscillator Input |
| OSCO | 8 | 10 | 7 | 31 | 34 | 8 | 10 | 7 | 31 | 34 | O | ANA | Primary Oscillator Output |
| PGEC1 | 5 | 5 | 2 | 22 | 24 | 5 | 5 | 2 | 22 | 24 | I/O | ST | ICSP Clock 1 |
| PGED1 | 4 | 4 | 1 | 21 | 23 | 4 | 4 | 1 | 21 | 23 | I/O | ST | ICSP Data 1 |
| PGEC2 | 2 | 22 | 19 | 9 | 10 | 2 | 22 | 19 | 9 | 10 | I/O | ST | ICSP Clock 2 |
| PGED2 | 3 | 21 | 18 | 8 | 9 | 3 | 21 | 18 | 8 | 9 | I/O | ST | ICSP Data 2 |
| PGEC3 | 10 | 15 | 12 | 42 | 46 | 10 | 15 | 12 | 42 | 46 | I/O | ST | ICSP Clock 3 |
| PGED3 | 9 | 14 | 11 | 41 | 45 | 9 | 14 | 11 | 41 | 45 | I/O | ST | ICSP Data 3 |
| PWRLCLK | 10 | 12 | 9 | 34 | 37 | 10 | 12 | 9 | 34 | 37 | I | ST | RTCC Power Line Clock Input |
| RA0 | 2 | 2 | 27 | 19 | 21 | 2 | 2 | 27 | 19 | 21 | I/O | ST | PORTA Pins |
| RA1 | 3 | 3 | 28 | 20 | 22 | 3 | 3 | 28 | 20 | 22 | I/O | ST | PORTA Pins |
| RA2 | 7 | 9 | 6 | 30 | 33 | 7 | 9 | 6 | 30 | 33 | I/O | ST | PORTA Pins |
| RA3 | 8 | 10 | 7 | 31 | 34 | 8 | 10 | 7 | 31 | 34 | I/O | ST | PORTA Pins |
| RA4 | 10 | 12 | 9 | 34 | 37 | 10 | 12 | 9 | 34 | 37 | I/O | ST | PORTA Pins |
| RA5 | 1 | 1 | 26 | 18 | 19 | 1 | 1 | 26 | 18 | 19 | I/O | ST | PORTA Pins |
| RA6 | 14 | 20 | 17 | 7 | 7 | — | — | — | — | — | I/O | ST | PORTA Pins |
| RA7 | — | 19 | 16 | 6 | 6 | — | 19 | 16 | 6 | 6 | I/O | ST | PORTA Pins |
| RA8 | — | — | — | 32 | 35 | — | — | — | 32 | 35 | I/O | ST | PORTA Pins |
| RA9 | — | — | — | 35 | 38 | — | — | — | 35 | 38 | I/O | ST | PORTA Pins |
| RA10 | — | — | — | 12 | 13 | — | — | — | 12 | 13 | I/O | ST | PORTA Pins |
| RA11 | — | — | — | 13 | 14 | — | — | — | 13 | 14 | I/O | ST | PORTA Pins |
| RB0 | 4 | 4 | 1 | 21 | 23 | 4 | 4 | 1 | 21 | 23 | I/O | ST | PORTB Pins |
| RB1 | 5 | 5 | 2 | 22 | 24 | 5 | 5 | 2 | 22 | 24 | I/O | ST | PORTB Pins |
| RB2 | 6 | 6 | 3 | 23 | 25 | 6 | 6 | 3 | 23 | 25 | I/O | ST | PORTB Pins |
| RB3 | — | 7 | 4 | 24 | 26 | — | 7 | 4 | 24 | 26 | I/O | ST | PORTB Pins |
| RB4 | 9 | 11 | 8 | 33 | 36 | 9 | 11 | 8 | 33 | 36 | I/O | ST | PORTB Pins |
| RB5 | — | 14 | 11 | 41 | 45 | — | 14 | 11 | 41 | 45 | I/O | ST | PORTB Pins |
| RB6 | — | 15 | 12 | 42 | 46 | — | 15 | 12 | 42 | 46 | I/O | ST | PORTB Pins |
| RB7 | 11 | 16 | 13 | 43 | 47 | 11 | 16 | 13 | 43 | 47 | I/O | ST | PORTB Pins |
| RB8 | 12 | 17 | 14 | 44 | 48 | 12 | 17 | 14 | 44 | 48 | I/O | ST | PORTB Pins |

**Legend:** ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C$™ = $I^2C$/SMBus input buffer

**TABLE 4-21: PORTA REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11(4,5) | Bit 10(4,5) | Bit 9(4,5) | Bit 8(4,5) | Bit 7(4) | Bit 6(3) | Bit 5(2) | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 2C0h | — | — | — | — | TRISA11 | TRISA10 | TRISA9 | TRISA8 | TRISA7 | TRISA6 | — | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 0FDF(1) |
| PORTA | 2C2h | — | — | — | — | RA11 | RA10 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| LATA | 2C4h | — | — | — | — | LATA11 | LATA10 | LATA9 | LATA8 | LATA7 | LATA6 | — | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| ODCA | 2C6h | — | — | — | — | ODA11 | ODA10 | ODA9 | ODA8 | ODA7 | ODA6 | — | ODA4 | ODA3 | ODA2 | ODA1 | ODA0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** Reset value depends on the device type; the PIC24F16KM204 value is shown.
**2:** These bits are only available when MCLRE (FPOR<7>) = 0.
**3:** These bits are not implemented in FV devices.
**4:** These bits are not implemented in 20-pin devices.
**5:** These bits are not implemented in 28-pin devices.

**TABLE 4-22: PORTB REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11(2) | Bit 10(2) | Bit 9 | Bit 8 | Bit 7 | Bit 6(2) | Bit 5(2) | Bit 4 | Bit 3(2) | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 2C8h | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF(1) |
| PORTB | 2CAh | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| LATB | 2CCh | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| ODCB | 2CEh | ODB15 | ODB14 | ODB13 | ODB12 | ODB11 | ODB10 | ODB9 | ODB8 | ODB7 | ODB6 | ODB5 | ODB4 | ODB3 | ODB2 | ODB1 | ODB0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** Reset value depends on the device type; the PIC24F16KM204 value is shown.
**2:** These bits are not implemented in 20-pin devices.

**TABLE 4-23: PORTC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9(2,3) | Bit 8(2,3) | Bit 7(2,3) | Bit 6(2,3) | Bit 5(2,3) | Bit 4(2,3) | Bit 3(2,3) | Bit 2(2,3) | Bit 1(2,3) | Bit 0(2,3) | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 2D0h | — | — | — | — | — | — | TRISC9 | TRISC8 | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 03FF(1) |
| PORTC | 2D2h | — | — | — | — | — | — | RC9 | RC8 | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx |
| LATTC | 2D4h | — | — | — | — | — | — | LATC9 | LATC8 | LATC7 | LATC6 | LATC5 | LATC4 | LATC3 | LATC2 | LATC1 | LATC0 | xxxx |
| ODCC | 2D6h | — | — | — | — | — | — | ODC9 | ODC8 | ODC7 | ODC6 | ODC5 | ODC4 | ODC3 | ODC2 | ODC1 | ODC0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** Reset value depends on the device type; the PIC24F16KM204 value is shown.
**2:** These bits are not implemented in 20-pin devices.
**3:** These bits are not implemented in 28-pin devices.

**TABLE 4-31: CLOCK CONTROL REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | 740h | TRAPR | IOPUWR | SBOREN | RETEN | — | — | CM | PMSLP | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | (Note 1) |
| OSCCON | 742h | — | COSC2 | COSC1 | COSC0 | — | NOSC2 | NOSC1 | NOSC0 | CLKLOCK | — | LOCK | — | CF | SOSCDRV | SOSCEN | OSWEN | (Note 2) |
| CLKDIV | 744h | ROI | DOZE2 | DOZE1 | DOZE0 | DOZEN | RCDIV2 | RCDIV1 | RCDIV0 | — | — | — | — | — | — | — | — | 0100 |
| OSCTUN | 748h | — | — | — | — | — | — | — | — | — | — | TUN5 | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 | 0000 |
| REFOCON | 74Eh | ROEN | — | ROSSLP | ROSEL | RODIV3 | RODIV2 | RODIV1 | RODIV0 | — | — | — | — | — | — | — | — | 0000 |
| HLVDCON | 756h | HLVDEN | — | HLSIDL | — | — | — | — | — | VDIR | BGVST | IRVST | — | HLVDL3 | HLVDL2 | HLVDL1 | HLVDL0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** RCON register Reset values are dependent on the type of Reset.
**2:** OSCCON register Reset values are dependent on Configuration fuses and by type of Reset.

**TABLE 4-32: NVM REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NVMCON | 760h | WR | WREN | WRERR | PGMONLY | — | — | — | — | — | ERASE | NVMOP5 | NVMOP4 | NVMOP3 | NVMOP2 | NVMOP1 | NVMOP0 | 0000 |
| NVMKEY | 766h | — | — | — | — | — | — | — | — | NVMKEY7 | NVMKEY6 | NVMKEY5 | NVMKEY4 | NVMKEY3 | NVMKEY2 | NVMKEY1 | NVMKEY0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**TABLE 4-33: ULTRA LOW-POWER WAKE-UP REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ULPWCON | 768h | ULPEN | — | ULPSIDL | — | — | — | — | ULPSINK | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**TABLE 4-34: PMD REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 770h | — | — | — | — | T1MD | — | — | — | SSP1MD | U2MD(1) | U1MD | — | — | — | — | ADCMD | 0000 |
| PMD2 | 772h | — | — | — | — | — | — | — | — | — | — | — | CCP5MD(1) | CCP4MD(1) | CCP3MD(1) | CCP2MD | CCP1MD | 0000 |
| PMD3 | 774h | — | — | — | — | — | CMPMD | RTCCMD | — | — | DAC1MD(1) | — | — | — | — | SSP2MD(1) | — | 0000 |
| PMD4 | 776h | — | — | — | — | — | — | — | — | — | ULPWUMD | — | — | REFOMD | CTMUMD | HLVDMD | — | 0000 |
| PMD6 | 77Ah | — | — | — | — | — | — | — | — | — | — | AMP1MD(1) | DAC2MD(1) | AMP2MD(1) | — | — | — | 0000 |
| PMD8 | 77Eh | — | — | — | — | — | — | — | — | — | — | — | — | CLC2MD(1) | CLC1MD | — | — | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** These bits are available only on PIC24F(V)16KM2XX devices.

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on Flash programming, refer to the *"PIC24F Family Reference Manual"*, **"Program Memory"** (DS39715).

The PIC24FV16KM204 family of devices contains internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable when operating with VDD over 1.8V.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FXXXXX device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (which are named PGECx and PGEDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear/Program Mode Entry Voltage (MCLR/VPP). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or custom firmware to be programmed.

Run-Time Self-Programming (RTSP) is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 32 instructions (96 bytes) at a time, and erase program memory in blocks of 32, 64 and 128 instructions (96,192 and 384 bytes) at a time.

The NVMOP<1:0> (NVMCON<1:0>) bits decide the erase block size.

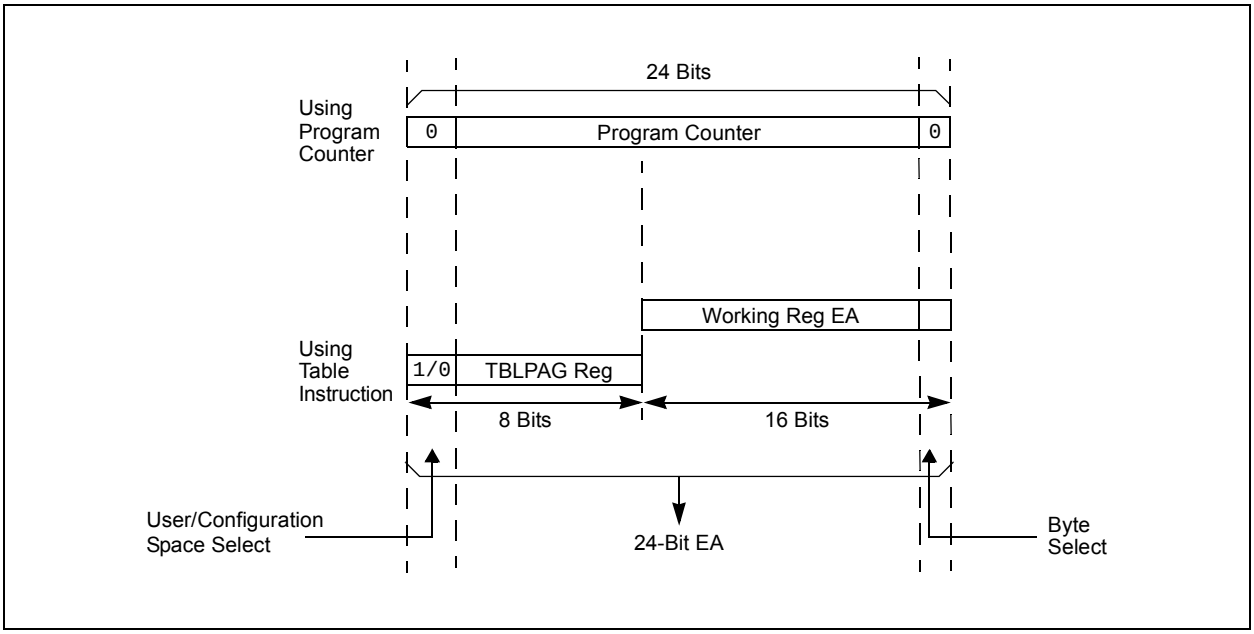
### 5.1 Table Instructions and Flash Programming

Regardless of the method used, Flash memory programming is done with the Table Read and Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as depicted in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

**FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS**



## 7.1 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 7-2. If clock switching is disabled, the system clock source is always selected according to the Oscillator Configuration bits. For more information, see **Section 9.0 "Oscillator Configuration"**.

**TABLE 7-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)**

| Reset Type | Clock Source Determinant |
|---|---|
| POR | FNOSC<2:0> Configuration bits (FOSCSEL<2:0>) |
| BOR | |
| $\overline{\text{MCLR}}$ | COSC<2:0> Control bits (OSCCON<14:12>) |
| WDTO | |
| SWR | |

## 7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-3. Note that the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR and PWRT delay times expire.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

**TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS**

| Reset Type | Clock Source | $\overline{\text{SYSRST}}$ Delay | System Clock Delay | Notes |
|---|---|---|---|---|
| POR(6) | EC | TPOR + TPWRT | — | 1, 2 |
| | FRC, FRCDIV | TPOR + TPWRT | TFRC | 1, 2, 3 |
| | LPRC | TPOR + TPWRT | TLPRC | 1, 2, 3 |
| | ECPLL | TPOR + TPWRT | TLOCK | 1, 2, 4 |
| | FRCPLL | TPOR + TPWRT | TFRC + TLOCK | 1, 2, 3, 4 |
| | XT, HS, SOSC | TPOR+ TPWRT | TOST | 1, 2, 5 |
| | XTPLL, HSPLL | TPOR + TPWRT | TOST + TLOCK | 1, 2, 4, 5 |
| BOR | EC | TPWRT | — | 2 |
| | FRC, FRCDIV | TPWRT | TFRC | 2, 3 |
| | LPRC | TPWRT | TLPRC | 2, 3 |
| | ECPLL | TPWRT | TLOCK | 2, 4 |
| | FRCPLL | TPWRT | TFRC + TLOCK | 2, 3, 4 |
| | XT, HS, SOSC | TPWRT | TOST | 2, 5 |
| | XTPLL, HSPLL | TPWRT | TFRC + TLOCK | 2, 3, 4 |
| All Others | Any Clock | — | — | None |

**Note 1:** TPOR = Power-on Reset delay.

**2:** TPWRT = 64 ms nominal if the Power-up Timer is enabled; otherwise, it is zero.

**3:** TFRC and TLPRC = RC Oscillator start-up times.

**4:** TLOCK = PLL Lock time.

**5:** TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

**6:** If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

**Note:** For detailed operating frequency and timing specifications, see **Section 27.0 "Electrical Characteristics"**.

**REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2**

| R/W-0 | R-0, HSC | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ALTIVT | DISI | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT2EP | INT1EP | INT0EP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Hardware Settable/Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table (AIVT)
0 = Uses standard (default) Interrupt Vector Table (IVT)

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt is on the negative edge
0 = Interrupt is on the positive edge

**REGISTER 8-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | NVMIP2 | NVMIP1 | NVMIP0 | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | AD1IP2 | AD1IP1 | AD1IP0 | — | U1TXIP2 | U1TXIP1 | U1TXIP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **NVMIP<2:0>:** NVM Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** A/D Conversion Complete Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

**REGISTER 8-27: IPC10: INTERRUPT PRIORITY CONTROL REGISTER 10**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | CCT5IP2 | CCT5IP1 | CCT5IP0 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCT5IP<2:0>:** Capture/Compare 5 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

**REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN5(1) | TUN4(1) | TUN3(1) | TUN2(1) | TUN1(1) | TUN0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

011111 = Maximum frequency deviation
011110
•
•
•
000001
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111
•
•
•
100001
100000 = Minimum frequency deviation

**Note 1:** Increments or decrements of TUN<5:0> may not change the FRC frequency in equal steps over the FRC tuning range and may not be monotonic.

### 10.2.2 IDLE MODE

Idle mode includes these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.6 "Selective Peripheral Module Control"**).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction or the first instruction in the ISR.

### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

#### 10.2.3.1 Power-on Resets (PORs)

VDD voltage is monitored to produce PORs. When a true POR occurs, the entire device is reset.

## 10.3 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on pin, RB0, allows a slow falling voltage to generate an interrupt without excess current consumption.

To use this feature:

1. Charge the capacitor on RB0 by configuring the RB0 pin to an output and setting it to '1'.
2. Stop charging the capacitor by configuring RB0 as an input.
3. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the ULPWCON register.
4. Configure Sleep mode.
5. Enter Sleep mode.

When the voltage on RB0 drops below VIL, the device wakes up and executes the next instruction.

This feature provides a low-power technique for periodically waking up the device from Sleep mode.

The time-out is dependent on the discharge time of the RC circuit on RB0.

When the ULPWU module wakes the device from Sleep mode, the ULPWUIF bit (IFS5<0>) is set. Software can check this bit upon wake-up to determine the wake-up source.

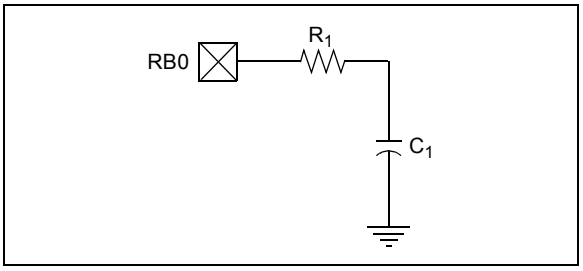
See Example 10-2 for initializing the ULPWU module.

**EXAMPLE 10-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION**

```
//*****************************
// 1. Charge the capacitor on RB0
//*****************************
    TRISBbits.TRISB0 = 0;
    LATBbits.LATB0 = 1;
    for(i = 0; i < 10000; i++) Nop();
//*****************************
//2. Stop Charging the capacitor
//   on RB0
//*****************************
    TRISBbits.TRISB0 = 1;
//*****************************
//3. Enable ULPWU Interrupt
//*****************************
IFS5bits.ULPWUIF = 0;
IEC5bits.ULPWUIE = 1;
IPC21bits.ULPWUIP = 0x7;
//*****************************
//4. Enable the Ultra Low Power
//   Wakeup module and allow
//   capacitor discharge
//*****************************
    ULPWCONbits.ULPEN = 1;
    ULPWCONbit.ULPSINK = 1;
//*****************************
//5. Enter Sleep Mode
//*****************************
    Sleep();
//for sleep, execution will
//resume here
```

A series resistor, between RB0 and the external capacitor provides overcurrent protection for the AN2/ULPWU/RB0 pin and enables software calibration of the time-out (see Figure 10-1).

**FIGURE 10-1: SERIES RESISTOR**




A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired delay in Sleep. This technique compensates for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple, programmable Low-Voltage Detect (LVD) or temperature sensor.

**NOTES:**

**REGISTER 17-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)**

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

**REGISTER 17-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | G4POL | G3POL | G2POL | G1POL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

**REGISTER 17-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| G4D4T | G4D4N | G4D3T | G4D3N | G4D2T | G4D2N | G4D1T | G4D1N |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| G3D4T | G3D4N | G3D3T | G3D3N | G3D2T | G3D2N | G3D1T | G3D1N |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **G4D4T:** Gate 4 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 14 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 13 **G4D3T:** Gate 4 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 12 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 11 **G4D2T:** Gate 4 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 10 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 9 **G4D1T:** Gate 4 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 8 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 7 **G3D4T:** Gate 3 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 6 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 5 **G3D3T:** Gate 3 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 4 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

**REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER (CONTINUED)**

bit 7-5 **CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits
The same definitions as for CHONB<2:0>.

bit 4-0 **CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits
The same definitions as for CHONA<4:0>.

**Note 1:** This is implemented on 44-pin devices only.
**2:** This is implemented on 28-pin and 44-pin devices only.
**3:** The band gap value used for this input is 2x or 4x the internal $V_{BG}$, which is selected when PVCFG<1:0> = 1x.

**REGISTER 19-6: AD1CHITH: A/D SCAN COMPARE HIT REGISTER (HIGH WORD)(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHH23 | CHH22 | CHH21 | CHH20(2) | CHH19(2) | CHH18 | CHH17 | CHH16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'.

bit 7-0 **CHH<23:16>:** A/D Compare Hit bits(2)
If CM<1:0> = 11:
1 = A/D Result Buffer x has been written with data or a match has occurred
0 = A/D Result Buffer x has not been written with data
For All Other Values of CM<1:0>:
1 = A match has occurred on A/D Result Channel x
0 = No match has occurred on A/D Result Channel x

**Note 1:** Unimplemented channels are read as '0'.
**2:** The CHH<20:19> bits are not implemented in 20-pin devices.

**REGISTER 19-7: AD1CHITL: A/D SCAN COMPARE HIT REGISTER (LOW WORD)(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHH15 | CHH14 | CHH13 | CHH12 | CHH11 | CHH10 | CHH9 | CHH8(2,3) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHH7(2,3) | CHH6(2,3) | CHH5(2) | CHH4 | CHH3 | CHH2 | CHH1 | CHH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **CHH<15:0>:** A/D Compare Hit bits(2,3)

If CM<1:0> = 11:
1 = A/D Result Buffer x has been written with data or a match has occurred
0 = A/D Result Buffer x has not been written with data

For All Other Values of CM<1:0>:
1 = A match has occurred on A/D Result Channel x
0 = No match has occurred on A/D Result Channel x

**Note 1:** Unimplemented channels are read as '0'.
**2:** The CHH<8:5> bits are not implemented in 20-pin devices.
**3:** The CHH<8:6> bits are not implemented in 28-pin devices.

## 19.2 A/D Sampling Requirements

The analog input model of the 12-bit A/D Converter is shown in Figure 19-2. The total sampling time for the A/D is a function of the holding capacitor charge time.

For the A/D Converter to meet its specified accuracy, the Charge Holding Capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The Source Impedance (RS), the Interconnect Impedance (RIC) and the Internal Sampling Switch Impedance (RSS) combine to directly affect the time required to charge CHOLD. The combined impedance of the analog sources must, therefore, be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the A/D Converter, the maximum recommended source impedance, RS, is 2.5 kΩ. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

At least 1 TAD time period should be allowed between conversions for the sample time. For more details, see **Section 27.0 "Electrical Characteristics"**.

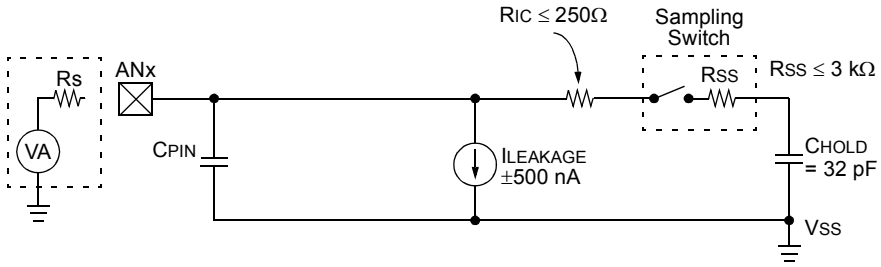
**EQUATION 19-1: A/D CONVERSION CLOCK PERIOD**

$$TAD = TCY\ (ADCS + 1)$$

$$ADCS = \frac{TAD}{TCY} - 1$$

**Note:** Based on TCY = 2/FOSC; Doze mode and PLL are disabled.

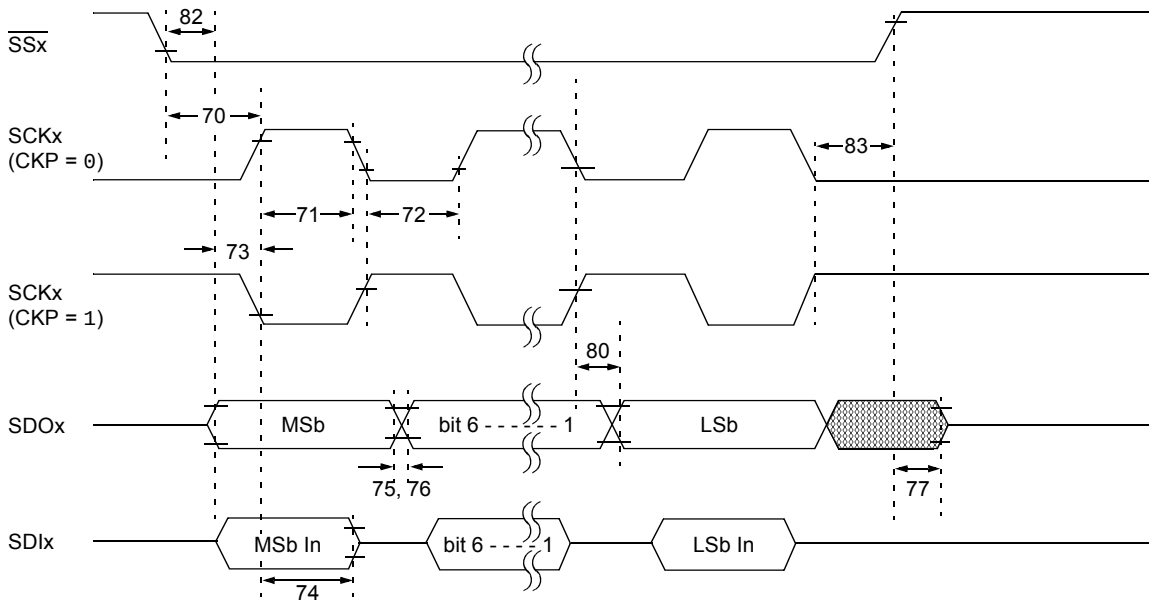
**FIGURE 19-2: 12-BIT A/D CONVERTER ANALOG INPUT MODEL**




**Legend:** CPIN = Input Capacitance
VT = Threshold Voltage
ILEAKAGE = Leakage Current at the Pin Due to Various Junctions
RIC = Interconnect Resistance
RSS = Sampling Switch Resistance
CHOLD = Sample-and-Hold Capacitance (from DAC)

**Note:** The CPIN value depends on the device package and is not tested. The effect of CPIN is negligible if Rs ≤ 5 kΩ.

**FIGURE 27-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)**




**Note:** Refer to Figure 27-5 for load conditions.

**TABLE 27-32: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)**

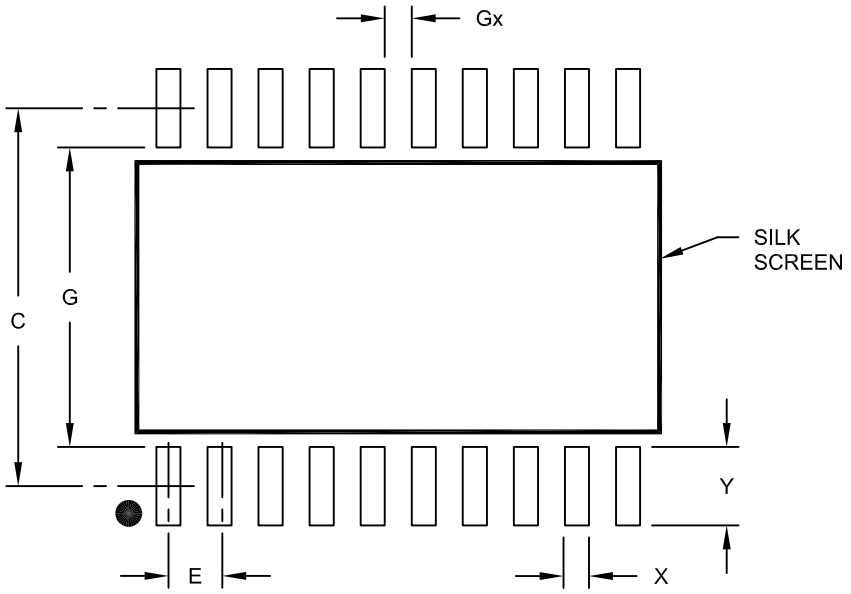
| Param No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | | 3 Tcy | — | ns | |
| 70A | TssL2WB | $\overline{SSx}$ to Write to SSPxBUF | | 3 Tcy | — | ns | |
| 71 | TscH | SCKx Input High Time (Slave mode) | Continuous | 1.25 Tcy + 30 | — | ns | |
| 71A | | | Single Byte | 40 | — | ns | **(Note 1)** |
| 72 | TscL | SCKx Input Low Time (Slave mode) | Continuous | 1.25 Tcy + 30 | — | ns | |
| 72A | | | Single Byte | 40 | — | ns | **(Note 1)** |
| 73A | Tb2b | Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2 | | 1.5 Tcy + 40 | — | ns | **(Note 2)** |
| 74 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | | 40 | — | ns | |
| 75 | TdoR | SDOx Data Output Rise Time | | — | 25 | ns | |
| 76 | TdoF | SDOx Data Output Fall Time | | — | 25 | ns | |
| 77 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance | | 10 | 50 | ns | |
| 80 | TscH2doV, TscL2doV | SDOx Data Output Valid After SCKx Edge | | — | 50 | ns | |
| 82 | TssL2doV | SDOx Data Output Valid After $\overline{SSx}$ ↓ Edge | | — | 50 | ns | |
| 83 | TscH2ssH, TscL2ssH | $\overline{SSx}$ ↑ After SCKx Edge | | 1.5 Tcy + 40 | — | ns | |
| | Fsck | SCKx Frequency | | — | 10 | MHz | |

**Note 1:** Requires the use of Parameter 73A.

**2:** Only if Parameters 71A and 72A are used.

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X20) | X | | | 0.60 |
| Contact Pad Length (X20) | Y | | | 1.95 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.45 | | |

Notes:

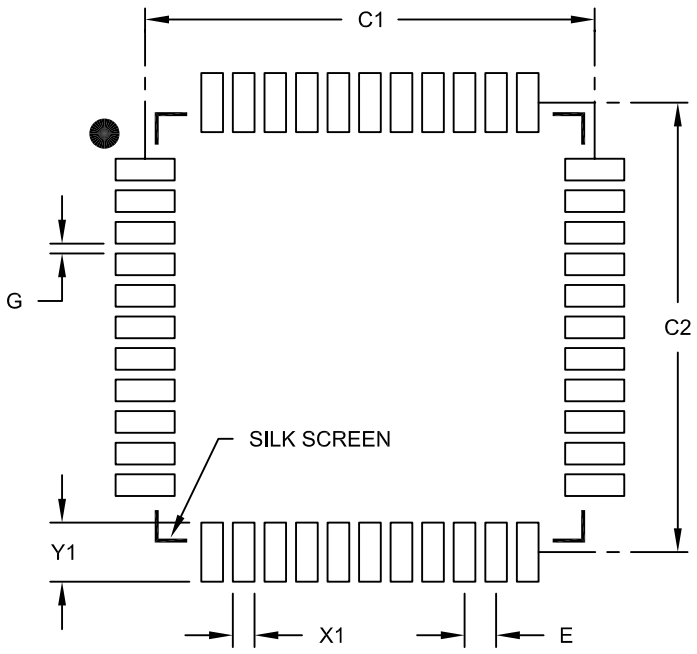
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.80 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X44) | X1 | | | 0.55 |
| Contact Pad Length (X44) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

**NOTES:**