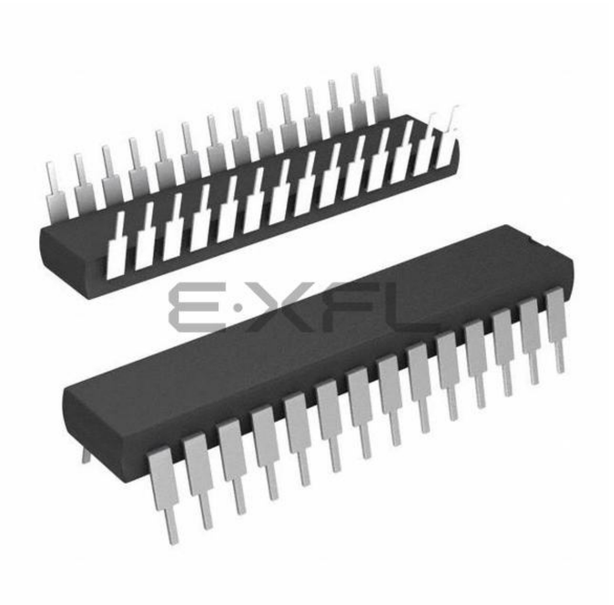

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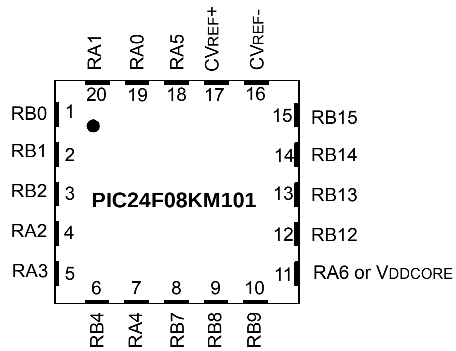
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 8KB (2.75K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5V |
| Data Converters | A/D 19x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km102-i-sp |

## Pin Diagrams (Continued)

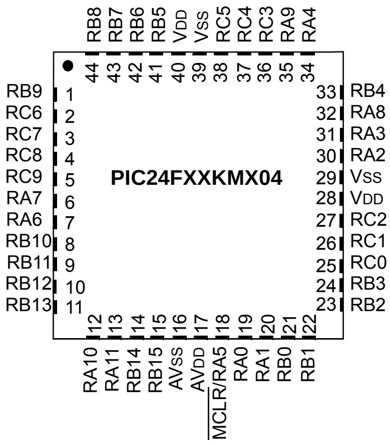
**20-Pin QFN**




| Pin | Pin Features | |
|---|---|---|
| | PIC24F08KM101 | PIC24FV08KM101 |
| 1 | PGED1/AN2/CTCMP/ULPWU/C1IND/OC2A/CN4/RB0 | |
| 2 | PGEC1/AN3/C1INC/CTED12/CN5/RB1 | |
| 3 | AN4/U1RX/TCKIB/CTED13/CN6/RB2 | |
| 4 | OSCI/CLKI/AN13/C1INB/CN30/RA2 | |
| 5 | OSCO/CLKO/AN14/C1INA/CN29/RA3 | |
| 6 | PGED3/SOSCI/AN15/CLCINA/CN1/RB4 | |
| 7 | PGEC3/SOSCO/SCLKI/AN16/PWRLCLK/CLCINB/CN0/RA4 | |
| 8 | AN19/U1TX/CTED1/INT0/CN23/RB7 | AN19/U1TX/IC1/OC1A/CTED1/INT0/CN23/RB7 |
| 9 | AN20/SCL1/$\overline{\text{U1CTS}}$/OC1B/CTED10/CN22/RB8 | |
| 10 | AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/CLC1O/CTED4/CN21/RB9 | |
| 11 | IC1/OC1A/INT2/CN8/RA6 | VCAP OR VDDCORE |
| 12 | AN12/HLVDIN/SCK1/OC1C/CTED2/CN14/RB12 | AN12/HLVDIN/SCK1/OC1C/CTED2/INT2/CN14/RB12 |
| 13 | AN11/SDO1/OCFB/OC1D/CTPLS/CN13/RB13 | |
| 14 | CVREF/AN10/SDI1/C1OUT/OCFA/CTED5/INT1/CN12/RB14 | |
| 15 | AN9/REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15 | |
| 16 | VSS/AVSS | |
| 17 | VDD/AVDD | |
| 18 | $\overline{\text{MCLR}}$/VPP/RA5 | |
| 19 | PGEC2/CVREF+ /VREF+/AN0/CN2/RA0 | |
| 20 | PGED2/CVREF-/VREF-/AN1/CN3/RA1 | |

## Pin Diagrams (Continued)

**44-Pin TQFP/QFN[1]**




| Pin | Pin Features: PIC24FXXKMX04 | Pin Features: PIC24FVXXKMX04 |
|---|---|---|
| 1 | AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/ /CLC1O/CTED4/CN21/RB9 | |
| 2 | U1RX/ /CN18/RC6 | |
| 3 | U1TX/ /CN17/RC7 | |
| 4 | /CN20/RC8 | |
| 5 | IC4/OC2F/CTED7/CN19/RC9 | |
| 6 | IC1/ / /CTED3/CN9/RA7 | |
| 7 | /OC1A/CTED1/INT2/CN8/RA6 | VCAP or VDDCORE |
| 8 | PGED2/SDI1/OC1C/CTED11/CN16/RB10 | |
| 9 | PGEC2/SCK1/OC2A/CTED9/CN15/RB11 | |
| 10 | /AN12/HLVDIN/ /CTED2/ CN14/RB12 | /AN12/HLVDIN/ /CTED2/INT2/ CN14/RB12 |
| 11 | / /AN11/SDO1/OC1D/CTPLS/CN13/RB13 | |
| 12 | / /CN35/RA10 | |
| 13 | / /CTED8/CN36/RA11 | |
| 14 | /CVREF/ / /AN10/ / /C1OUT/OCFA/CTED5/INT1/CN12/ RB14 | |
| 15 | / /AN9/ /REFO/SS1/TCKIA/CTED6/CN11/RB15 | |
| 16 | AVSS | |
| 17 | AVDD | |
| 18 | MCLR/VPP/RA5 | |
| 19 | CVREF+/VREF+/ /AN0/ /CN2/ RA0 | CVREF+/VREF+/ /AN0/ / CTED1/CN2/RA0 |
| 20 | CVREF-/VREF-/AN1/CN3/RA1 | |
| 21 | PGED1/AN2/CTCMP/ULPWU/C1IND/ / / /CN4/RB0 | |
| 22 | PGEC1/ / /AN3/C1INC/ / /CTED12/CN5//RB1 | |
| 23 | / /AN4/C1INB/ / /TCKIB/CTED13/CN6/RB2 | |
| 24 | /AN5/C1INA/ / /CN7/RB3 | |
| 25 | AN6/CN32/RC0 | |
| 26 | AN7/CN31/RC1 | |
| 27 | AN8/CN10/RC2 | |
| 28 | VDD | |
| 29 | VSS | |
| 30 | OSCI/CLKI/AN13/CN30/RA2 | |
| 31 | OSCO/CLKO/AN14/CN29/RA3 | |
| 32 | OCFB/CN33/RA8 | |
| 33 | SOSCI/AN15/ / /CN1/RB4 | |
| 34 | SOSCO/SCLKI/AN16/PWRLCLK/ /CN0/RA4 | |
| 35 | /CN34/RA9 | |
| 36 | /CN28/RC3 | |
| 37 | /CN25/RC4 | |
| 38 | /CN26/RC5 | |
| 39 | VSS | |
| 40 | VDD | |
| 41 | PGED3/AN17/ASDA1/OC1E/CLCINA/CN27/RB5 | |
| 42 | PGEC3/AN18/ASCL1/OC1F/CLCINB/CN24/RB6 | |
| 43 | AN19/INT0/CN23/RB7 | AN19/ /OC1A/INT0/CN23/RB7 |
| 44 | AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8 | |

**Legend:** Values in indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

**Note 1:** Exposed pad on underside of device is connected to VSS.

## 4.2 Data Address Space

The PIC24F core has a separate, 16-bit-wide data memory space, addressable as a single linear range. The Data Space is accessed using two Address Generation Units (AGUs), one each for read and write operations. The Data Space memory map is displayed in Figure 4-3.

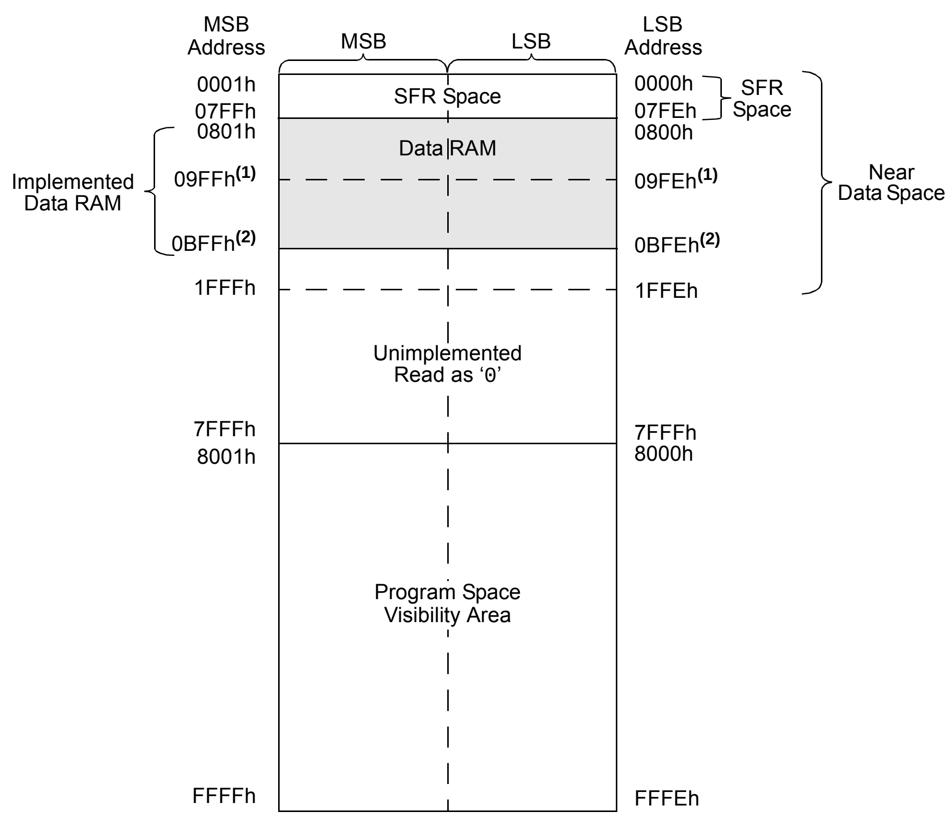
All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This gives a Data Space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility (PSV) area (see **Section 4.3.3 "Reading Data From Program Memory Using Program Space Visibility"**).

Depending on the particular device, PIC24FV16KM family devices implement either 512 or 1024 words of data memory. Should an EA point to a location outside of this area, an all zero word or byte will be returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all the Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

**FIGURE 4-3: DATA SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES(3)**




**Note 1:** Upper data memory boundary for PIC24FXXKM10X devices.
**2:** Upper data memory boundary for PIC24FXXKM20X devices.
**3:** Data memory areas are not shown to scale.

## TABLE 4-9: MCCP2 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCP2CON1L | 164h | CCPON | — | CCPSIDL | r | TMRSYNC | CLKSEL2 | CLKSEL1 | CLKSEL0 | TMRPS1 | TMRPS0 | T32 | CCSEL | MOD3 | MOD2 | MOD1 | MOD0 | 0000 |
| CCP2CON1H | 166h | OPSSRC | RTRGEN | — | — | IOPS3 | IOPS2 | IOPS1 | IOPS0 | TRIGEN | ONESHOT | ALTSYNC | SYNC4 | SYNC3 | SYNC2 | SYNC1 | SYNC0 | 0000 |
| CCP2CON2L | 168h | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 | 0000 |
| CCP2CON2H | 16Ah | OENSYNC | — | OCFEN(1) | OCEEN(1) | OCDEN(1) | OCCEN(1) | OCBEN(1) | OCAEN | ICGSM1 | ICGSM0 | — | AUXOUT1 | AUXOUT0 | ICSEL2 | ICSEL1 | ICSEL0 | 0100 |
| CCP2CON3L | 16Ch | — | — | — | — | — | — | — | — | — | | DT5 | DT4 | DT3 | DT2 | DT1 | DT0 | 0000 |
| CCP2CON3H | 16Eh | OETRIG | OSCNT2 | OSCNT1 | OSCNT0 | — | OUTM2(1) | OUTM1(1) | OUTM0(1) | — | — | POLACE | POLBDF(1) | PSSACE1 | PSSACE0 | PSSBDF1(1) | PSSBDF0(1) | 0000 |
| CCP2STATL | 170h | — | — | — | — | — | — | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| CCP2TMRL | 174h | MCCP2 Time Base Register Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP2TMRH | 176h | MCCP2 Time Base Register High Word | | | | | | | | | | | | | | | | 0000 |
| CCP2PRL | 178h | MCCP2 Time Base Period Register Low Word | | | | | | | | | | | | | | | | FFFF |
| CCP2PRH | 17Ah | MCCP2 Time Base Period Register High Word | | | | | | | | | | | | | | | | FFFF |
| CCP2RAL | 17Ch | Output Compare 2 Data Word A | | | | | | | | | | | | | | | | 0000 |
| CCP2RBL | 180h | Output Compare 2 Data Word B | | | | | | | | | | | | | | | | 0000 |
| CCP2BUFL | 184h | Input Capture 2 Data Buffer Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP2BUFH | 186h | Input Capture 2 Data Buffer High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
**Note 1:** These bits are available only on PIC24F(V)16KM2XX devices.

**TABLE 4-10: MCCP3 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCP3CON1L(1) | 188h | CCPON | — | CCPSIDL | r | TMRSYNC | CLKSEL2 | CLKSEL1 | CLKSEL0 | TMRPS1 | TMRPS0 | T32 | CCSEL | MOD3 | MOD2 | MOD1 | MOD0 | 0000 |
| CCP3CON1H(1) | 18Ah | OPSSRC | RTRGEN | — | — | IOPS3 | IOPS2 | IOPS1 | IOPS0 | TRIGEN | ONESHOT | ALTSYNC | SYNC4 | SYNC3 | SYNC2 | SYNC1 | SYNC0 | 0000 |
| CCP3CON2L(1) | 18Ch | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 | 0000 |
| CCP3CON2H(1) | 18Eh | OENSYNC | — | OCFEN | OCEEN | OCDEN | OCCEN | OCBEN | OCAEN | ICGSM1 | ICGSM0 | — | AUXOUT1 | AUXOUT0 | ICS2 | ICS1 | ICS0 | 0100 |
| CCP3CON3L(1) | 190h | — | — | — | — | — | — | — | — | — | — | DT5 | DT4 | DT3 | DT2 | DT1 | DT0 | 0000 |
| CCP3CON3H(1) | 192h | OETRIG | OSCNT2 | OSCNT1 | OSCNT0 | — | OUTM2 | OUTM1 | OUTM0 | — | — | POLACE | POLBDF | PSSACE1 | PSSACE0 | PSSBDF1 | PSSBDF0 | 0000 |
| CCP3STAT(1) | 194h | — | — | — | — | — | — | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| CCP3TMRL(1) | 198h | MCCP3 Time Base Register Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP3TMRH(1) | 19Ah | MCCP3 Time Base Register High Word | | | | | | | | | | | | | | | | 0000 |
| CCP3PRL(1) | 19Ch | MCCP3 Time Base Period Register Low Word | | | | | | | | | | | | | | | | FFFF |
| CCP3PRH(1) | 19Eh | MCCP3 Time Base Period Register High Word | | | | | | | | | | | | | | | | FFFF |
| CCP3RAL(1) | 1A0h | Output Compare 3 Data Word A | | | | | | | | | | | | | | | | 0000 |
| CCP3RBL(1) | 1A4h | Output Compare 3 Data Word B | | | | | | | | | | | | | | | | 0000 |
| CCP3BUFL(1) | 1A8h | Input Capture 3 Data Buffer Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP3BUFH(1) | 1AAh | Input Capture 3 Data Buffer High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These registers are available only on PIC24F(V)16KM2XX devices.

## TABLE 4-11: SCCP4 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCP4CON1L(1) | 1ACh | CCPON | — | CCPSIDL | r | TMRSYNC | CLKSEL2 | CLKSEL1 | CLKSEL0 | TMRPS1 | TMRPS0 | T32 | CCSEL | MOD3 | MOD2 | MOD1 | MOD0 | 0000 |
| CCP4CON1H(1) | 1AEh | OPSSRC | RTRGEN | — | — | IOPS3 | IOPS2 | IOPS1 | IOPS0 | TRIGEN | ONESHOT | ALTSYNC | SYNC4 | SYNC3 | SYNC2 | SYNC1 | SYNC0 | 0000 |
| CCP4CON2L(1) | 1B0h | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 | 0000 |
| CCP4CON2H(1) | 1B2h | OENSYNC | — | — | — | — | — | — | OCAEN | ICGSM1 | ICGSM0 | — | AUXOUT1 | AUXOUT0 | ICSEL2 | ICSEL1 | ICSEL0 | 0100 |
| CCP4CON3H(1) | 1B6h | OETRIG | OSCNT2 | OSCNT1 | OSCNT0 | — | — | — | — | — | — | POLACE | — | PSSACE1 | PSSACE0 | — | — | 0000 |
| CCP4STATL(1) | 1B8h | — | — | — | — | — | — | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| CCP4TMRL(1) | 1BCh | SCCP4 Time Base Register Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP4TMRH(1) | 1BEh | SCCP4 Time Base Register High Word | | | | | | | | | | | | | | | | 0000 |
| CCP4PRL(1) | 1C0h | SCCP4 Time Base Period Register Low Word | | | | | | | | | | | | | | | | FFFF |
| CCP4PRH(1) | 1C2h | SCCP4 Time Base Period Register High Word | | | | | | | | | | | | | | | | FFFF |
| CCP4RAL(1) | 1C4h | Output Compare 4 Data Word A | | | | | | | | | | | | | | | | 0000 |
| CCP4RBL(1) | 1C8h | Output Compare 4 Data Word B | | | | | | | | | | | | | | | | 0000 |
| CCP4BUFL(1) | 1CCh | Input Capture 4 Data Buffer Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP4BUFH(1) | 1CEh | Input Capture 4 Data Buffer High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These registers are available only on PIC24F(V)16KM2XX devices.

## TABLE 4-12: SCCP5 REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CCP5CON1L(1) | 1D0h | CCPON | — | CCPSIDL | r | TMRSYNC | CLKSEL2 | CLKSEL1 | CLKSEL0 | TMRPS1 | TMRPS0 | T32 | CCSEL | MOD3 | MOD2 | MOD1 | MOD0 | 0000 |
| CCP5CON1H(1) | 1D2h | OPSSRC | RTRGEN | — | — | IOPS3 | IOPS2 | IOPS1 | IOPS0 | TRIGEN | ONESHOT | ALTSYNC | SYNC4 | SYNC3 | SYNC2 | SYNC1 | SYNC0 | 0000 |
| CCP5CON2L(1) | 1D4h | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG7 | ASDG6 | ASDG5 | ASDG4 | ASDG3 | ASDG2 | ASDG1 | ASDG0 | 0000 |
| CCP5CON2H(1) | 1D6h | OENSYNC | — | — | — | — | — | — | OCAEN | ICGSM1 | ICGSM0 | — | AUXOUT1 | AUXOUT0 | ICSEL2 | ICSEL1 | ICSEL0 | 0100 |
| CCP5CON3H(1) | 1DAh | OETRIG | OSCNT2 | OSCNT1 | OSCNT0 | — | — | — | — | — | — | POLACE | — | PSSACE1 | PSSACE0 | — | — | 0000 |
| CCP5STATL(1) | 1DCh | — | — | — | — | — | — | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| CCP5TMRL(1) | 1E0h | SCCP5 Time Base Register Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP5TMRH(1) | 1E2h | SCCP5 Time Base Register High Word | | | | | | | | | | | | | | | | 0000 |
| CCP5PRL(1) | 1E4h | SCCP5 Time Base Period Register Low Word | | | | | | | | | | | | | | | | FFFF |
| CCP5PRH(1) | 1E6h | SCCP5 Time Base Period Register High Word | | | | | | | | | | | | | | | | FFFF |
| CCP5RAL(1) | 1E8h | Output Compare 5 Data Word A | | | | | | | | | | | | | | | | 0000 |
| CCP5RBL(1) | 1ECh | Output Compare 5 Data Word B | | | | | | | | | | | | | | | | 0000 |
| CCP5BUFL(1) | 1F0h | Input Capture 5 Data Buffer Low Word | | | | | | | | | | | | | | | | 0000 |
| CCP5BUFH(1) | 1F2h | Input Capture 5 Data Buffer High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These registers are available only on PIC24F(V)16KM2XX devices.

### 5.5.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time by erasing the programmable row. The general process is:

1. Read a row of program memory (32 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase a row (see Example 5-1):
   a) Set the NVMOPx bits (NVMCON<5:0>) to '011000' to configure for row erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
   b) Write the starting address of the block to be erased into the TBLPAG and W registers.
   c) Write 55h to NVMKEY.
   d) Write AAh to NVMKEY.
   e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 32 instructions from data RAM into the program memory buffers (see Example 5-1).
5. Write the program block to Flash memory:
   a) Set the NVMOPx bits to '000100' to configure for row programming. Clear the ERASE bit and set the WREN bit.
   b) Write 55h to NVMKEY.
   c) Write AAh to NVMKEY.
   d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as displayed in Example 5-5.

**EXAMPLE 5-1: ERASING A PROGRAM MEMORY ROW – ASSEMBLY LANGUAGE CODE**

```
; Set up NVMCON for row erase operation
       MOV     #0x4058, W0                  ;
       MOV     W0, NVMCON                   ; Initialize NVMCON
; Init pointer to row to be ERASED
       MOV     #tblpage(PROG_ADDR), W0      ;
       MOV     W0, TBLPAG                   ; Initialize PM Page Boundary SFR
       MOV     #tbloffset(PROG_ADDR), W0    ; Initialize in-page EA[15:0] pointer
       TBLWTL  W0, [W0]                     ; Set base address of erase block
       DISI    #5                           ; Block all interrupts
                                              for next 5 instructions
       MOV     #0x55, W0
       MOV     W0, NVMKEY                   ; Write the 55 key
       MOV     #0xAA, W1                    ;
       MOV     W1, NVMKEY                   ; Write the AA key
       BSET    NVMCON, #WR                  ; Start the erase sequence
       NOP                                  ; Insert two NOPs after the erase
       NOP                                  ; command is asserted
```

**EXAMPLE 5-2: ERASING A PROGRAM MEMORY ROW – 'C' LANGUAGE CODE**

```
// C example using MPLAB C30

int __attribute__ ((space(auto_psv))) progAddr = 0x1234;    // Variable located in Pgm Memory, declared as a
                                                            // global variable
    unsigned int offset;

//Set up pointer to the first memory location to be written

    TBLPAG = __builtin_tblpage(&progAddr);                  // Initialize PM Page Boundary SFR
    offset = __builtin_tbloffset(&progAddr);                // Initialize lower word of address

    __builtin_tblwtl(offset, 0x0000);                       // Set base address of erase block
                                                            // with dummy latch write

    NVMCON = 0x4058;                                        // Initialize NVMCON

    asm("DISI #5");                                         // Block all interrupts for next 5 instructions
    __builtin_write_NVM();                                  // C30 function to perform unlock
                                                            // sequence and set WR
```

### REGISTER 8-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CCP5IP2 | CCP5IP1 | CCP5IP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT1IP2 | INT1IP1 | INT1IP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as ‘0’

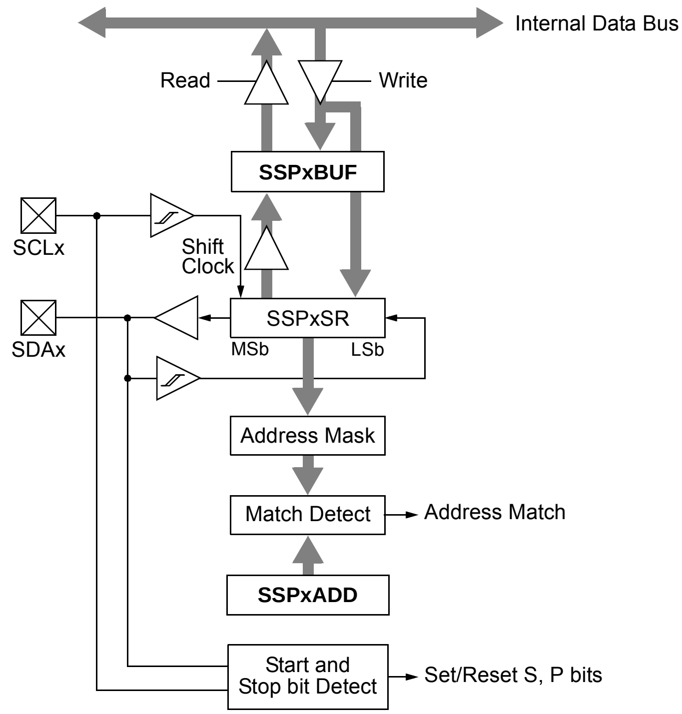
bit 10-8 **CCP5IP<2:0>:** Capture/Compare 5 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

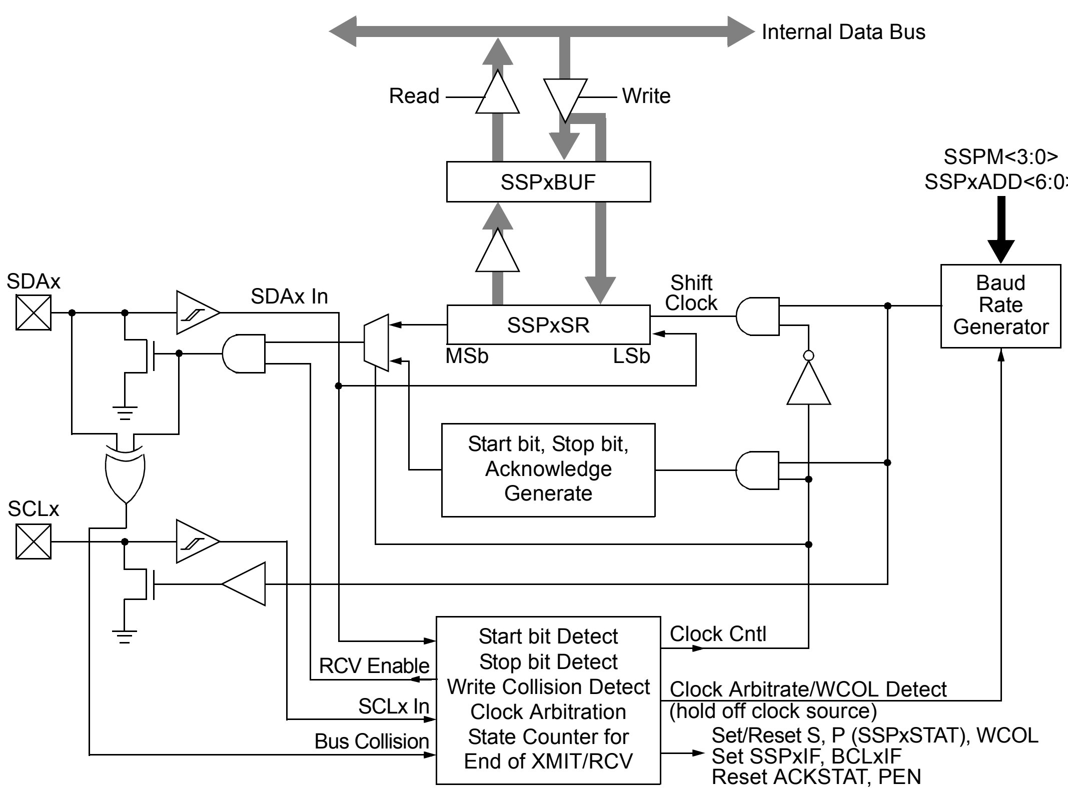
**NOTES:**

**FIGURE 14-3: MSSPx BLOCK DIAGRAM (I²C™ MODE)**




**Note:** Only port I/O names are shown in this diagram. Refer to the text for a full list of multiplexed functions.

**FIGURE 14-4: MSSPx BLOCK DIAGRAM (I²C™ MASTER MODE)**



**REGISTER 15-1: UxMODE: UARTx MODE REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0(2) | R/W-0(2) |
|---|---|---|---|---|---|---|---|
| UARTEN | — | USIDL | IREN(1) | RTSMD | — | UEN1 | UEN0 |
| bit 15 | | | | | | | bit 8 |

| R/C-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **UARTEN:** UARTx Enable bit
1 = UARTx is enabled; all UARTx pins are controlled by UARTx, as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by port latches, UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(1)
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **UEN<1:0>:** UARTx Enable bits(2)
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
1 = UARTx will continue to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Enables Loopback mode
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is ‘0’
0 = UxRX Idle state is ‘1’

**Note 1:** This feature is is only available for the 16x BRG mode (BRGH = 0).
**2:** The bit availability depends on the pin availability.

### REGISTER 16-2: RTCPWC: RTCC CONFIGURATION REGISTER 2[1]

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PWCEN | PWCPOL | PWCCPRE | PWCSPRE | RTCCLK1[2] | RTCCLK0[2] | RTCOUT1 | RTCOUT0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 14 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 13 **PWCCPRE:** Power Control/Stability Prescaler bits
1 = PWC stability window clock is divide-by-2 of source RTCC clock
0 = PWC stability window clock is divide-by-1 of source RTCC clock

bit 12 **PWCSPRE:** Power Control Sample Prescaler bits
1 = PWC sample window clock is divide-by-2 of source RTCC clock
0 = PWC sample window clock is divide-by-1 of source RTCC clock

bit 11-10 **RTCCLK<1:0>:** RTCC Clock Select bits[2]
Determines the source of the internal RTCC clock, which is used for all RTCC timer operations.
00 = External Secondary Oscillator (SOSC)
01 = Internal LPRC Oscillator
10 = External power line source – 50 Hz
11 = External power line source – 60 Hz

bit 9-8 **RTCOUT<1:0>:** RTCC Output Select bits
Determines the source of the RTCC pin output.
00 = RTCC alarm pulse
01 = RTCC seconds clock
10 = RTCC clock
11 = Power control

bit 7-0 **Unimplemented:** Read as ‘0’

**Note 1:** The RTCPWC register is only affected by a POR.
**2:** When a new value is written to these register bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

### 16.2.5 RTCVAL REGISTER MAPPINGS

**REGISTER 16-4: YEAR: YEAR VALUE REGISTER[(1)]**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| YRTEN3 | YRTEN2 | YRTEN1 | YRTEN0 | YRONE3 | YRONE2 | YRONE1 | YRONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year’s Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year’s Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to the YEAR register is only allowed when RTCWREN = 1.

**REGISTER 16-5: MTHDY: MONTH AND DAY VALUE REGISTER[(1)]**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | MTHTEN0 | MTHONE3 | MTHONE2 | MTHONE1 | MTHONE0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | DAYTEN1 | DAYTEN0 | DAYONE3 | DAYONE2 | DAYONE1 | DAYONE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit bit
Contains a value of ‘0’ or ‘1’.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month’s Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day’s Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day’s Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

## 19.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

### 19.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSH and AD1CSSL: A/D Input Scan Select Registers
- AD1CTMENH and AD1CTMENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 19-1, Register 19-2 and Register 19-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion Triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 19-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 19-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 19-6 and Register 19-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases, indicates if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 19-8 and Register 19-9) select the channels to be included for sequential scanning.

The AD1CTMENH/L registers (Register 19-10 and Register 19-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMENL is always implemented, whereas AD1CTMENH may not be implemented in devices with 16 or fewer channels.

### 19.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port buffer, called ADC1BUFx. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFx (x = up to 17).

The A/D result buffers are both readable and writable. When the module is active (AD1CON<15> = 1), the buffers are read-only and store the results of A/D conversions. When the module is inactive (AD1CON<15> = 0), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1<15>). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

### REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PVCFG1 | PVCFG0 | NVCFG0 | — | BUFREGEN | CSCNA | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUFS(1) | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM(1) | ALTS |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **PVCFG<1:0>:** A/D Converter Positive Voltage Reference Configuration bits
11 = 4 * Internal $V_{BG}$(2)
10 = 2 * Internal $V_{BG}$(3)
01 = External $V_{REF+}$
00 = $AV_{DD}$

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bits
1 = External $V_{REF-}$
0 = $AV_{SS}$

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into a buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ S/H Input for MUX A Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **BUFS:** A/D Buffer Fill Status bit(1)
1 = A/D is filling the upper half of the buffer; user should access data in the lower half
0 = A/D is filling the lower half of the buffer; user should access data in the upper half

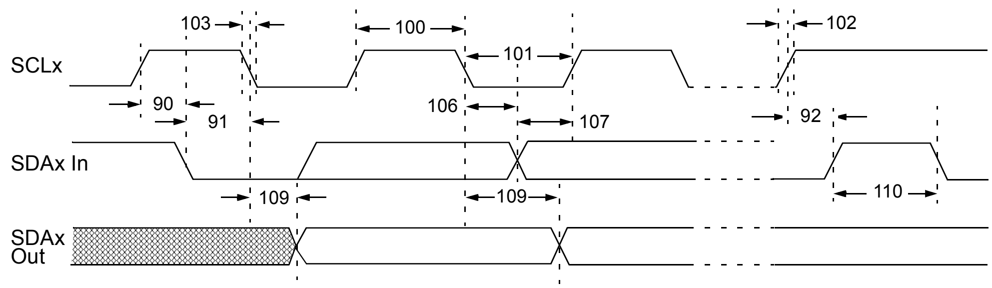
bit 6-2 **SMPI<4:0>:** Interrupt Sample Rate Select bits
11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
•
•
•
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

bit 1 **BUFM:** A/D Buffer Fill Mode Select bit(1)
1 = Starts filling the buffer at address, ADC1BUF0, on the first interrupt and ADC1BUF(x/2) on the next interrupt (Split Buffer mode)
0 = Starts filling the buffer at address, ADC1BUF0, and each sequential address on successive interrupts (FIFO mode)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
0 = Always uses channel input selects for Sample A

**Note 1:** This is only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.
**2:** PIC24FV16KMXXX devices only. Reference setting will not be within specification for $V_{DD}$ below 4.5V.
**3:** Reference setting will not be within specification for $V_{DD}$ below 2.3V.

**FIGURE 27-18: MSSPx I²C™ BUS DATA TIMING**




**Note:** Refer to Figure 27-5 for load conditions.

**TABLE 27-36: I²C™ BUS DATA REQUIREMENTS (MASTER MODE)**

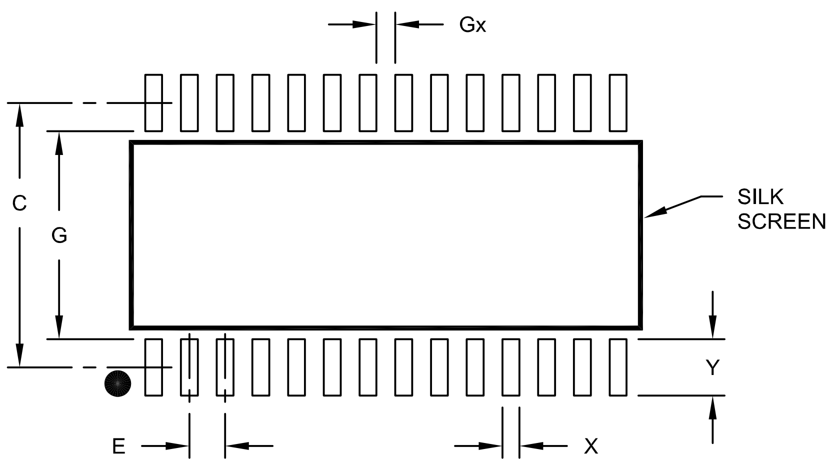
| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 100 | THIGH | Clock High Time | 100 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| | | | 400 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| 101 | TLOW | Clock Low Time | 100 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| | | | 400 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| 102 | TR | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| 103 | TF | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| 90 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 2(TOSC)(BRG + 1) | — | — | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| 91 | THD:STA | Start Condition Hold Time | 100 kHz mode | 2(TOSC)(BRG + 1) | — | — | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| 106 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| 107 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | **(Note 1)** |
| | | | 400 kHz mode | 100 | — | ns | |
| 92 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| | | | 400 kHz mode | 2(TOSC)(BRG + 1) | — | — | |
| 109 | TAA | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| 110 | TBUF | Bus Free Time | 100 kHz mode | 4.7 | — | μs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| D102 | CB | Bus Capacitive Loading | | — | 400 | pF | |

**Note 1:** A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but Parameter 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, Parameter 102 + Parameter 107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCLx line is released.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| | | Units | MILLIMETERS | | |
|---|---|---|---|---|---|
| | | Dimension Limits | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | | |
| Contact Pad Spacing | C | | | 9.40 | |
| Contact Pad Width (X28) | X | | | | 0.60 |
| Contact Pad Length (X28) | Y | | | | 2.00 |
| Distance Between Pads | Gx | | 0.67 | | |
| Distance Between Pads | G | | 7.40 | | |

Notes:

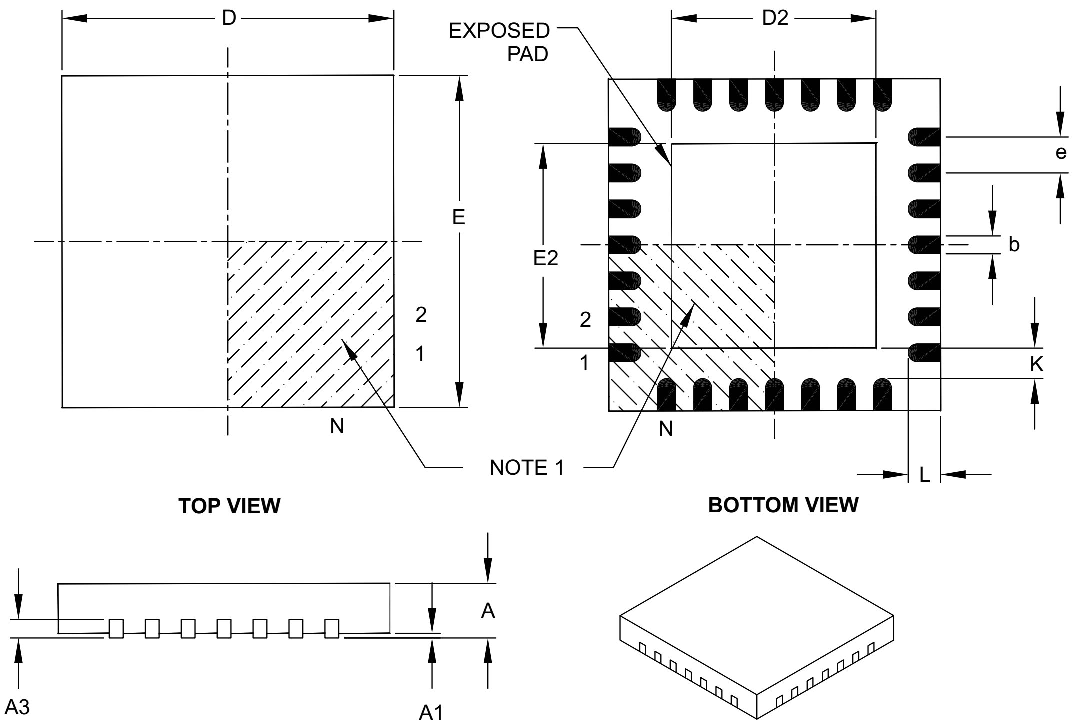
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.20 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.20 |
| Contact Width | b | 0.23 | 0.30 | 0.35 |
| Contact Length | L | 0.50 | 0.55 | 0.70 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

**NOTES:**