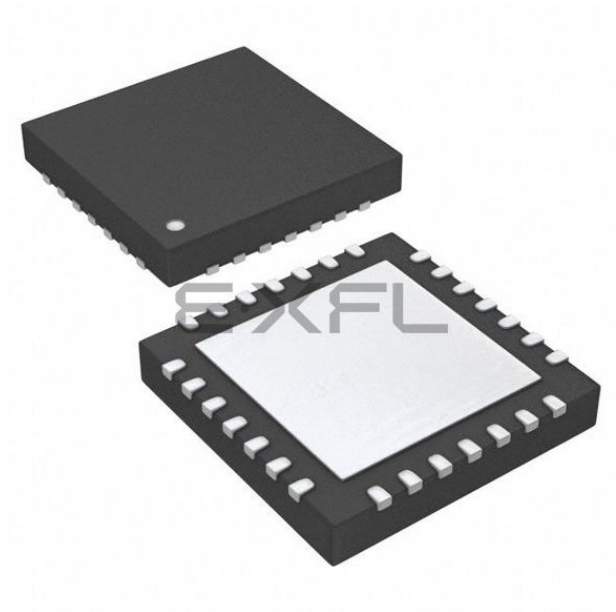
Microchip Technology - PIC24FV08KM102T-I/ML Datasheet



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What is "Embedded - Microcontrollers"?

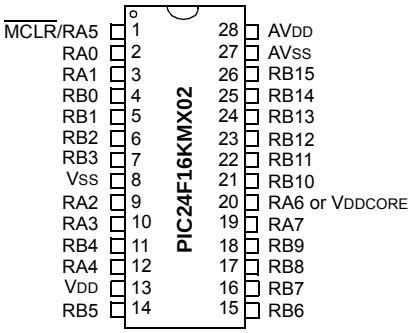
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km102t-i-ml

Pin Diagrams (Continued)

28-Pin SPDIP/SSOP/SOIC



Pin	Pin Features	
	PIC24FXXKMX02	PIC24FVXXKMX02
1	MCLR/VPP/RA5	
2	CVREF+/VREF+/ /AN0/ /CN2/RA0	
3	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/RA1
4	PGED1/AN2/CTCMP/ULPWU/C1IND/ / / /CN4/RB0	
5	PGEC1/ / /AN3/C1INC/ / /CTED12/CN5/RB1	
6	/ /AN4/C1INB/ / /U1RX/TCKIB/CTED13/CN6/RB2	
7	/AN5/C1INA/ / /CN7/RB3	
8	VSS	
9	OSCI/CLKI/AN13/CN30/RA2	
10	OSCO/CLKO/AN14/CN29/RA3	
11	SOSCI/AN15/ / /CN1/RB4	
12	SOSCO/SCLKI/AN16/PWRLCLK/ /CN0/RA4	
13	VDD	
14	PGED3/AN17/ASDA1/ / /OC1E/CLCINA/CN27/RB5	
15	PGEC3/AN18/ASCL1/ / /OC1F/CLCINB/CN24/RB6	
16	AN19/U1TX/INT0/CN23/RB7	AN19/U1TX/ / /INT0/CN23/RB7
17	AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8	
18	AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/ /CLC1O/CTED4/CN21/RB9	
19	/IC1/ / /CTED3/CN9/RA7	
20	/OC1A/CTED1/INT2/CN8/RA6	VCAP OR VDDCORE
21	PGED2/SDI1/ /OC1C/CTED11/CN16/RB10	
22	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
23	/AN12/HLVDIN/ / / /CTED2/CN14/RB12	/AN12/HLVDIN/ / / /CTED2/INT2/CN14/RB12
24	/ /AN11/SDO1/OCFB/ /OC1D/CTPLS/CN13/RB13	
25	/CVREF/ / /AN10/ / /C1OUT/OCFA/CTED5/INT1/CN12/RB14	
26	/ /AN9/ /REFO/SS1/TCKIA/CTED6/CN11/RB15	
27	VSS/AVSS	
28	VDD/AVDD	

Legend: Values in indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24F16KM204 FAMILY

Features	PIC24F16KM204	PIC24F08KM204	PIC24F16KM202	PIC24F08KM202
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	8K	16K	8K
Program Memory (instructions)	5632	2816	5632	2816
Data Memory (bytes)	2048			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	40 (36/4)			
Voltage Range	1.8-3.6V			
I/O Ports	PORTA<11:0> PORTB<15:0> PORTC<9:0>		PORTA<7:0> PORTB<15:0>	
Total I/O Pins	38		24	
Timers	11 (One 16-bit timer, five MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 3 2			
Serial Communications MSSP UART	 2 2			
Input Change Notification Interrupt	37		23	
12-Bit Analog-to-Digital Module (input channels)	22	22	19	19
Analog Comparators	3			
8-Bit Digital-to-Analog Converters	2			
Operational Amplifiers	2			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	Yes			
Configurable Logic Cell (CLC)	2			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN		28-Pin SPDIP/SSOP/SOIC/QFN	

NOTES:

REGISTER 3-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0, HSC	R/W-0	U-0	U-0
—	—	—	—	IPL3(1)	PSV	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
1 = Program space is visible in Data Space
0 = Program space is not visible in Data Space

bit 1-0 **Unimplemented:** Read as '0'

Note 1: User interrupts are disabled when IPL3 = 1.

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware division for 16-bit divisor.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

7.4.2 SOFTWARE ENABLED BOR

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON<13>). Setting SBOREN enables the BOR to function as previously described. Clearing the SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise, it is read as '0'.

Placing BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change the BOR configuration. It also allows the user to tailor the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when the BOR is under software control, the Brown-out Reset voltage level is still set by the BORV<1:0> Configuration bits; it can not be changed in software.

7.4.3 DETECTING BOR

When BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

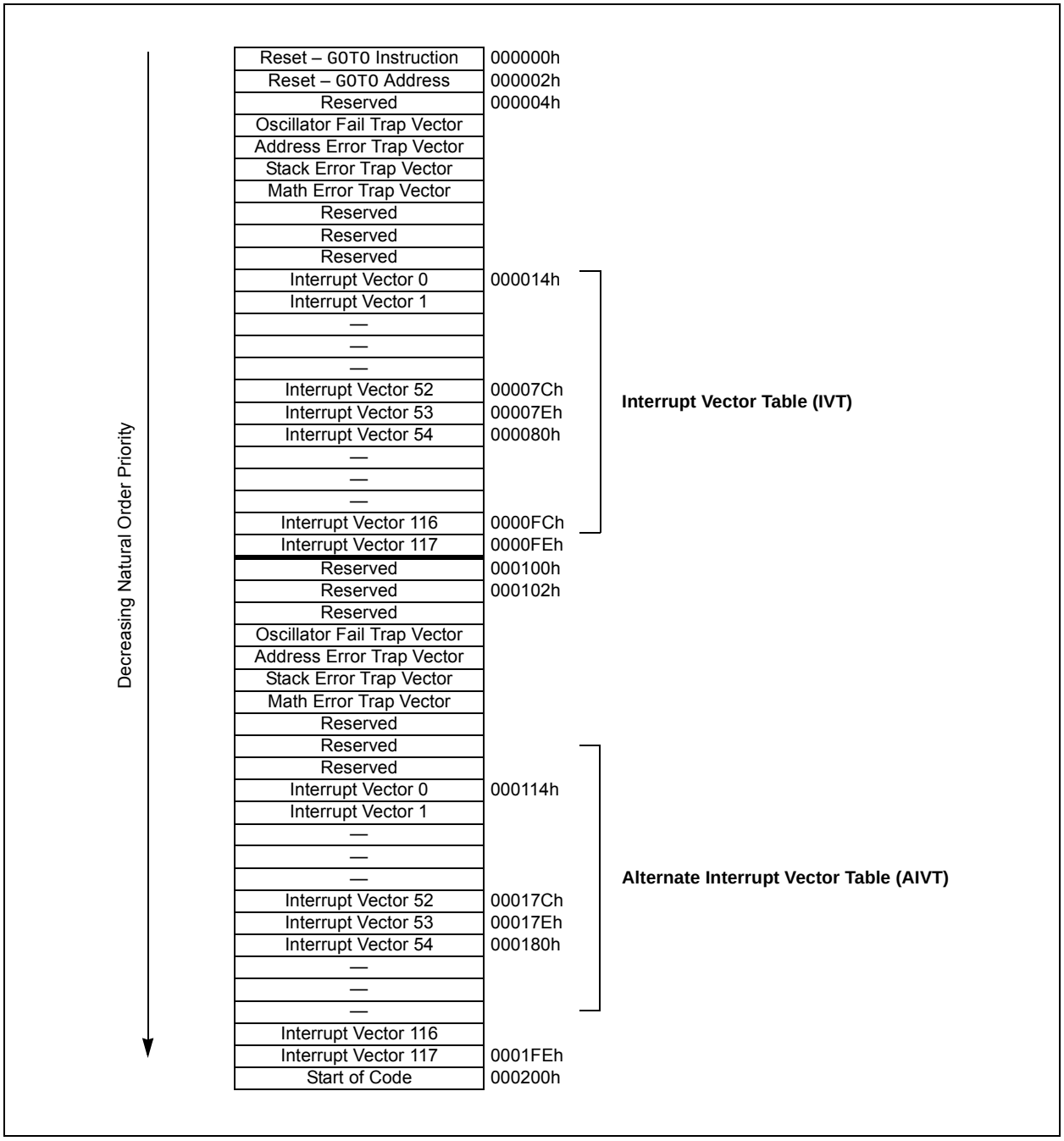
7.4.4 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

Note:	BOR levels differ depending on device type; PIC24FV16KM204 devices are at different levels than those of PIC24F16KM204 devices. See **Section 27.0 "Electrical Characteristics"** for BOR voltage levels.

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



REGISTER 8-23: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	BCL1IP2	BCL1IP1	BCL1IP0	—	SSP1IP2	SSP1IP1	SSP1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **BCL1IP<2:0>:** MSSP1 I^2C™ Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SSP1IP<2:0>:** MSSP1 SPI/I^2C Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

9.0 OSCILLATOR CONFIGURATION

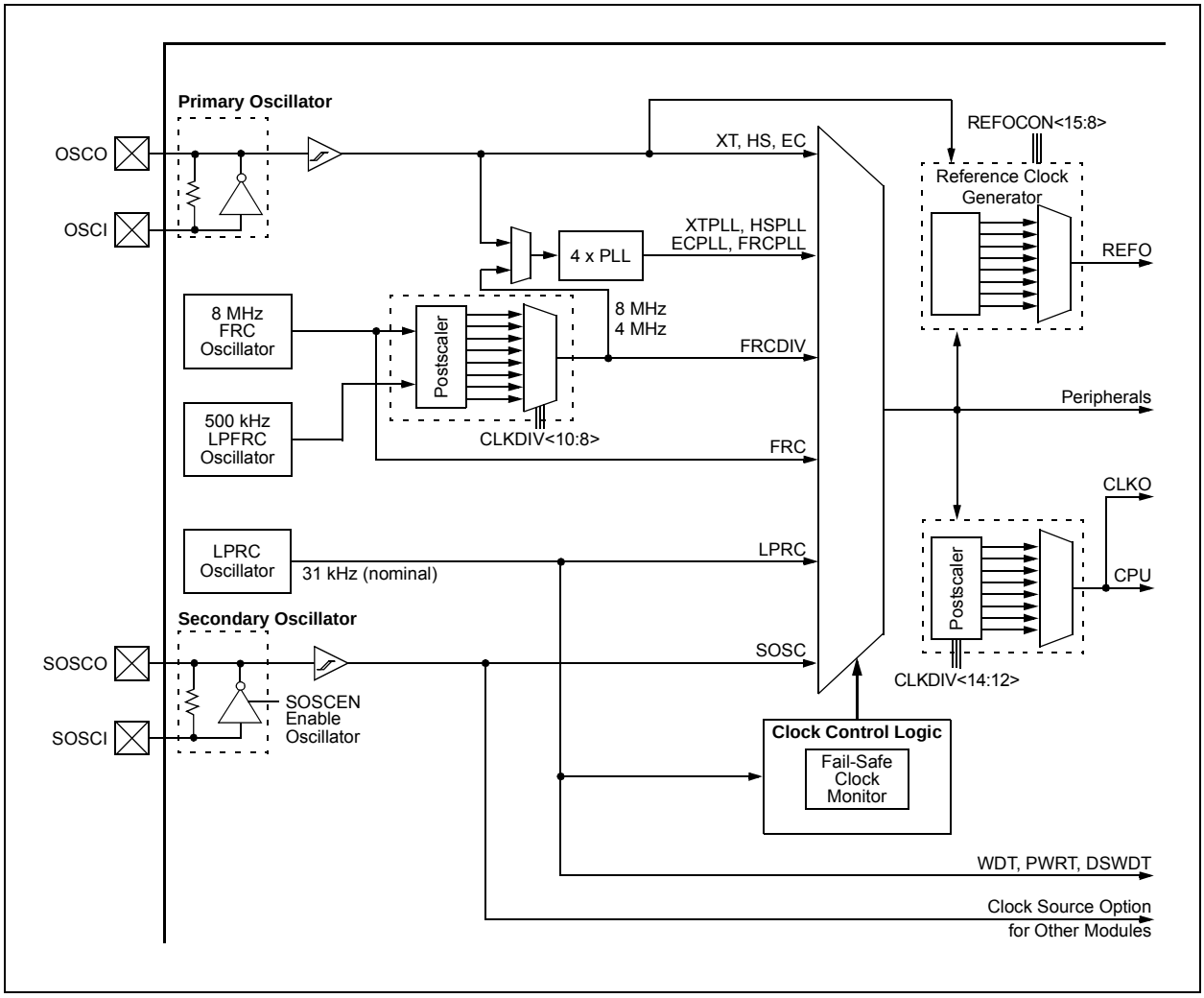
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on oscillator configuration, refer to the *"PIC24F Family Reference Manual"*, **"Oscillator with 500 kHz Low-Power FRC"** (DS39726).

The oscillator system for the PIC24FV16KM204 family of devices has the following features:

- A total of five external and internal oscillator options as clock sources, providing 11 different clock modes.
- On-chip 4x Phase Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources.
- Software-controllable switching between various clock sources.
- Software-controllable postscaler for selective clocking of CPU for system power savings.
- System frequency range declaration bits for External Clock (EC) mode. When using an EC source, the current consumption is reduced by setting the declaration bits to the expected frequency range.
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown.

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: PIC24FXXXXX FAMILY CLOCK DIAGRAM



REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference Oscillator is enabled on the REFO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep
0 = Reference Oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Primary Oscillator is used as the base clock(1)
0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits
1111 = Base clock value divided by 32,768
1110 = Base clock value divided by 16,384
1101 = Base clock value divided by 8,192
1100 = Base clock value divided by 4,096
1011 = Base clock value divided by 2,048
1010 = Base clock value divided by 1,024
1001 = Base clock value divided by 512
1000 = Base clock value divided by 256
0111 = Base clock value divided by 128
0110 = Base clock value divided by 64
0101 = Base clock value divided by 32
0100 = Base clock value divided by 16
0011 = Base clock value divided by 8
0010 = Base clock value divided by 4
0001 = Base clock value divided by 2
0000 = Base clock value

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

NOTES:

REGISTER 13-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS (1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT5	DT4	DT3	DT2	DT1	DT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

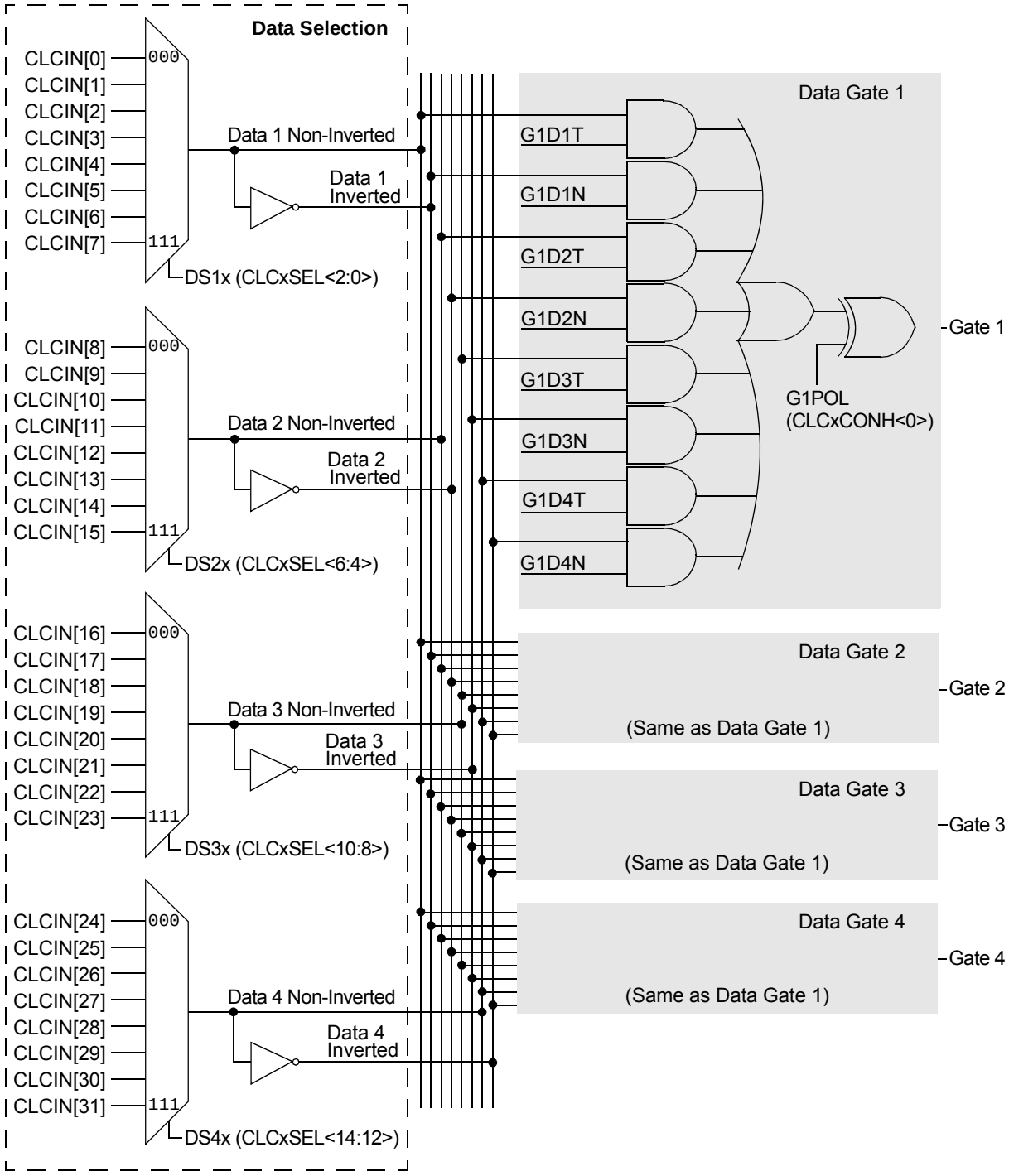
bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DT<5:0>:** CCPx Dead-Time Select bits

111111 = Insert 63 dead-time delay periods between complementary output signals
111110 = Insert 62 dead-time delay periods between complementary output signals
. . .
000010 = Insert 2 dead-time delay periods between complementary output signals
000001 = Insert 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in MCCPx modules only.

FIGURE 17-3: CLCx INPUT SOURCE SELECTION DIAGRAM



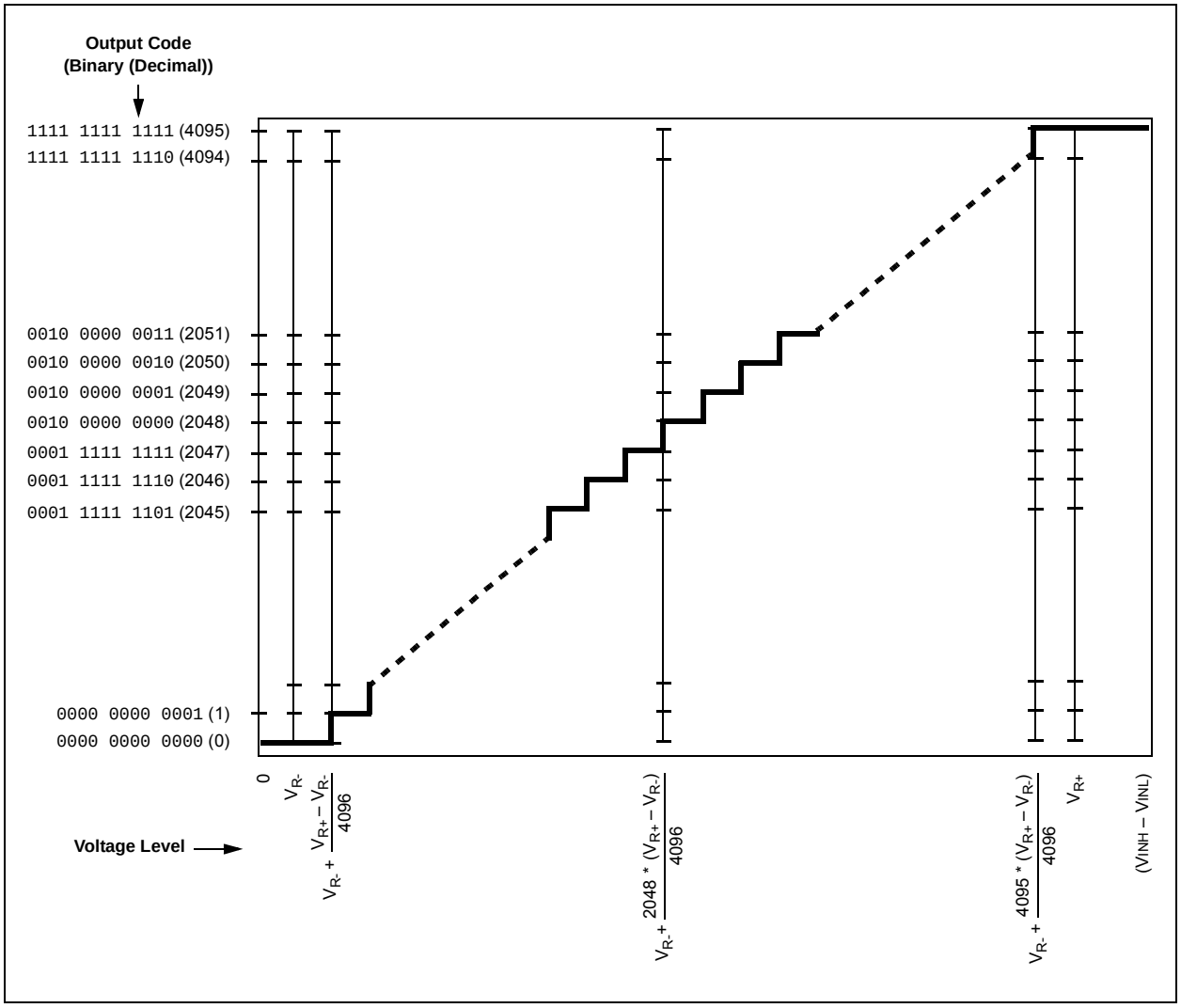
Note: All controls are undefined at power-up.

19.3 Transfer Function

The transfer functions of the A/D Converter in 12-bit resolution are shown in Figure 19-3. The difference of the input voltages ($V_{INH} - V_{INL}$) is compared to the reference ((V_{R+}) – (V_{R-})).

- The first code transition occurs when the input voltage is ((V_{R+}) – (V_{R-}))/4096 or 1.0 LSb.
- The '0000 0000 0001' code is centered at V_{R-} + (1.5 * ((V_{R+}) – (V_{R-}))/4096).
- The '0010 0000 0000' code is centered at V_{REFL} + (2048.5 * ((V_{R+}) – (V_{R-}))/4096).
- An input voltage less than V_{R-} + (((V_{R-}) – (V_{R-}))/4096) converts as '0000 0000 0000'.
- An input voltage greater than (V_{R-}) + (4095 ((V_{R+}) – (V_{R-}))/4096) converts as '1111 1111 1111'.

FIGURE 19-3: 12-BIT A/D TRANSFER FUNCTION



22.0 COMPARATOR MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator module, refer to the *"PIC24F Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734).

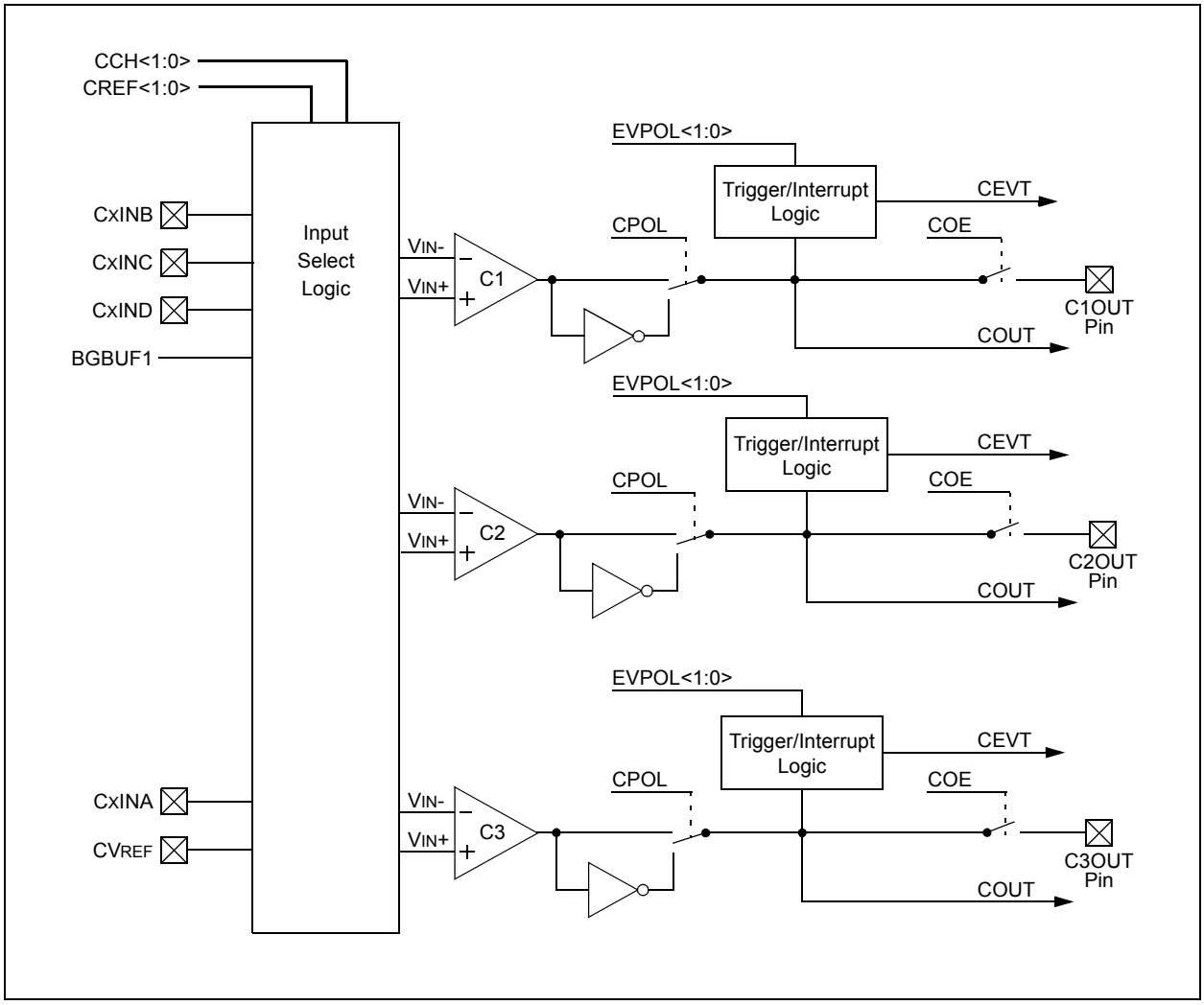
The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as a voltage reference input from either the Internal Band Gap Buffer 1 (BGBUF1) or the comparator voltage reference generator.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 22-1. Diagrams of the possible individual comparator configurations are shown in Figure 22-2.

Each comparator has its own control register, CMxCON (Register 22-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 22-2).

FIGURE 22-1: COMPARATOR x MODULE BLOCK DIAGRAM



REGISTER 25-6: FPOR: RESET CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE(2)	BORV1(3)	BORV0(3)	I2C1SEL(1)	PWRTEN	RETCFG(1)	BOREN1	BOREN0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit(2)
1 = $\overline{\text{MCLR}}$ pin is enabled; RA5 input pin is disabled
0 = RA5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-5 **BORV<1:0>:** Brown-out Reset Enable bits(3)
11 = Brown-out Reset is set to the lowest voltage
10 = Brown-out Reset is set to the middle voltage
01 = Brown-out Reset is set to the highest voltage
00 = Downside protection on POR is enabled – Low-Power BOR (LPBOR) is selected

bit 4 **I2C1SEL:** Alternate I2C1 Pin Mapping bit(1)
1 = Default location for SCL1/SDA1 pins
0 = Alternate location for SCL1/SDA1 pins

bit 3 **PWRTEN:** Power-up Timer Enable bit
1 = PWRT is enabled
0 = PWRT is disabled

bit 2 **RETCFG:** Retention Regulator Configuration bit(1)
1 = Low-voltage regulator is not available
0 = Low-voltage regulator is available and controlled by the RETEN bit (RCON<12>) during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

Note 1: This setting only applies to the "FV" devices. This bit is reserved and should be maintained as '1' on "F" devices.

2: The MCLRE fuse can only be changed when using the VPP-based ICSP™ mode entry. This prevents a user from accidentally locking out the device from the low-voltage test entry.

3: Refer to **Section 27.0 "Electrical Characteristics"** for BOR voltages.

TABLE 27-12: DC CHARACTERISTICS: DATA EEPROM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D140	EPD	Cell Endurance	100,000	—	—	E/W	
D141	VPRD	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D143A	TIWD	Self-Timed Write Cycle Time	—	4	—	ms	
D143B	TREF	Number of Total Write/Erase Cycles Before Refresh	—	10M	—	E/W	
D144	TRETDD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D145	IDDPD	Supply Current During Programming	—	7	—	mA	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

TABLE 27-13: DC CHARACTERISTICS: COMPARATOR

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D300	VIOFF	Input Offset Voltage	—	20	40	mV	
D301	VICM	Input Common-Mode Voltage	0	—	VDD	V	
D302	CMRR	Common-Mode Rejection Ratio	55	—	—	dB	

TABLE 27-14: DC CHARACTERISTICS: COMPARATOR VOLTAGE REFERENCE

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
VRD310	CVRES	Resolution	—	—	VDD/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	1	LSb	AVDD = 3.3V-5.5V
VRD312	CVRUR	Unit Resistor Value (R)	—	2k	—	Ω	

FIGURE 27-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS

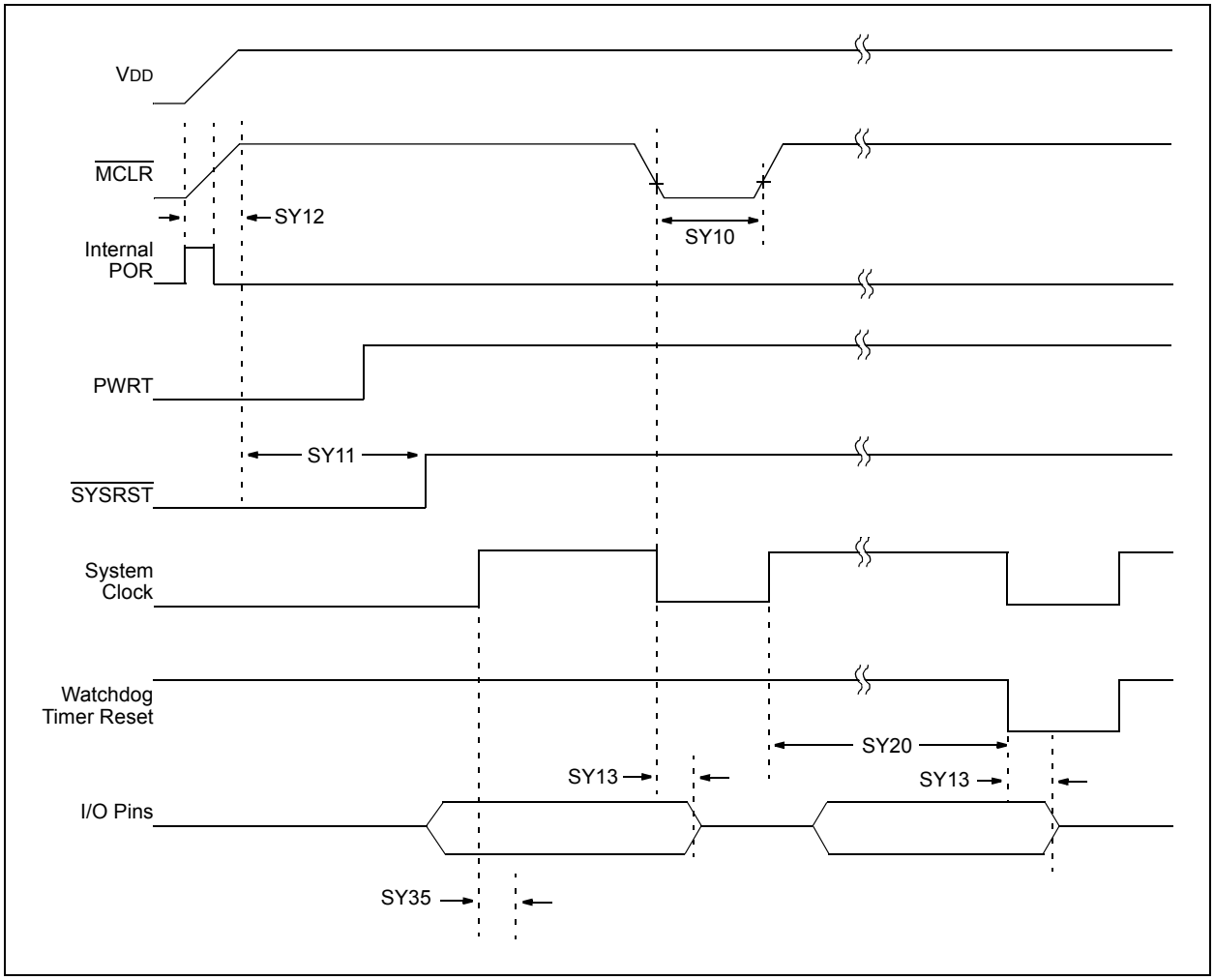
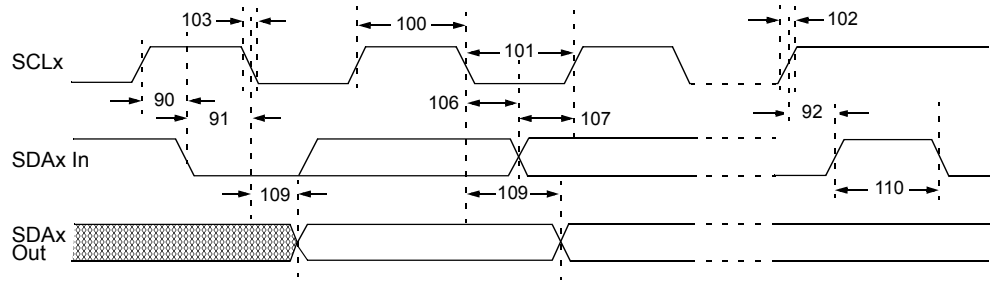


FIGURE 27-18: MSSPx I²C™ BUS DATA TIMING



Note: Refer to Figure 27-5 for load conditions.

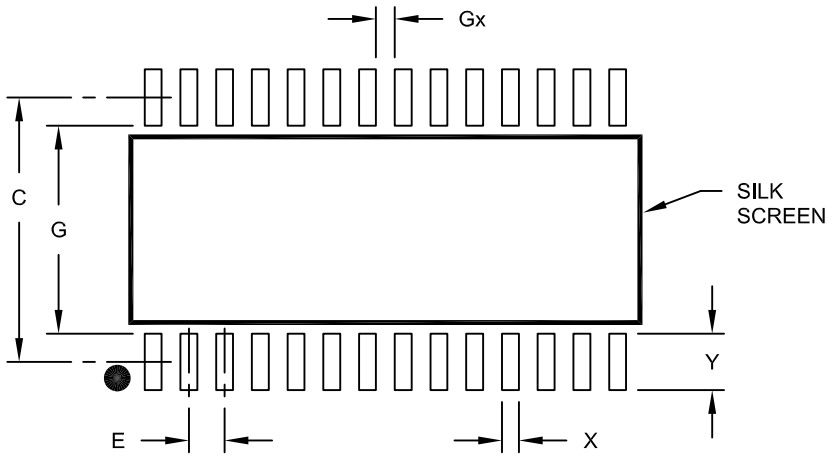
TABLE 27-36: I²C™ BUS DATA REQUIREMENTS (MASTER MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
101	TLOW	Clock Low Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 1)**
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	—	
			400 kHz mode	2(TOSC)(BRG + 1)	—	—	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
D102	CB	Bus Capacitive Loading		—	400	pF	

Note 1: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but Parameter 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, Parameter 102 + Parameter 107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCLx line is released.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

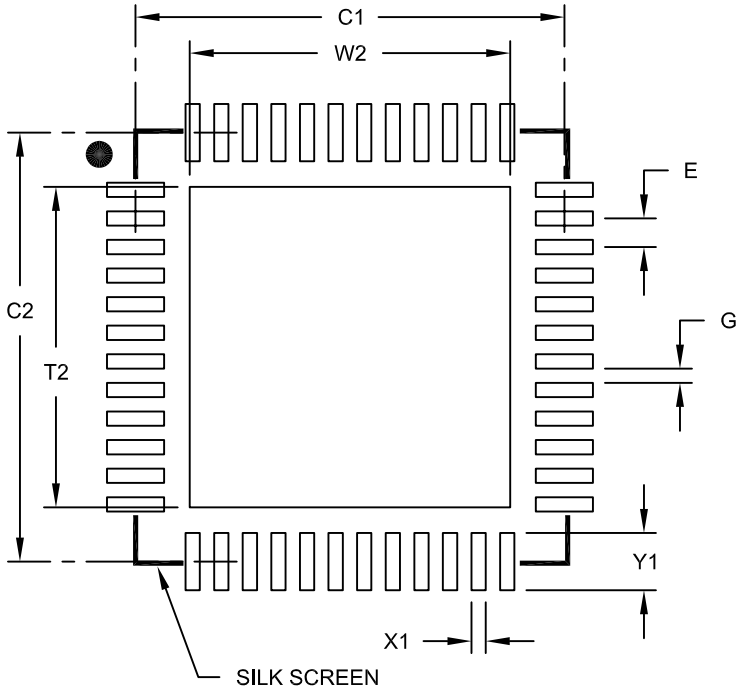
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A