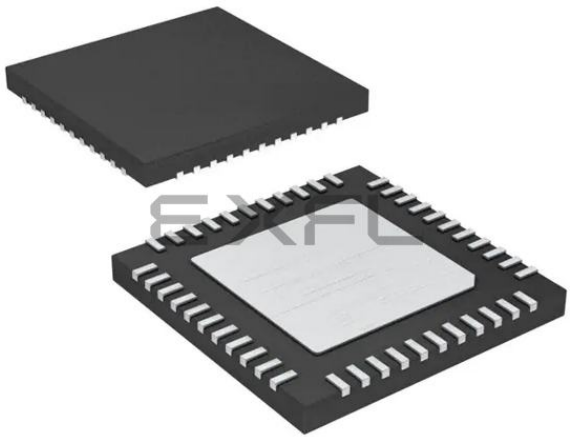

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km204-e-ml

TABLE 1-2: DEVICE FEATURES FOR THE PIC24F16KM104 FAMILY

Features	PIC24F16KM104	PIC24F16KM102	PIC24F08KM102	PIC24F08KM101
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	16K	8K	8K
Program Memory (instructions)	5632	5632	2816	2816
Data Memory (bytes)	1024			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	25 (21/4)			
Voltage Range	1.8-3.6V			
I/O Ports	PORTA<11:0> PORTB<15:0> PORTC<9:0>	PORTA<7:0> PORTB<15:0>		PORTA<6:0> PORTB<15:12,9:7, 4,2:0>
Total I/O Pins	38	24		18
Timers	5 (One 16-bit timer, two MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 1 1			
Serial Communications MSSP UART	 1 1			
Input Change Notification Interrupt	37	23		17
12-Bit Analog-to-Digital Module (input channels)	22	19		16
Analog Comparators	1			
8-Bit Digital-to-Analog Converters	—			
Operational Amplifiers	—			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	—			
Configurable Logic Cell (CLC)	1			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN	28-Pin SPDIP/SSOP/SOIC/QFN		20-Pin SOIC/SSOP/PDIP

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TABLE 4-17: OP AMP 1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
AMP1CON(1)	24Ah	AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—	SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: This registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-18: OP AMP 2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
AMP2CON(1)	24Ch	AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—	SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: This registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-19: DAC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DAC1CON(1)	274h	DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG	DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0	0000
DAC1DAT(1)	276h	DACDAT15(2)	DACDAT14(2)	DACDAT13(2)	DACDAT12(2)	DACDAT11(2)	DACDAT10(2)	DACDAT9(2)	DACDAT8(2)	DACDAT7(2)	DACDAT6(2)	DACDAT5(2)	DACDAT4(2)	DACDAT3(2)	DACDAT2(2)	DACDAT1(2)	DACDAT0(2)	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM1XX devices.
2: The 8-bit result format depends on the value of the DACFM control bit.

TABLE 4-20: DAC2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DAC2CON(1)	278h	DACEN	—	DACSIDL	DACSLP	DACFM	—	SRDIS	DACTRIG	DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0	0000
DAC2DAT(1)	27Ah	DACDAT15(2)	DACDAT14(2)	DACDAT13(2)	DACDAT12(2)	DACDAT11(2)	DACDAT10(2)	DACDAT9(2)	DACDAT8(2)	DACDAT7(2)	DACDAT6(2)	DACDAT5(2)	DACDAT4(2)	DACDAT3(2)	DACDAT2(2)	DACDAT1(2)	DACDAT0(2)	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM2XX devices.
2: The 8-bit result format depends on the value of the DACFM control bit.

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REGISTER 7-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.

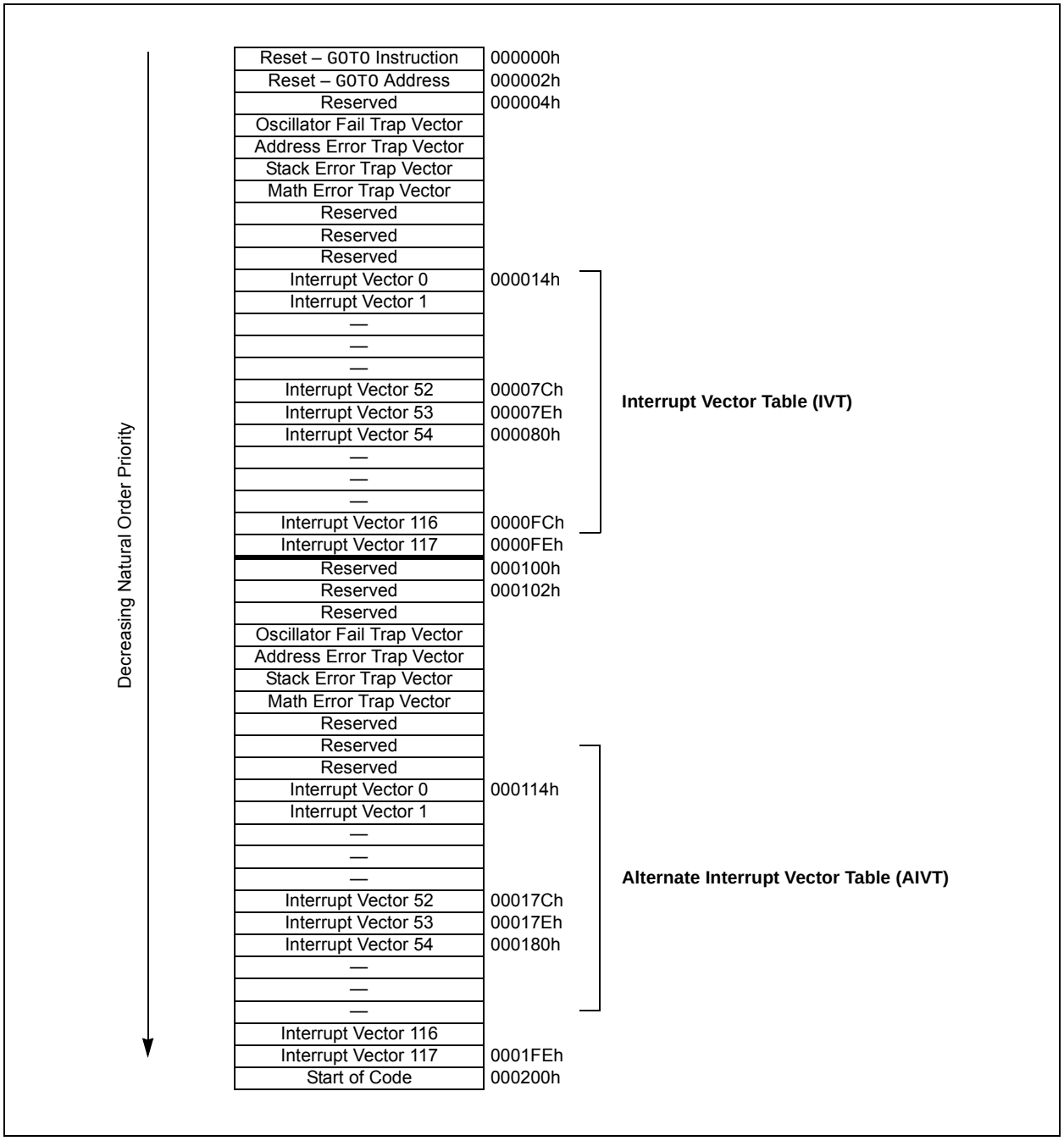
3: This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



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REGISTER 16-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1) (CONTINUED)

bit 7-0 **CAL<7:0>:** RTC Drift Calibration bits

01111111 = Maximum positive adjustment; adds 508 RTC clock pulses every one minute
.
.
.
00000001 = Minimum positive adjustment; adds 4 RTC clock pulses every one minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts 4 RTC clock pulses every one minute
.
.
.
10000000 = Maximum negative adjustment; subtracts 512 RTC clock pulses every one minute

Note 1: The RCFGCAL register is only affected by a POR.

2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

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16.2.5 RTCVAL REGISTER MAPPINGS

REGISTER 16-4: YEAR: YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 16-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

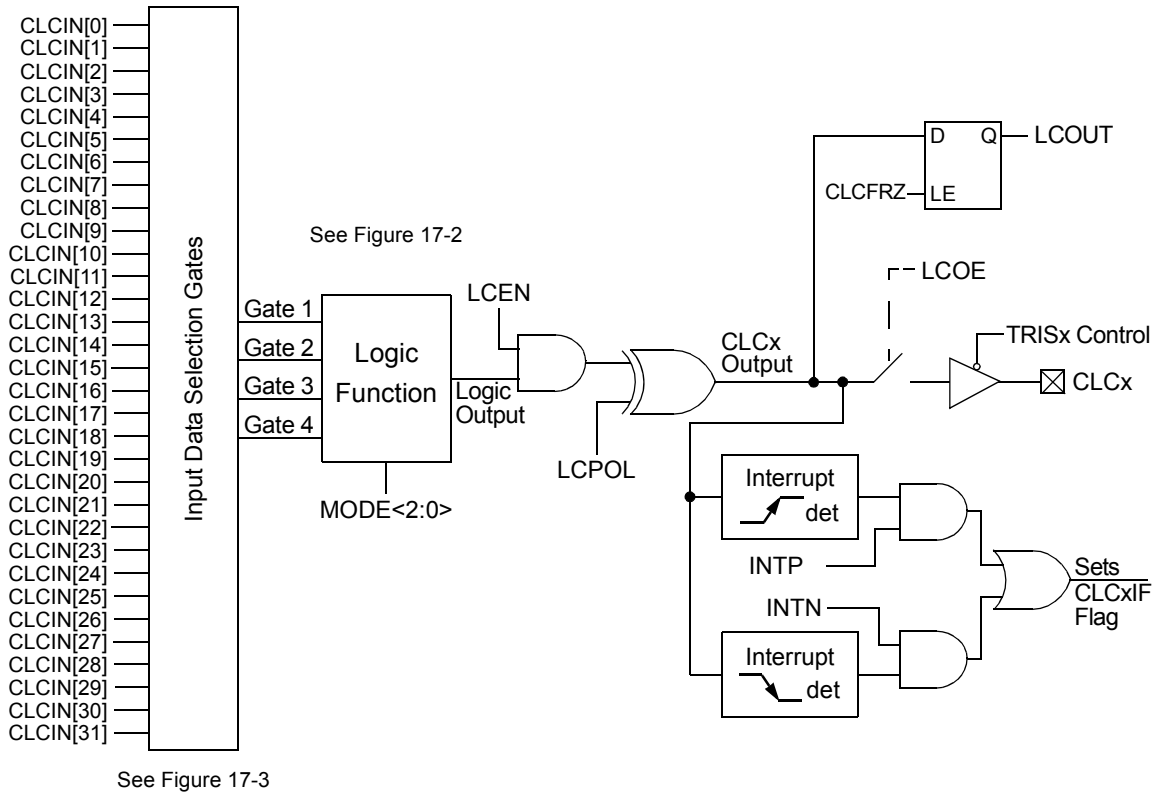
Note 1: A write to this register is only allowed when RTCWREN = 1.

17.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

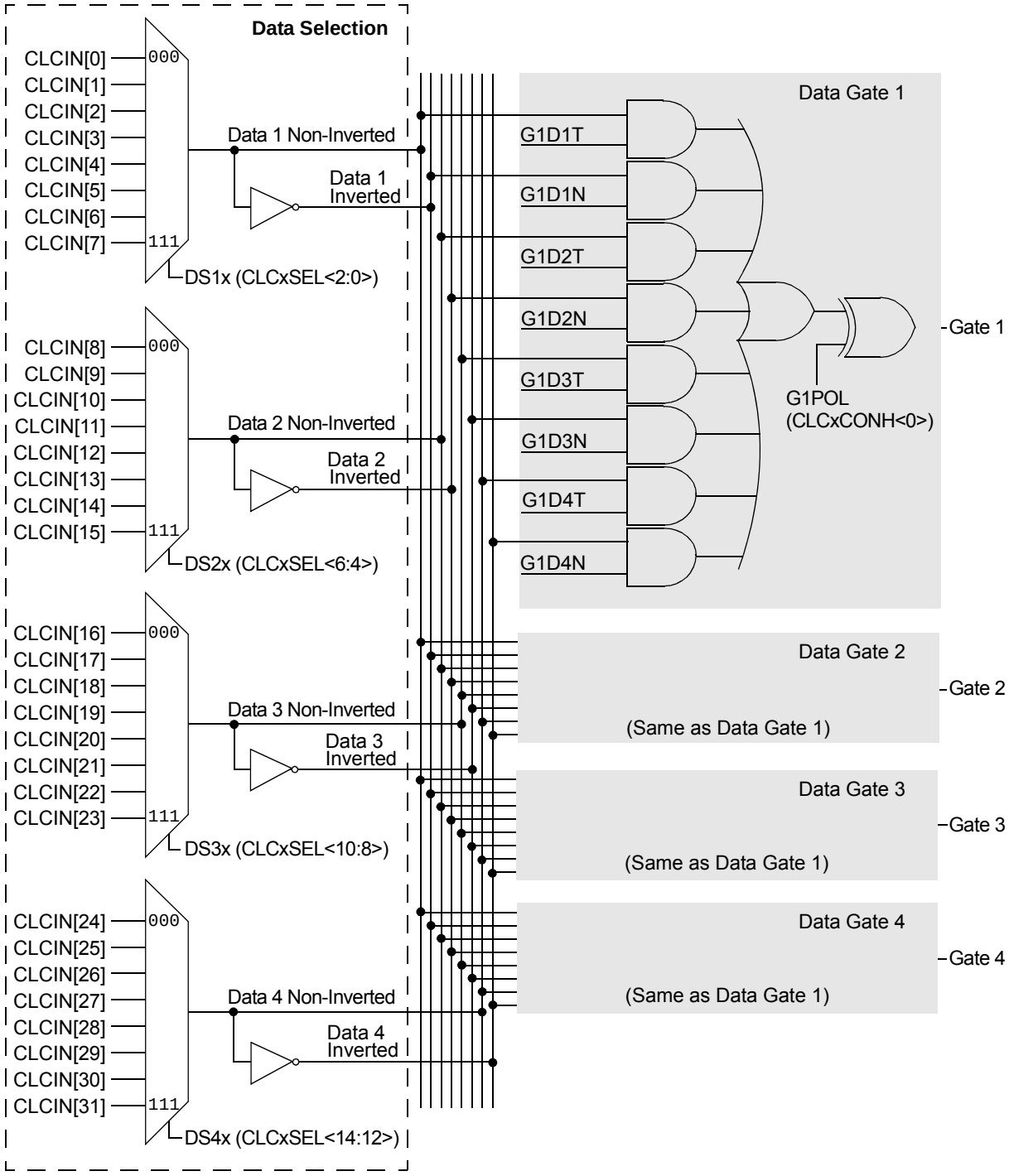
There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 17-1 shows an overview of the module. Figure 17-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 17-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCONL register.

FIGURE 17-3: CLCx INPUT SOURCE SELECTION DIAGRAM



Note: All controls are undefined at power-up.

REGISTER 18-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the internal reference voltage is stable and the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0 = Indicates that the internal reference voltage is unstable and the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Trip Point 1(1)
1101 = Trip Point 2(1)
1100 = Trip Point 3(1)
.
.
.
0000 = Trip Point 15(1)

Note 1: For the actual trip point, see **Section 27.0 "Electrical Characteristics"**.

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REGISTER 21-1: AMPxCON: OP AMP x CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AMPEN:** Op Amp x Control Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **AMPSIDL:** Op Amp x Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **AMPSLP:** Op Amp x Peripheral Enabled in Sleep Mode bit
1 = Continues module operation when device enters Sleep mode
0 = Discontinues module operation in Sleep mode

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **SPDSEL:** Op Amp x Power/Speed Select bit
1 = Higher power and bandwidth (faster response time)
0 = Lower power and bandwidth (slower response time)

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **NINSEL<2:0>:** Negative Op Amp Input Select bits
111 = Reserved; do not use
110 = Reserved; do not use
101 = Op amp negative input is connected to the op amp output (voltage follower)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp negative input is connected to the OAxIND pin
001 = Op amp negative input is connected to the OAxINB pin
000 = Op amp negative input is connected to AVSS

bit 2-0 **PINSEL<2:0>:** Positive Op Amp Input Select bits
111 = Op amp positive input is connected to the output of the A/D input multiplexer
110 = Reserved; do not use
101 = Op amp positive input is connected to the DAC1 output for OA1 (DAC2 output for OA2)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp positive input is connected to the OAxINC pin
001 = Op amp positive input is connected to the OAxINA pin
000 = Op amp positive input is connected to AVSS

Note 1: This register is available only on PIC24F(V)16KM2XX devices.

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REGISTER 23-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = CVREF circuit is powered on
0 = CVREF circuit is powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit
1 = CVREF voltage level is output on the CVREF pin
0 = CVREF voltage level is disconnected from the CVREF pin

bit 5 **CVRSS:** Comparator VREF Source Selection bit
1 = Comparator reference source, CVRSRC = VREF+ – VREF-
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 4-0 **CVR<4:0>:** Comparator VREF Value Selection 0 ≤ CVR<4:0> ≤ 31 bits
When CVRSS = 1:
CVREF = (VREF-) + (CVR<4:0>/32) • (VREF+ – VREF-)
When CVRSS = 0:
CVREF = (AVSS) + (CVR<4:0>/32) • (AVDD – AVSS)

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27.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV16KM204 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV16KM204 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

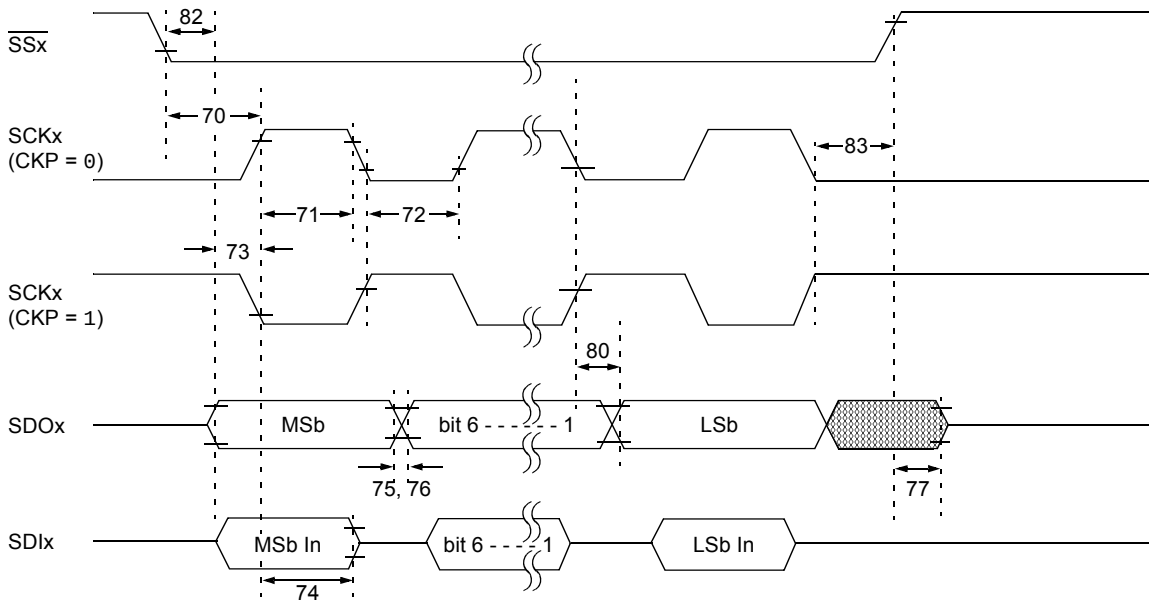
Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} (PIC24FXXKMXXX) ..... -0.3V to +4.5V
Voltage on V_{DD} with respect to V_{SS} (PIC24FVXXKMXXX) ..... -0.3V to +6.5V
Voltage on any combined analog and digital pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any digital only pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on $\overline{MCLR}/V_{PP}$ pin with respect to V_{SS} ..... -0.3V to +9.0V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin(1) ..... 250 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(1) ..... 200 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 27-1).

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 27-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-32: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 Tcy	—	ns	
70A	TssL2WB	$\overline{SSx}$ to Write to SSPxBUF		3 Tcy	—	ns	
71	TscH	SCKx Input High Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
71A			Single Byte	40	—	ns	**(Note 1)**
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	—	ns	**(Note 1)**
73A	Tb2b	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 Tcy + 40	—	ns	**(Note 2)**
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time		—	25	ns	
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
82	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ ↓ Edge		—	50	ns	
83	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge		1.5 Tcy + 40	—	ns	
	Fsck	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

TABLE 27-39: 8-BIT DIGITAL-TO-ANALOG CONVERTER SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Comments**
		Resolution	8	—	—	bits	
		DACREF<1:0> Input Voltage Range	AVSS + 1.8	—	AVDD	V	
		Differential Linearity Error (DNL)	—	—	±0.5	LSb	
		Integral Linearity Error (INL)	—	—	±1.5	LSb	
		Offset Error	—	—	±0.5	LSb	
		Gain Error	—	—	±3.0	LSb	
		Monotonicity	—	—	—	—	**(Note 1)**
		Output Voltage Range	AVSS + 50	AVSS + 5 to AVDD – 5	AVDD – 50	mV	0.5V input overdrive, no output loading
		Slew Rate	—	5	—	V/µs	
		Settling Time	—	10	—	µs	

Note 1: DAC output voltage never decreases with an increase in the data code.

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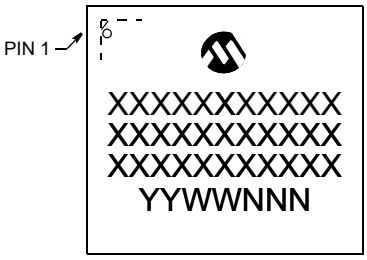
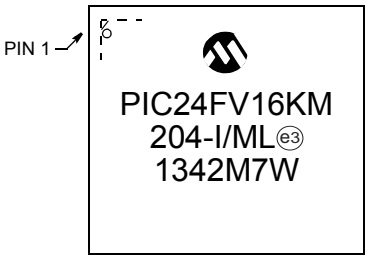
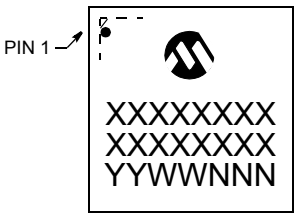
44-Lead QFN (8x8x0.9 mm)



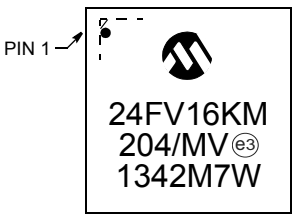
Example



48-Lead UQFN (6x6x0.5 mm)

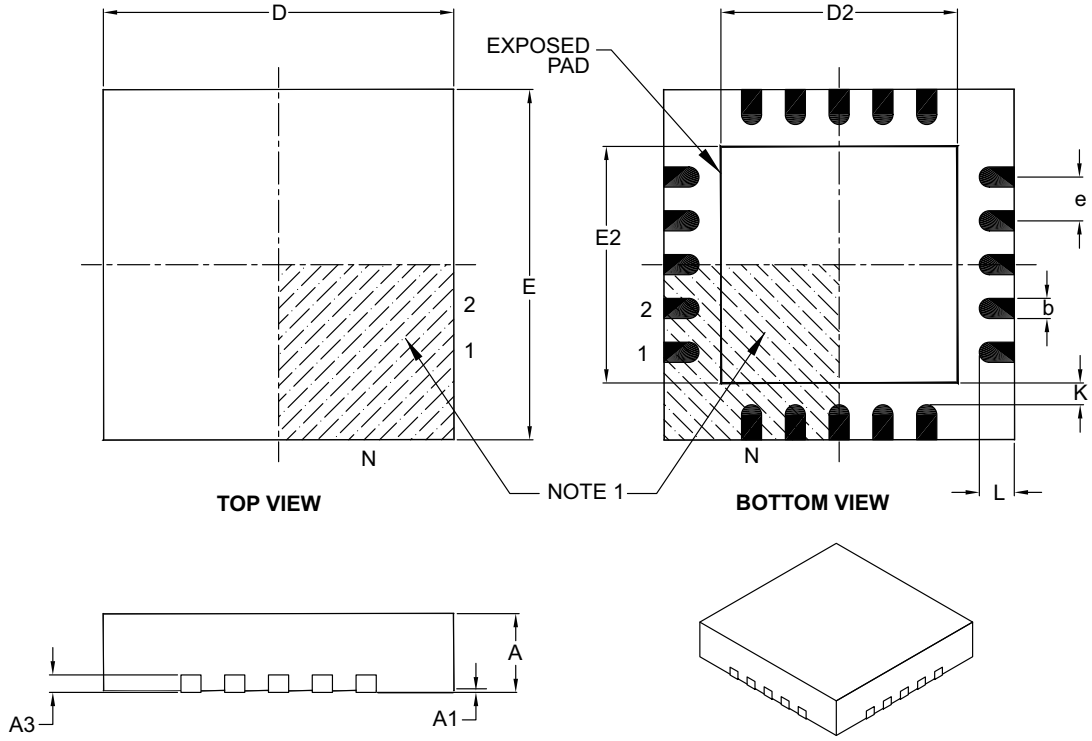


Example



20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

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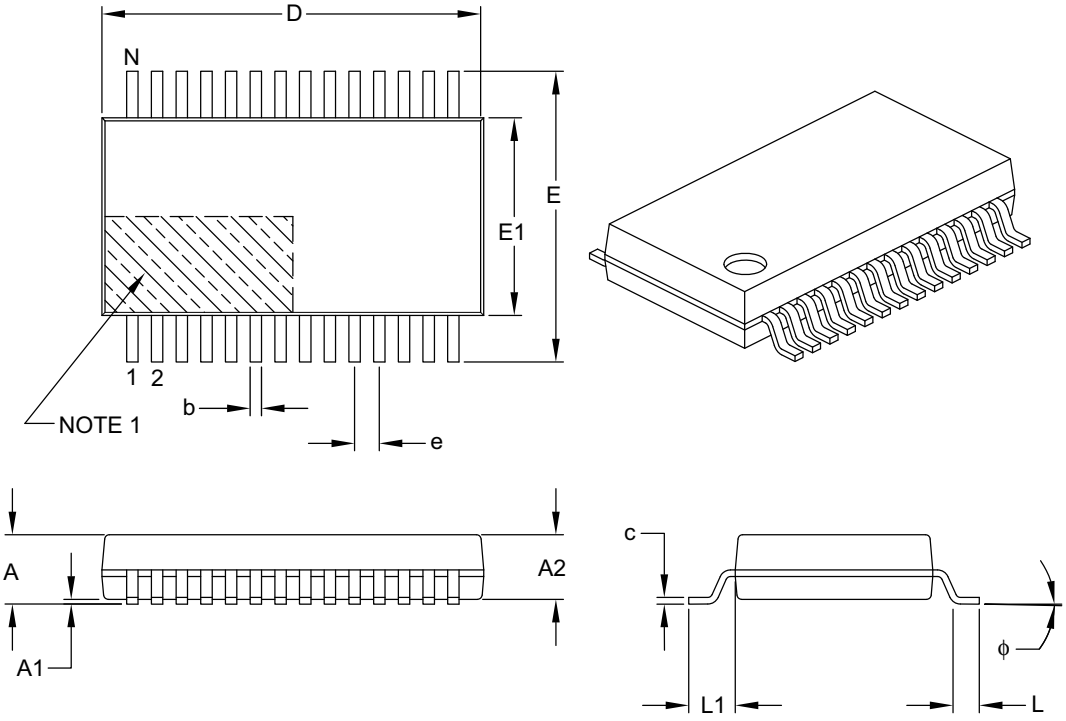
28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

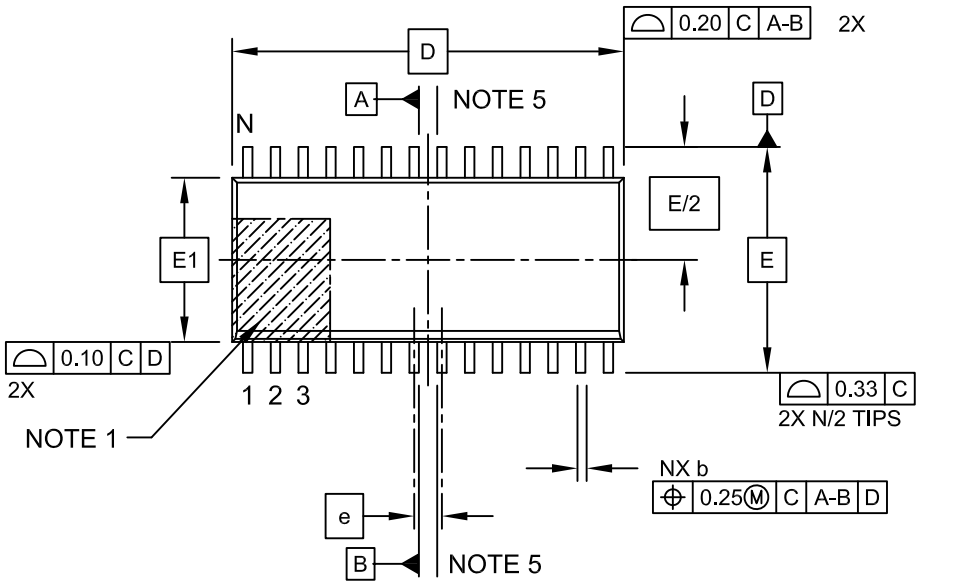
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

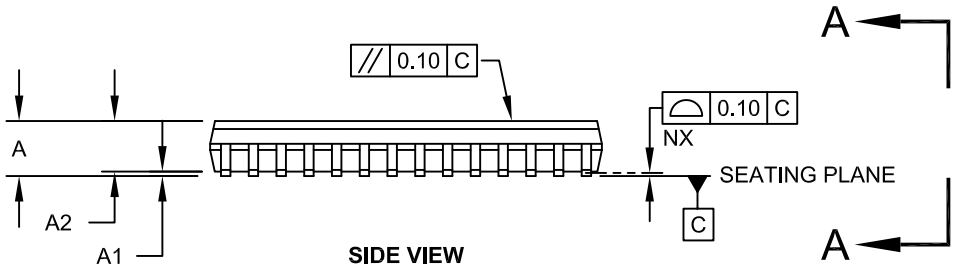
Microchip Technology Drawing C04-073B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

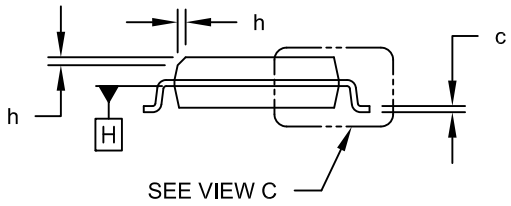
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

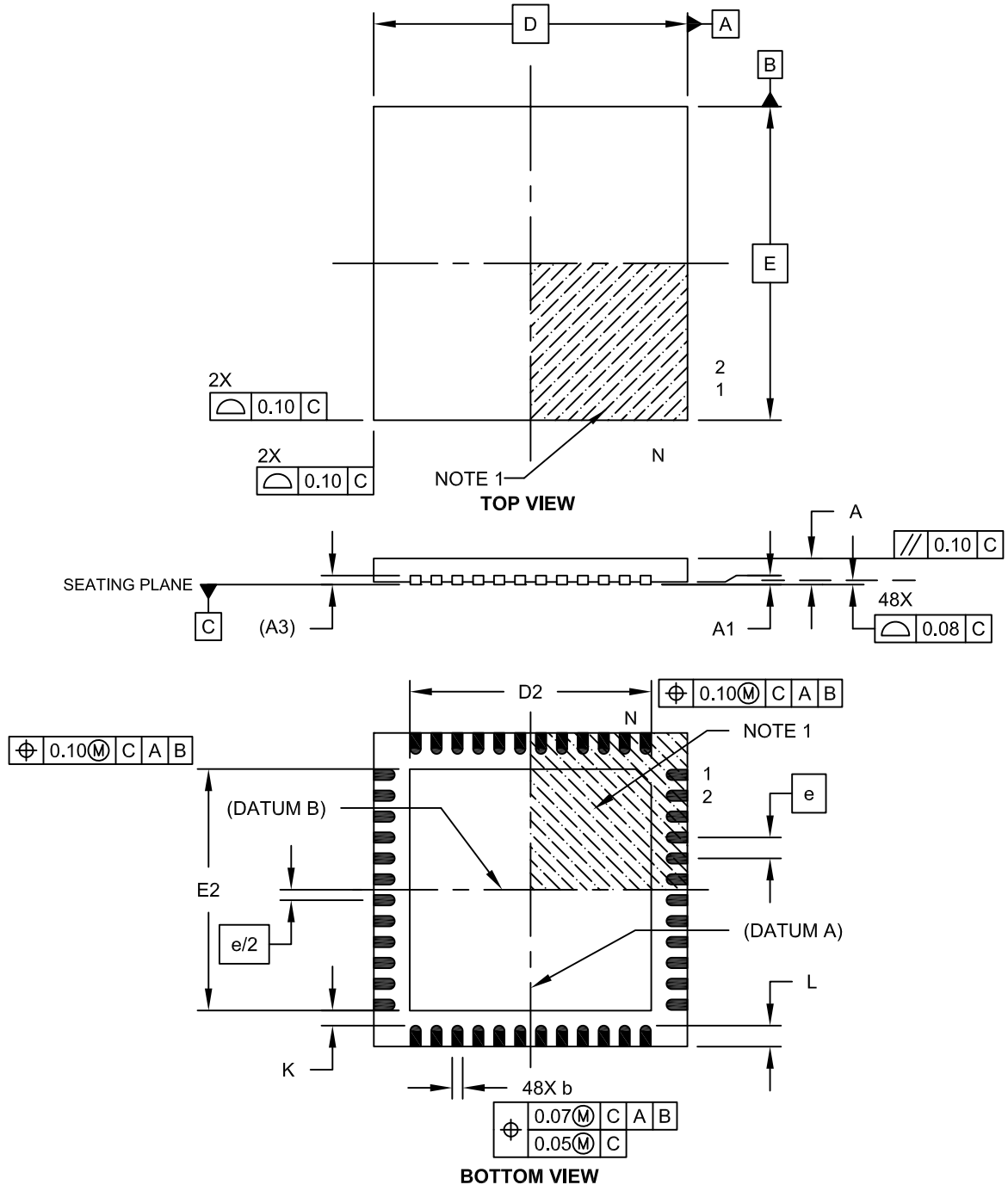


VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-153A Sheet 1 of 2

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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