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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km204-e-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

DETIGETERTOREOTO				
Features	PIC24FV16KM204	PIC24FV08KM204	PIC24FV16KM202	PIC24FV08KM202
Operating Frequency		DC-3	2 MHz	
Program Memory (bytes)	16K	8K	16K	8K
Program Memory (instructions)	5632	2816	5632	2816
Data Memory (bytes)		20)48	
Data EEPROM Memory (bytes)		5	12	
Interrupt Sources (soft vectors/NMI traps)		40 (36/4)	
Voltage Range		2.0-	-5.5V	
I/O Ports	PORTA<1 PORTB< PORTC	1:7,5:0> <15:0> <9:0>	POF POF	RTA<7,5:0> RTB<15:0>
Total I/O Pins	37			23
Timers	(One 16-bit timer, f	, ive MCCPs/SCC	11 Ps with up to tv	vo 16/32 timers each)
Capture/Compare/PWM modules MCCP SCCP			3 2	
Serial Communications MSSP UART			2 2	
Input Change Notification Interrupt	36			22
12-Bit Analog-to-Digital Module (input channels)	22			19
Analog Comparators			3	
8-Bit Digital-to-Analog Converters			2	
Operational Amplifiers			2	
Charge Time Measurement Unit (CTMU)		Y	<i>ï</i> es	
Real-Time Clock and Calendar (RTCC)		Y	es	
Configurable Logic Cell (CLC)			2	
Resets (and delays)	POR, BOR, R REPEAT Instruction	ESET Instruction on, Hardware Tra (PWRT, OS	n, <mark>MCLR</mark> , WDT aps, Configurat T, PLL Lock)	, Illegal Opcode, tion Word Mismatch
Instruction Set	76 Base Inst	ructions, Multiple	e Addressing N	lode Variations
Packages	44-Pin QFI 48-Pin U	N/TQFP, JQFN	SPDIP/S	28-Pin SOP/SOIC/QFN

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FV16KM204 FAMILY

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

			F					FV					
			Pin Numb	er				Pin Numb	er				
Function	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	I/O	Buffer	Description
C1OUT	17	25	22	14	15	17	25	22	14	15	0	_	Comparator 1 Output
C2INA	_	5	2	22	24	_	5	2	22	24	Ι	ANA	Comparator 2 Input A (+)
C2INB	_	4	1	21	23	_	4	1	21	23	Ι	ANA	Comparator 2 Input B (-)
C2INC	_	7	4	24	26	_	7	4	24	26	Ι	ANA	Comparator 2 Input C (+)
C2IND	_	6	3	23	25	_	6	3	23	25	Ι	ANA	Comparator 2 Input D (-)
C2OUT	_	20	17	7	7	_	16	13	43	47	0	_	Comparator 2 Output
C3INA	_	26	23	15	16	_	26	23	15	16	Ι	ANA	Comparator 3 Input A (+)
C3INB	_	25	22	14	15	_	25	22	14	15	Ι	ANA	Comparator 3 Input B (-)
C3INC	_	2	27	19	21	_	2	27	19	21	Ι	ANA	Comparator 3 Input C (+)
C3IND	_	4	1	21	23	_	4	1	21	23	Ι	ANA	Comparator 3 Input D (-)
C3OUT	_	17	14	44	48	_	17	14	44	48	0		Comparator 3 Output
CLC10	13	18	15	1	1	13	18	15	1	1	0	_	CLC 1 Output
CLC2O	—	19	16	6	6	—	19	16	6	6	0	_	CLC 2 Output
CLCINA	9	14	11	41	45	9	14	11	41	45	Ι	ST	CLC External Input A
CLCINB	10	15	12	42	46	10	15	12	42	46	Ι	ST	CLC External Input B
CLKI	7	9	6	30	33	7	9	6	30	33	Ι	ANA	Primary Clock Input
CLKO	8	10	7	31	34	8	10	7	31	34	0	_	System Clock Output
CN0	10	12	9	34	37	10	12	9	34	37	I	ST	Interrupt-on-Change Inputs
CN1	9	11	8	33	36	9	11	8	33	36	I	ST	Interrupt-on-Change Inputs
CN2	2	2	27	19	21	2	2	27	19	21	I	ST	Interrupt-on-Change Inputs
CN3	3	3	28	20	22	3	3	28	20	22	I	ST	Interrupt-on-Change Inputs
CN4	4	4	1	21	23	4	4	1	21	23	I	ST	Interrupt-on-Change Inputs
CN5	5	5	2	22	24	5	5	2	22	24	I	ST	Interrupt-on-Change Inputs
CN6	6	6	3	23	25	6	6	3	23	25	I	ST	Interrupt-on-Change Inputs
CN7	_	7	4	24	26	_	7	4	24	26	I	ST	Interrupt-on-Change Inputs
CN8	14	20	17	7	7	_	_	_	—	_	I	ST	Interrupt-on-Change Inputs
CN9	—	19	16	6	6	—	19	16	6	6	Ι	ST	Interrupt-on-Change Inputs
CN10		—	_	27	29		—	_	27	29	Ι	ST	Interrupt-on-Change Inputs
CN11	18	26	23	15	16	18	26	23	15	16	Ι	ST	Interrupt-on-Change Inputs
CN12	17	25	22	14	15	17	25	22	14	15	1	ST	Interrupt-on-Change Inputs

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C^{TM} = I^2C/SMBus$ input buffer

TABLE 4-8: MCCP1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP1CON1L	140h	CCPON	_	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP1CON1H	142h	OPSSRC	RTRGEN	_	_	OPS3	OPS2	OPS1	OPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP1CON2L	144h	PWMRSEN	ASDGM	_	SSDG	_	_	_	_	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP1CON2H	146h	OENSYNC	_	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	_	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP1CON3L	148h	_	_	_	_	_	_	_	_	_		DT5	DT4	DT3	DT2	DT1	DT0	0000
CCP1CON3H	14Ah	OETRIG	OSCNT2	OSCNT1	OSCNT0	_	OUTM2	OUTM1	OUTM0	_	_	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP1STATL	14Ch	_	_	_	_	_	_	_	_	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP1TMRL	150h							MCC	P1 Time Ba	se Register	Low Word							0000
CCP1TMRH	152h							MCCI	P1 Time Ba	se Register	High Word							0000
CCP1PRL	154h							MCCP1	Time Base I	Period Regis	ster Low Wor	ď						FFFF
CCP1PRH	156h							MCCP1	lime Base F	Period Regis	ster High Wo	rd						FFFF
CCP1RAL	158h							0	utput Comp	are 1 Data \	Nord A							0000
CCP1RBL	15Ch		Output Compare 1 Data Word B 000								0000							
CCP1BUFL	160h		Input Capture 1 Data Buffer Low Word 0000									0000						
CCP1BUFH	162h							Input	Capture 1 [Data Buffer	High Word							0000

Legend: x = unknown, u = unchanged, --- = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access	Program Space Address							
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>			
Instruction Access	User	0 PC<22:1>							
(Code Execution)		0xx xxxx xxxx xxxx xxxx xxx0							
TBLRD/TBLWT	User	TB	LPAG<7:0>	Data EA<15:0>					
(Byte/Word Read/Write)		02	xxx xxxx	xxx		xxx			
	Configuration	TB	LPAG<7:0>	Data EA<15:0>					
		1xxx xxxx		xxxx xxxx xxxx xxxx					
Program Space Visibility	User	0	PSVPAG<7:	:0> ⁽²⁾ Data EA<14:0> ⁽¹⁾					
(Block Remap/Read)		0	XXXX XXX	κx	x				

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

2: PSVPAG can have only two values ('00' to access program memory and FF to access data EEPROM) on the PIC24F16KM family.

FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



REGISTER 8-10: IFS5: INTERRUPT FLAG STATUS REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
—	—	—	—	—	—	—	ULPWUIF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 Unimplemented: Read as '0'

bit 0 ULPWUIF: Ultra Low-Power Wake-up Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

REGISTER 8-11: IFS6: INTERRUPT FLAG STATUS REGISTER 6

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS
—	—	—	—	—	—	CLC2IF	CLC1IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 Unimplemented: Read as '0'

bit 1 CLC2IF: Configurable Logic Cell 2 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

bit 0 CLC1IF: Configurable Logic Cell 1 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

REGISTER 8-14: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	CCT5IE	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 15-10	Unimplemen	ted: Read as '	כי				
hit O		turo/Compore	E Timor Interru	nt Enchla hit			

bit 9	CCT5IE: Capture/Compare 5 Timer Interrupt Enable bit
	1 = Interrupt request is enabled
	0 = Interrupt request is not enabled

bit 8-0 Unimplemented: Read as '0'

REGISTER 8-15: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
_	RTCIE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	BCL2IE	SSP2IE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14	RTCIE: Real-Time Clock and Calendar Interrupt Enable bit
	1 = Interrupt request is enabled0 = Interrupt request is not enabled
bit 13-3	Unimplemented: Read as '0'
bit 2	BCL2IE: MSSP2 I ² C [™] Bus Collision Interrupt Enable bit
	1 = Interrupt request is enabled0 = Interrupt request is not enabled
bit 1	SSP2IE: MSSP2 SPI/I ² C Event Interrupt Enable bit
	1 = Interrupt request is enabled0 = Interrupt request is not enabled
bit 0	Unimplemented: Read as '0'

REGISTER 8-17: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	—			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	—	—	—	—	—	ULPWUIE
bit 7							bit 0
Legend:							

Logona.					
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-1 Unimplemented: Read as '0'

bit 0 ULPWUIE: Ultra Low-Power Wake-up Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

REGISTER 8-18: IEC6: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—		—	—	—	—	—
bit 15 k							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CLC2IE	CLC1IE
bit 7 bi							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 Unimplemented: Read as '0'

bit 1 CLC2IE: Configurable Logic Cell 2 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 0 CLC1IE: Configurable Logic Cell 1 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

REGISTER 10-1: ULPWCON: ULPWU CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0		
ULPEN	_	ULPSIDL		—	—	_	ULPSINK		
bit 15				-			bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—		—	—	—	—		
bit 7							bit 0		
Legend:									
R = Readabl	le bit	W = Writable b	pit	U = Unimplemented bit, read as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		
bit 15	ULPEN: ULF	PWU Module En	able bit						
	1 = Module is	s enabled							
	0 = Module is	s disabled							
bit 14	Unimplemer	nted: Read as '	י)						
bit 13	ULPSIDL: U	LPWU Stop in Id	dle Select bit						
	1 = Discontinues module operation when the device enters Idle mode								
	0 = Continues module operation in Idle mode								
bit 12-9	Unimplemented: Read as '0'								
bit 8	ULPSINK: ULPWU Current Sink Enable bit								
	1 = Current s	sink is enabled							
	0 = Current s	sink is disabled							
bit 7-0	Unimplemented: Read as '0'								

NOTES:

12.0 TIMER1

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on timers, refer to the "PIC24F Family Reference Manual", "Timers" (DS39704).

The Timer1 module is a 16-bit timer which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running, interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation During CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 illustrates a block diagram of the 16-bit Timer1 module.

To configure Timer1 for operation:

- 1. Set the TON bit (= 1).
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
- 5. Load the timer period value into the PR1 register.
- 6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.



SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	MCCP1 or SCCP1 Sync Output
00010	MCCP2 or SCCP2 Sync Output
00011	MCCP3 or SCCP3 Sync Output
00100	MCCP4 or SCCP4 Sync Output
00101	MCCP5 or SCCP5 Sync Output
00110 to 01010	Unused
01011	Timer1 Sync Output ⁽¹⁾
01100 to 10000	Unused
10001	CLC1 Output ⁽¹⁾
10010	CLC2 Output ⁽¹⁾
10011 to 11010	Unused
11011	A/D ⁽¹⁾
11110	Unused
11111	None; Timer with Auto-Rollover (FFFFh \rightarrow 0000h)

TABLE 13-6: SYNCHRONIZATION SOURCES

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	ADDEN: Address Character Detect bit (bit 8 of received data = 1)					
	 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled 					
bit 4	RIDLE: Receiver Idle bit (read-only)					
	1 = Receiver is Idle0 = Receiver is active					
bit 3	PERR: Parity Error Status bit (read-only)					
	 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected 					
bit 2	FERR: Framing Error Status bit (read-only)					
	 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected 					
bit 1	OERR: Receive Buffer Overrun Error Status bit (clear/read-only)					
	1 = Receive buffer has overflowed					
	0 = Receive buffer has not overflowed (clearing a previously set OERR bit ($1 \rightarrow 0$ transition) will reset the receiver buffer and the RSR to the empty state)					
bit 0	URXDA: UARTx Receive Buffer Data Available bit (read-only)					
	 1 = Receive buffer has data; at least one more characters can be read 0 = Receive buffer is empty 					

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REGISTER 16-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾ (CONTINUED)

- **Note 1:** The RCFGCAL register is only affected by a POR.
 - 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
 - 3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.



R/W-0	R-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADRC	EXTSAM	r	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	
bit 15		-				•	bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	
bit 7							bit 0	
Legend:		r = Reserved	bit					
R = Readable	e bit	W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 14 bit 13 bit 12-8	ADRC: A/D Conversion Clock Source bit 1 = RC clock 0 = Clock is derived from the system clock EXTSAM: Extended Sampling Time bit 1 = A/D is still sampling after SAMP = 0 0 = A/D is finished sampling Reserved: Maintain as '0' SAMC<4:0>: Auto-Sample Time Select bits 11111 = 31 TAD							
bit 7-0	00000 = 0 TA ADCS<7:0>: 11111111-01 00111111 = 0	AD A/D Conversion 1000000 = Res 64 * TCY = TAD 2 * TCY = TAD TCY = TAD	n Clock Select served	bits				

REGISTER 19-3: AD1CON3: A/D CONTROL REGISTER 3

26.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

26.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

26.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

26.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

26.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions	
100	Тнідн	Clock High Time	100 kHz mode	4.0	—	μS	Must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Must operate at a minimum of 10 MHz	
			MSSPx module	1.5 TCY	—	—		
101	TLOW	Clock Low Time	100 kHz mode	4.7	-	μS	Must operate at a minimum of 1.5 MHz	
			400 kHz mode	1.3	—	μS	Must operate at a minimum of 10 MHz	
			MSSPx module	1.5 TCY	—	—		
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns		
			400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10 to 400 pF	
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns		
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 to 400 pF	
90 T	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μS	Only relevant for Repeated	
			400 kHz mode	0.6	—	μS	Start condition	
91	Thd:sta	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first clock	
			400 kHz mode	0.6	—	μS	pulse is generated	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	_	ns		
			400 kHz mode	0	0.9	μS		
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	(Note 2)	
			400 kHz mode	100	—	ns		
92	Tsu:sto	Stop Condition Setup Time	100 kHz mode	4.7	—	μS		
			400 kHz mode	0.6	—	μS		
109	ΤΑΑ	Output Valid from Clock	100 kHz mode	—	3500	ns	(Note 1)	
			400 kHz mode	—	—	ns		
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free before	
			400 kHz mode	1.3	—	μS	a new transmission can start	
D102	Св	Bus Capacitive Loading		—	400	pF		

TABLE 27-34: I²C[™] BUS DATA REQUIREMENTS (SLAVE MODE)

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode I²C[™] bus device can be used in a Standard mode I²C bus system, but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

AC CHARACTERISTICS			$ \begin{array}{llllllllllllllllllllllllllllllllllll$				PIC24F16KM204) PIC24FV16KM204) ⊦85°C for Industrial ⊦125°C for Extended
Param No.	Sym	Characteristic	Min.	Тур	Max. Units Comments		
		Resolution	8	—	_	bits	
		DACREF<1:0> Input Voltage Range	AVss + 1.8	—	AVDD	V	
		Differential Linearity Error (DNL)	—	—	±0.5	LSb	
		Integral Linearity Error (INL)	—	—	±1.5	LSb	
		Offset Error	—	—	±0.5	LSb	
		Gain Error	—	—	±3.0	LSb	
		Monotonicity	—	—	—		(Note 1)
		Output Voltage Range	AVss + 50	AVss + 5 to AVpp – 5	AVDD - 50	mV	0.5V input overdrive, no output loading
		Slew Rate	—	5	_	V/µs	
		Settling Time	—	10	—	μs	

TABLE 27-39: 8-BIT DIGITAL-TO-ANALOG CONVERTER SPECIFICATIONS

Note 1: DAC output voltage never decreases with an increase in the data code.

