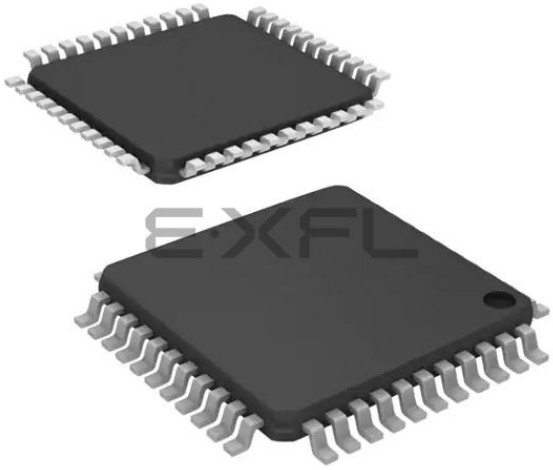
Microchip Technology - PIC24FV08KM204-E/PT Datasheet



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Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (2.75K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv08km204-e-pt

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TABLE 1-4: DEVICE FEATURES FOR THE PIC24FV16KM104 FAMILY

Features	PIC24FV16KM104	PIC24FV16KM102	PIC24FV08KM102	PIC24FV08KM101
Operating Frequency	DC-32 MHz			
Program Memory (bytes)	16K	16K	8K	8K
Program Memory (instructions)	5632	5632	2816	2816
Data Memory (bytes)	1024			
Data EEPROM Memory (bytes)	512			
Interrupt Sources (soft vectors/NMI traps)	25 (21/4)			
Voltage Range	2.0-5.5V			
I/O Ports	PORTA<11:7,5:0> PORTB<15:0> PORTC<9:0>	PORTA<7,5:0> PORTB<15:0>		PORTA<5:0> PORTB<15:12,9:7,4,2:0>
Total I/O Pins	37	23		17
Timers	5 (One 16-bit timer, two MCCPs/SCCPs with up to two 16/32 timers each)			
Capture/Compare/PWM modules MCCP SCCP	 1 1			
Serial Communications MSSP UART	 1 1			
Input Change Notification Interrupt	36	22		16
12-Bit Analog-to-Digital Module (input channels)	22	19		16
Analog Comparators	1			
8-Bit Digital-to-Analog Converters	—			
Operational Amplifiers	—			
Charge Time Measurement Unit (CTMU)	Yes			
Real-Time Clock and Calendar (RTCC)	—			
Configurable Logic Cell (CLC)	1			
Resets (and delays)	POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	44-Pin QFN/TQFP, 48-Pin UQFN	28-Pin SPDIP/SSOP/SOIC/QFN		20-Pin SOIC/SSOP/PDIP

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
$\overline{MCLR}$	1	1	26	18	19	1	1	26	18	19	I	ST	Master Clear (Device Reset) Input (active-low)
OA1INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 1 Input A
OA1INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 1 Input B
OA1INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 1 Input C
OA1IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 1 Input D
OA1OUT	—	7	4	24	26	—	7	4	24	26	O	ANA	Op Amp 1 Analog Output
OA2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Op Amp 2 Input A
OA2INB	—	6	3	23	25	—	6	3	23	25	I	ANA	Op Amp 2 Input B
OA2INC	—	24	21	11	12	—	24	21	11	12	I	ANA	Op Amp 2 Input C
OA2IND	—	25	22	14	15	—	25	22	14	15	I	ANA	Op Amp 2 Input D
OA2OUT	—	26	23	15	16	—	26	23	15	16	O	ANA	Op Amp 2 Analog Output
OC1A	14	20	17	7	7	11	16	13	43	47	O	—	MCCP1 Output Compare A
OC1B	12	17	14	44	48	12	17	14	44	48	O	—	MCCP1 Output Compare B
OC1C	15	21	18	8	9	15	21	18	8	9	O	—	MCCP1 Output Compare C
OC1D	16	24	21	11	12	16	24	21	11	12	O	—	MCCP1 Output Compare D
OC1E	—	14	11	41	45	—	14	11	41	45	O	—	MCCP1 Output Compare E
OC1F	—	15	12	42	46	—	15	12	42	46	O	—	MCCP1 Output Compare F
OC2A	4	22	19	9	10	4	22	19	9	10	O	—	MCCP2 Output Compare A
OC2B	—	23	20	10	11	—	23	20	10	11	O	—	MCCP2 Output Compare B
OC2C	—	—	—	2	2	—	—	—	2	2	O	—	MCCP2 Output Compare C
OC2D	—	—	—	3	3	—	—	—	3	3	O	—	MCCP2 Output Compare D
OC2E	—	—	—	4	4	—	—	—	4	4	O	—	MCCP2 Output Compare E
OC2F	—	—	—	5	5	—	—	—	5	5	O	—	MCCP2 Output Compare F
OC3A	—	21	18	12	13	—	21	18	12	13	O	—	MCCP3 Output Compare A
OC3B	—	24	21	13	14	—	24	21	13	14	O	—	MCCP3 Output Compare B
OC4	—	18	15	1	1	—	18	15	1	1	O	—	SCCP4 Output Compare
OC5	—	19	16	6	6	—	19	16	6	6	O	—	SCCP5 Output Compare
OCFA	17	25	22	14	15	17	25	22	14	15	I	ST	MCCP/SCCP Output Compare Fault Input A
OCFB	16	24	21	32	35	16	24	21	32	35	I	ST	MCCP/SCCP Output Compare Fault Input B

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

TABLE 4-8: MCCP1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP1CON1L	140h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP1CON1H	142h	OPSSRC	RTRGEN	—	—	OPS3	OPS2	OPS1	OPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP1CON2L	144h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP1CON2H	146h	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP1CON3L	148h	—	—	—	—	—	—	—	—	—		DT5	DT4	DT3	DT2	DT1	DT0	0000
CCP1CON3H	14Ah	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP1STATL	14Ch	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP1TMRL	150h	MCCP1 Time Base Register Low Word																0000
CCP1TMRH	152h	MCCP1 Time Base Register High Word																0000
CCP1PRL	154h	MCCP1 Time Base Period Register Low Word																FFFF
CCP1PRH	156h	MCCP1 Time Base Period Register High Word																FFFF
CCP1RAL	158h	Output Compare 1 Data Word A																0000
CCP1RBL	15Ch	Output Compare 1 Data Word B																0000
CCP1BUFL	160h	Input Capture 1 Data Buffer Low Word																0000
CCP1BUFH	162h	Input Capture 1 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-25: A/D REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	300h	A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF1	302h	A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF2	304h	A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF3	306h	A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF4	308h	A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF5	30Ah	A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF6	30Ch	A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF7	30Eh	A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF8	310h	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF9	312h	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF10	314h	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF11	316h	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare																xxxx
ADC1BUF12	318h	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare																xxxx
ADC1BUF13	31Ah	A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare																xxxx
ADC1BUF14	31Ch	A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare																xxxx
ADC1BUF15	31Eh	A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare																xxxx
ADC1BUF16	320h	A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare																xxxx
ADC1BUF17	322h	A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare																xxxx
ADC1BUF18	324h	A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare																xxxx
ADC1BUF19	326h	A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare																xxxx
ADC1BUF20	328h	A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare																xxxx
ADC1BUF21	32Ah	A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare																xxxx
ADC1BUF22	32Ch	A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare																xxxx
ADC1BUF23	32Eh	A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare																xxxx
AD1CON1	340h	ADON	—	ADSIDL	—	—	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	342h	PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	344h	ADRC	EXTSAM	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	348h	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	34Eh	—	CSS30	CSS29	CSS28	CSS27	CSS26	—	—	CSS23	CSS22	CSS21	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16	0000
AD1CSSL	350h	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8(1,2)	CSS7(1,2)	CSS6(1,2)	CSS5(1)	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON5	354h	ASEN	LPEN	CTMREQ	BGREQ	r	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITH	356h	—	—	—	—	—	—	—	—	CHH23	CHH22	CHH21	CHH20(1)	CHH19(1)	CHH18	CHH17	CHH16	0000
AD1CHITL	358h	CHH15	CHH14	CHH13	CHH12	CHH11	CHH10	CHH9	CHH8(1,2)	CHH7(1,2)	CHH6(1,2)	CHH5(1)	CHH4	CHH3	CHH2	CHH1	CHH0	0000
AD1CTMENH	360h	—	—	—	—	—	—	—	—	CTMEN23	CTMEN22	CTMEN21	CTMEN20(1)	CTMEN19(1)	CTMEN18	CTMEN17	CTMEN16	0000
AD1CTMENL	362h	CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8((1,2)	CTMEN7(1,2)	CTMEN6(1,2)	CTMEN5(1)	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are not implemented in 20-pin devices.

2: These bits are not implemented in 28-pin devices.

10.4 Voltage Regulator-Based Power-Saving Features

The PIC24FV16KM204 family series devices have a voltage regulator that has the ability to alter functionality to provide power savings. The on-chip regulator is made up of two basic modules: the Voltage Regulator (VREG) and the Retention Regulator (RETREG). With the combination of VREG and RETREG, the following power modes are available:

10.4.1 RUN MODE

In Run mode, the main VREG is providing a regulated voltage with enough current to supply a device running at full speed and the device is not in Sleep mode. The RETREG may or may not be running, but is unused.

10.4.2 SLEEP MODE

In Sleep mode, the device is in Sleep and the main VREG is providing a regulated voltage to the core. By default, in Sleep mode, the regulator enters a low-power standby state which consumes reduced quiescent current. The PMSLP bit (RCON<8>) controls the regulator state in Sleep mode. If the PMSLP bit is set, the program Flash memory will stay powered on during Sleep mode and the regulator will stay in its full-power mode.

10.4.3 RETENTION REGULATOR

The Retention Regulator, sometimes referred to as the low-voltage regulator, is designed to provide power to the core at a lower voltage than the standard voltage regulator, while consuming significantly lower quiescent current. Refer to **Section 27.0 "Electrical Characteristics"** for the voltage output range of the RETREG. This regulator is only used in Sleep mode, and has limited output current to maintain the RAM and provide power for limited peripherals, such as the WDT, while the device is in Sleep. It is controlled by the RETCFG Configuration bit (FPOR<2>) and in firmware by the RETEN bit (RCON<12>). RETCFG must be programmed (= 0) and the RETEN bit must be set (= 1) for the Retention Regulator to be enabled.

10.4.4 RETENTION SLEEP MODE

In Retention Sleep mode, the device is in Sleep and all regulated voltage is provided solely by the RETREG, while the main VREG is disabled. Consequently, this mode provides the lowest Sleep power consumption, but has a trade-off of a longer wake-up time. The low-voltage Sleep wake-up time is longer than Sleep mode due to the extra time required to re-enable the VREG and raise the V_{DDCORE} supply rail back to normal regulated levels.

Note:	The PIC24F16KM204 family devices do not have any internal voltage regulation, and therefore, do not support Retention Sleep mode.

TABLE 10-1: VOLTAGE REGULATION CONFIGURATION SETTINGS FOR PIC24FXXXXX FAMILY DEVICES

RETCFG Bit (FPOR<2>)	RETEN Bit (RCON<12>	PMSLP Bit (RCON<8>)	Power Mode During Sleep	Description
0	0	1	Sleep	VREG mode (normal) is unchanged during Sleep. RETREG is unused.
0	0	0	Sleep (Standby)	VREG goes to Low-Power Standby mode during Sleep. RETREG is unused.
0	1	0	Retention Sleep	VREG is off during Sleep. RETREG is enabled and provides Sleep voltage regulation.
1	x	1	Sleep	VREG mode (normal) is unchanged during Sleep. RETREG is disabled at all times.
1	x	0	Sleep (Standby)	VREG goes to Low-Power Standby mode during Sleep. RETREG is disabled at all times.

NOTES:

REGISTER 14-1: SSPxSTAT: MSSPx STATUS REGISTER (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE(1)	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **SMP:** Sample bit
SPI Master mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit(1)
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit
Used in I^{2}C™ mode only.

bit 4 **P:** Stop bit
Used in I^{2}C mode only. This bit is cleared when the MSSPx module is disabled; SSPEN bit is cleared.

bit 3 **S:** Start bit
Used in I^{2}C mode only.

bit 2 **R/$\overline{W}$:** Read/$\overline{\text{Write}}$ Information bit
Used in I^{2}C mode only.

bit 1 **UA:** Update Address bit
Used in I^{2}C mode only.

bit 0 **BF:** Buffer Full Status bit
1 = Receive is complete, SSPxBUF is full
0 = Receive is not complete, SSPxBUF is empty

Note 1: Polarity of clock state is set by the CKP bit (SSPxCON1<4>).

REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the empty state)

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data; at least one more characters can be read
0 = Receive buffer is empty

16.3 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value, loaded into the lower half of RCFGCAL, is multiplied by four and will be either added or subtracted from the RTCC timer, once every minute. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute.
3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGCAL register value must be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

   b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGCAL register value must be positive. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

EQUATION 16-1:

(Ideal Frequency† – Measured Frequency) *
60 = Clocks per Minute

† Ideal Frequency = 32,768 Hz

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse, except when SECONDS = 00, 15, 30 or 45. This is due to the auto-adjust of the RTCC at 15 second intervals.

Note:	It is up to the user to include, in the error value, the initial error of the crystal: drift due to temperature and drift due to crystal aging.

16.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>)
- One-time alarm and repeat alarm options are available

16.4.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 16-2, the interval selection of the alarm is configured through the AMASKx bits (ALCFGRPT<13:10>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT<7:0> bits (ALCFGRPT<7:0>). When the value of the ARPTx bits equals 00h and the CHIME bit (ALCFGRPT<14>) is cleared, the repeat function is disabled, and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT<7:0> with FFh.

After each alarm is issued, the value of the ARPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ARPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

16.4.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to other peripherals.

Note:	Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers, and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

REGISTER 17-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS42	DS41	DS40	—	DS32	DS31	DS30
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS22	DS21	DS20	—	DS12	DS11	DS10
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits
111 = MCCP3 Compare Event Flag (CCP3IF)
110 = MCCP1 Compare Event Flag (CCP1IF)
101 = Digital logic low
100 = CTMU Trigger interrupt
For CLC1:
011 = SPI1 SDIx
010 = Comparator 3 output
001 = CLC2 output
000 = CLCINB I/O pin
For CLC2:
011 = SPI2 SDIx
010 = Comparator 3 output
001 = CLC1 output
000 = CLCINB I/O pin

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits
111 = MCCP3 Compare Event Flag (CCP3IF)
110 = MCCP2 Compare Event Flag (CCP2IF)
101 = Digital logic low
For CLC1:
100 = UART1 RX
011 = SPI1 SDOx
010 = Comparator 2 output
001 = CLC1 output
000 = CLCINA I/O pin
For CLC2:
100 = UART2 RX
011 = SPI2 SDOx
010 = Comparator 2 output
001 = CLC2 output
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as '0'

TABLE 27-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated) -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VBG	Band Gap Reference Voltage	0.973	1.024	1.075	V	VDD > 4.5V for 4*VBG reference VDD > 2.3V for 2*VBG reference
	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
	VRGOUT	Regulator Output Voltage	3.1	3.3	3.6	V	
	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Series resistance < 3 Ohm recommended; < 5 Ohm is required.
	VLVR	Low-Voltage Regulator Output Voltage	—	2.6	—	V	

TABLE 27-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204)** **2.0V to 5.5V (PIC24FV16KM204)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**	**Conditions**
	IOUT1	CTMU Current Source, Base Range	—	550	—	nA	CTMUCON1L<1:0> = 01	2.5V < VDD < VDDMAX
	IOUT2	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUCON1L<1:0> = 10	
	IOUT3	CTMU Current Source, 100x Range	—	55	—	μA	CTMUCON1L<1:0> = 11	
	IOUT4	CTMU Current Source, 1000x Range	—	550	—	μA	CTMUCON1L<1:0> = 00 **(Note 2)**	
	VF	Temperature Diode Forward Voltage	—	.76	—	V		
	VΔ	Voltage Change per Degree Celsius	—	1.6	—	mV/°C		

Note 1: Nominal value at the center point of the current trim range (CTMUCON1L<7:2> = 000000). On PIC24F16KM parts, the current output is limited to the typical current value when IOUT4 is chosen.

2: Do not use this current range with a temperature sensing diode.

TABLE 27-17: OPERATIONAL AMPLIFIER SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**
	GBWP	Gain Bandwidth Product	—	5	—	MHz	SPDSEL = 1
			—	0.5	—	MHz	SPDSEL = 0
	SR	Slew Rate	—	1.2	—	V/µs	SPDSEL = 1
			—	0.3	—	V/µs	SPDSEL = 0
	AOL	DC Open-Loop Gain	—	90	—	dB	
	VIOFF	Input Offset Voltage	—	±2	±10	mV	
	VIBC	Input Bias Current	—	—	—	nA	**(Note 1)**
	VICM	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
	CMRR	Common-Mode Rejection Ratio	—	60	—	db	
	PSRR	Power Supply Rejection Ratio	—	60	—	dB	
	VOR	Output Voltage Range	AVSS + 200	AVSS + 5 to AVDD – 5	AVDD – 200	mV	0.5V input overdrive, no output loading

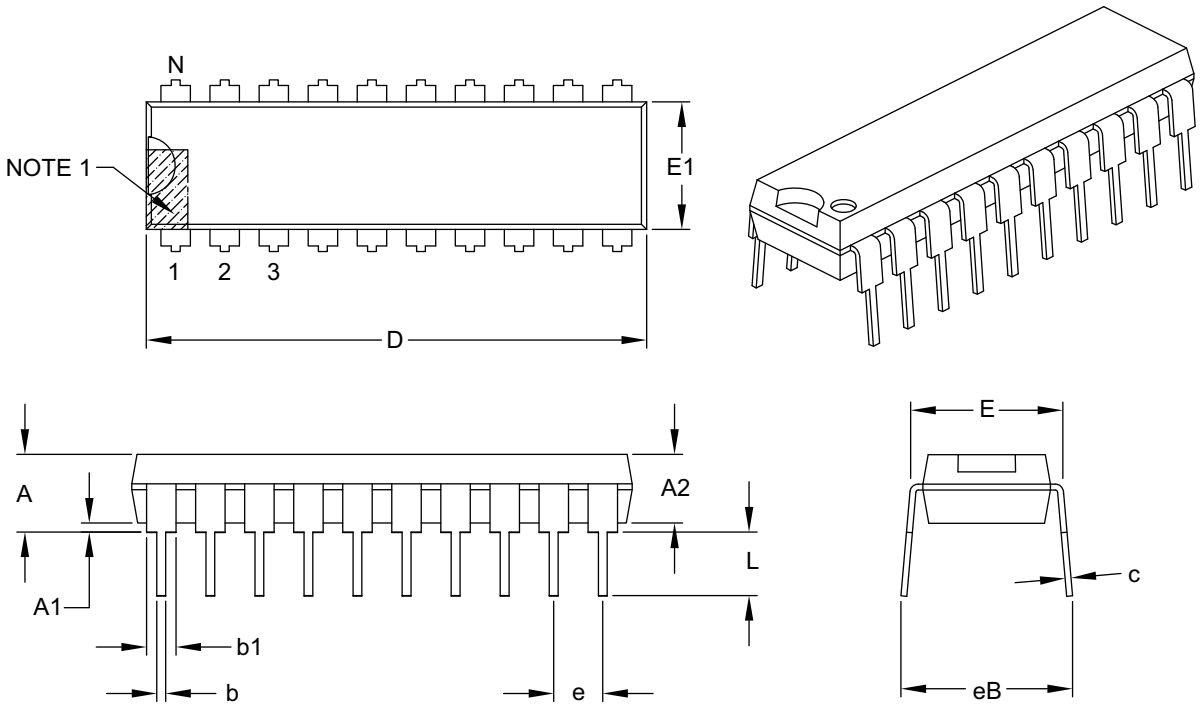
Note 1: The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI50.

28.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

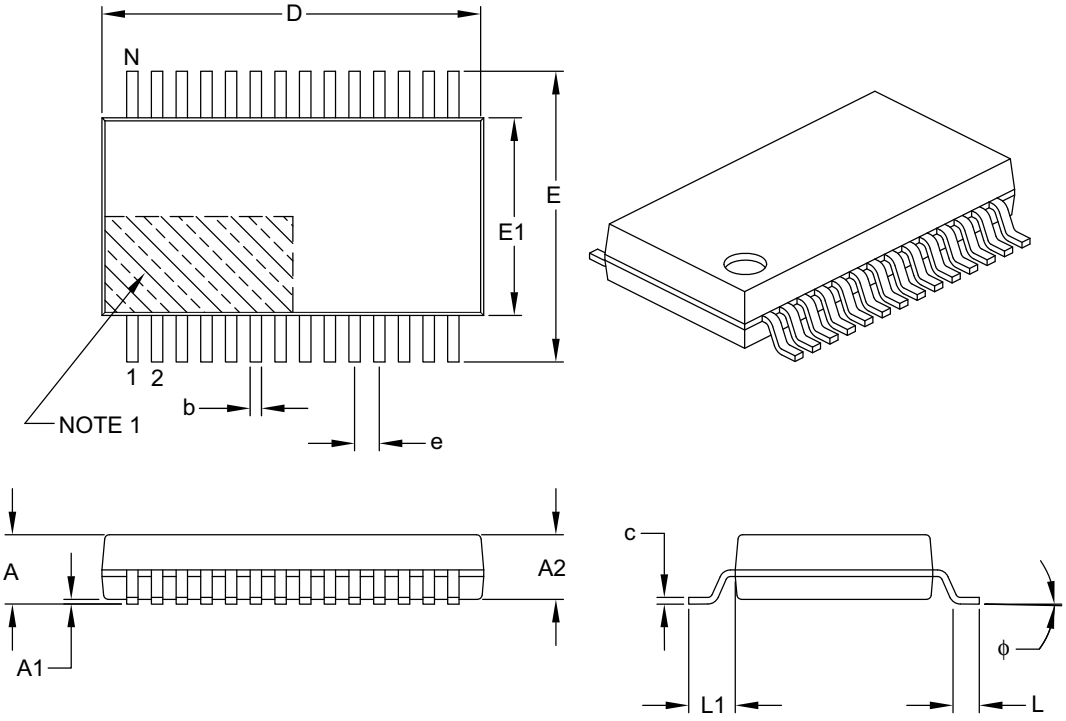
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

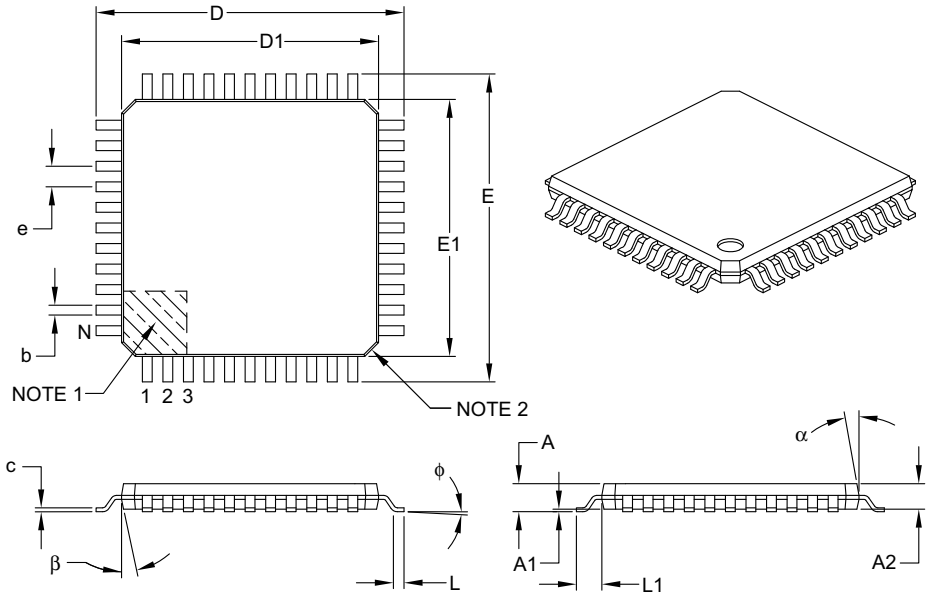
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

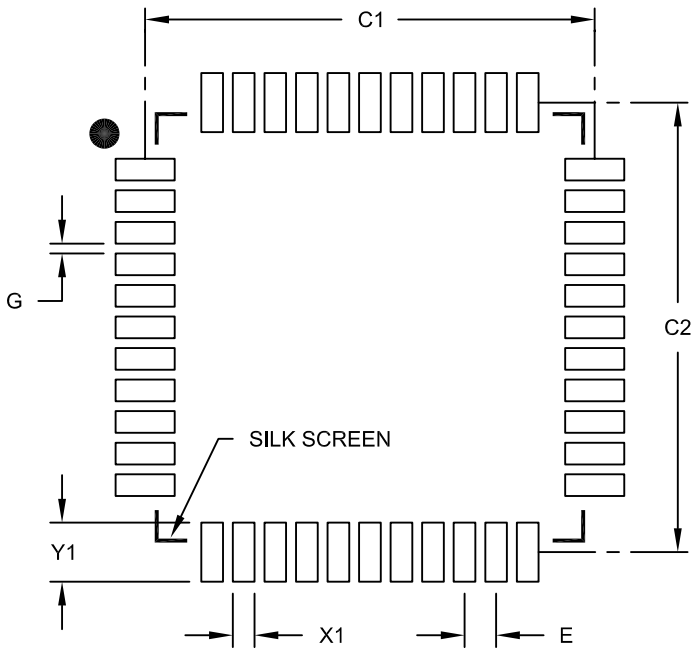
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

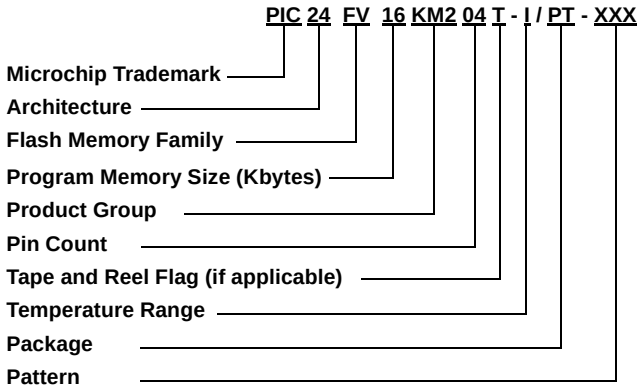
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Standard voltage range Flash program memory
	FV	= Wide voltage range Flash program memory
Product Group	KM2	= General Purpose PIC24F Lite Microcontroller
	KM1	= General Purpose PIC24F Lite Microcontroller with Reduced Feature Set
Pin Count	01	= 20-pin
	02	= 28-pin
	04	= 44-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	SP	= SPDIP
	SO	= SOIC
	SS	= SSOP
	ML	= QFN
	P	= PDIP
	PT	= TQFP
	MV	= UQFN
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample

Examples:

a) PIC24FV16KM204-I/ML: Wide Voltage Range, General Purpose, 16-Kbyte Program Memory, 44-Pin, Industrial Temp., QFN Package

b) PIC24F08KM102-I/SS: Standard Voltage Range, General Purpose with Reduced Feature Set, 8-Kbyte Program Memory, 28-Pin, Industrial Temp., SSOP Package