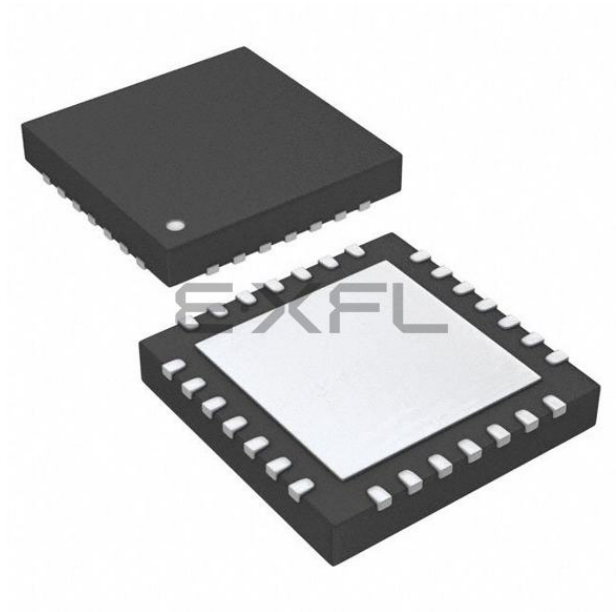
Microchip Technology - PIC24FV16KM102-E/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km102-e-ml

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
C1OUT	17	25	22	14	15	17	25	22	14	15	O	—	Comparator 1 Output
C2INA	—	5	2	22	24	—	5	2	22	24	I	ANA	Comparator 2 Input A (+)
C2INB	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 2 Input B (-)
C2INC	—	7	4	24	26	—	7	4	24	26	I	ANA	Comparator 2 Input C (+)
C2IND	—	6	3	23	25	—	6	3	23	25	I	ANA	Comparator 2 Input D (-)
C2OUT	—	20	17	7	7	—	16	13	43	47	O	—	Comparator 2 Output
C3INA	—	26	23	15	16	—	26	23	15	16	I	ANA	Comparator 3 Input A (+)
C3INB	—	25	22	14	15	—	25	22	14	15	I	ANA	Comparator 3 Input B (-)
C3INC	—	2	27	19	21	—	2	27	19	21	I	ANA	Comparator 3 Input C (+)
C3IND	—	4	1	21	23	—	4	1	21	23	I	ANA	Comparator 3 Input D (-)
C3OUT	—	17	14	44	48	—	17	14	44	48	O	—	Comparator 3 Output
CLC1O	13	18	15	1	1	13	18	15	1	1	O	—	CLC 1 Output
CLC2O	—	19	16	6	6	—	19	16	6	6	O	—	CLC 2 Output
CLCINA	9	14	11	41	45	9	14	11	41	45	I	ST	CLC External Input A
CLCINB	10	15	12	42	46	10	15	12	42	46	I	ST	CLC External Input B
CLKI	7	9	6	30	33	7	9	6	30	33	I	ANA	Primary Clock Input
CLKO	8	10	7	31	34	8	10	7	31	34	O	—	System Clock Output
CN0	10	12	9	34	37	10	12	9	34	37	I	ST	Interrupt-on-Change Inputs
CN1	9	11	8	33	36	9	11	8	33	36	I	ST	Interrupt-on-Change Inputs
CN2	2	2	27	19	21	2	2	27	19	21	I	ST	Interrupt-on-Change Inputs
CN3	3	3	28	20	22	3	3	28	20	22	I	ST	Interrupt-on-Change Inputs
CN4	4	4	1	21	23	4	4	1	21	23	I	ST	Interrupt-on-Change Inputs
CN5	5	5	2	22	24	5	5	2	22	24	I	ST	Interrupt-on-Change Inputs
CN6	6	6	3	23	25	6	6	3	23	25	I	ST	Interrupt-on-Change Inputs
CN7	—	7	4	24	26	—	7	4	24	26	I	ST	Interrupt-on-Change Inputs
CN8	14	20	17	7	7	—	—	—	—	—	I	ST	Interrupt-on-Change Inputs
CN9	—	19	16	6	6	—	19	16	6	6	I	ST	Interrupt-on-Change Inputs
CN10	—	—	—	27	29	—	—	—	27	29	I	ST	Interrupt-on-Change Inputs
CN11	18	26	23	15	16	18	26	23	15	16	I	ST	Interrupt-on-Change Inputs
CN12	17	25	22	14	15	17	25	22	14	15	I	ST	Interrupt-on-Change Inputs

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

TABLE 4-8: MCCP1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP1CON1L	140h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP1CON1H	142h	OPSSRC	RTRGEN	—	—	OPS3	OPS2	OPS1	OPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP1CON2L	144h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP1CON2H	146h	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP1CON3L	148h	—	—	—	—	—	—	—	—	—		DT5	DT4	DT3	DT2	DT1	DT0	0000
CCP1CON3H	14Ah	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP1STATL	14Ch	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP1TMRL	150h	MCCP1 Time Base Register Low Word																0000
CCP1TMRH	152h	MCCP1 Time Base Register High Word																0000
CCP1PRL	154h	MCCP1 Time Base Period Register Low Word																FFFF
CCP1PRH	156h	MCCP1 Time Base Period Register High Word																FFFF
CCP1RAL	158h	Output Compare 1 Data Word A																0000
CCP1RBL	15Ch	Output Compare 1 Data Word B																0000
CCP1BUFL	160h	Input Capture 1 Data Buffer Low Word																0000
CCP1BUFH	162h	Input Capture 1 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-11: SCCP4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP4CON1L(1)	1ACh	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP4CON1H(1)	1AEh	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP4CON2L(1)	1B0h	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP4CON2H(1)	1B2h	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICSEL2	ICSEL1	ICSEL0	0100
CCP4CON3H(1)	1B6h	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	—	—	—	—	—	POLACE	—	PSSACE1	PSSACE0	—	—	0000
CCP4STATL(1)	1B8h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP4TMRL(1)	1BCh	SCCP4 Time Base Register Low Word																0000
CCP4TMRH(1)	1BEh	SCCP4 Time Base Register High Word																0000
CCP4PRL(1)	1C0h	SCCP4 Time Base Period Register Low Word																FFFF
CCP4PRH(1)	1C2h	SCCP4 Time Base Period Register High Word																FFFF
CCP4RAL(1)	1C4h	Output Compare 4 Data Word A																0000
CCP4RBL(1)	1C8h	Output Compare 4 Data Word B																0000
CCP4BUFL(1)	1CCh	Input Capture 4 Data Buffer Low Word																0000
CCP4BUFH(1)	1CEh	Input Capture 4 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

5.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 32 instructions or 96 bytes. RTSP allows the user to erase blocks of 1 row, 2 rows and 4 rows (32, 64 and 128 instructions) at a time, and to program one row at a time. It is also possible to program single words.

The 1-row (96 bytes), 2-row (192 bytes) and 4-row (384 bytes) erase blocks, and single row write block (96 bytes) are edge-aligned, from the beginning of program memory.

When data is written to program memory using TBLWT instructions, the data is not written directly to memory. Instead, data written using Table Writes is stored in holding latches until the programming sequence is executed.

Any number of TBLWT instructions can be executed and a write will be successfully performed. However, 32 TBLWT instructions are required to write the full row of memory.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

Note:	Writing to a location multiple times, without erasing it, is not recommended.

All of the Table Write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

5.3 Enhanced In-Circuit Serial Programming

Enhanced ICSP uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls the blocks that need to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to **Section 5.5 “Programming Operations”** for further details.

5.5 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

6.4.1 ERASE DATA EEPROM

The data EEPROM can be fully erased, or can be partially erased, at three different sizes: one word, four words or eight words. The bits, NVMOP<1:0> (NVMCON<1:0>), decide the number of words to be erased. To erase partially from the data EEPROM, the following sequence must be followed:

1. Configure NVMCON to erase the required number of words: one, four or eight.
2. Load TBLPAG and WREG with the EEPROM address to be erased.
3. Clear the NVMIF status bit and enable the NVM interrupt (optional).
4. Write the key sequence to NVMKEY.
5. Set the WR bit to begin the erase cycle.
6. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical erase sequence is provided in Example 6-2. This example shows how to do a one-word erase. Similarly, a four-word erase and an eight-word erase can be done. This example uses C library procedures to manage the Table Pointer (`builtin_tblpage` and `builtin_tbloffset`) and the Erase Page Pointer (`builtin_tblwtl`). The memory unlock sequence (`builtin_write_NVM`) also sets the WR bit to initiate the operation and returns control when complete.

EXAMPLE 6-2: SINGLE-WORD ERASE

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
/*-----------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the erase
-----------------------------------------------------------------------------------------------
*/
    unsigned int offset;

    // Set up NVMCON to erase one word of data EEPROM
    NVMCON = 0x4058;

    // Set up a pointer to the EEPROM location to be erased
    TBLPAG = __builtin_tblpage(&eeData);            // Initialize EE Data page pointer
    offset = __builtin_tbloffset(&eeData);          // Initizlize lower word of address
    __builtin_tblwtl(offset, 0);                    // Write EEPROM data to write latch

    asm volatile ("disi #5");                       // Disable Interrupts For 5 Instructions
    __builtin_write_NVM();                          // Issue Unlock Sequence & Start Write Cycle
    while(NVMCONbits.WR=1);                         // Optional: Poll WR bit to wait for
                                                    // write sequence to complete
```

REGISTER 8-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0
U2TXIF	U2RXIF	INT2IF	CCT4IF	CCT3IF	—	—	—
bit 15							bit 8

U-0	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
—	CCP5IF	—	INT1IF	CNIF	CMIF	BCL1IF	SSP1IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIF:** UART2 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **U2RXIF:** UART2 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **CCT4IF:** Capture/Compare 4 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **CCT3IF:** Capture/Compare 3 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10-7 **Unimplemented:** Read as '0'

bit 6 **CCP5IF:** Capture/Compare 5 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **Unimplemented:** Read as '0'

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CMIF:** Comparator Interrupt Flag Status Bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **BCL1IF:** MSSP1 I^2C™ Bus Collision Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SI2C1IF:** MSSP1 SPI/I^2C Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

TABLE 13-6: SYNCHRONIZATION SOURCES

SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	MCCP1 or SCCP1 Sync Output
00010	MCCP2 or SCCP2 Sync Output
00011	MCCP3 or SCCP3 Sync Output
00100	MCCP4 or SCCP4 Sync Output
00101	MCCP5 or SCCP5 Sync Output
00110 to 01010	Unused
01011	Timer1 Sync Output(1)
01100 to 10000	Unused
10001	CLC1 Output(1)
10010	CLC2 Output(1)
10011 to 11010	Unused
11011	A/D(1)
11110	Unused
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

REGISTER 13-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output is defined by module operating mode (see Table 13-5)
01 = Time base rollover event (all modes)
00 = Disabled

bit 2-0 **ICS<2:0>:** Input Capture Source Select bits
111 = Unused
110 = CLC2 output
101 = CLC1 output
100 = Unused
011 = Comparator 3 output
010 = Comparator 2 output
001 = Comparator 1 output
000 = Input Capture x (ICx) I/O pin

Note 1: OCFEN through OCBEN (bits<13:9>) are implemented in MCCPx modules only.

15.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the *"PIC24F Family Reference Manual"*, **"UART"** (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

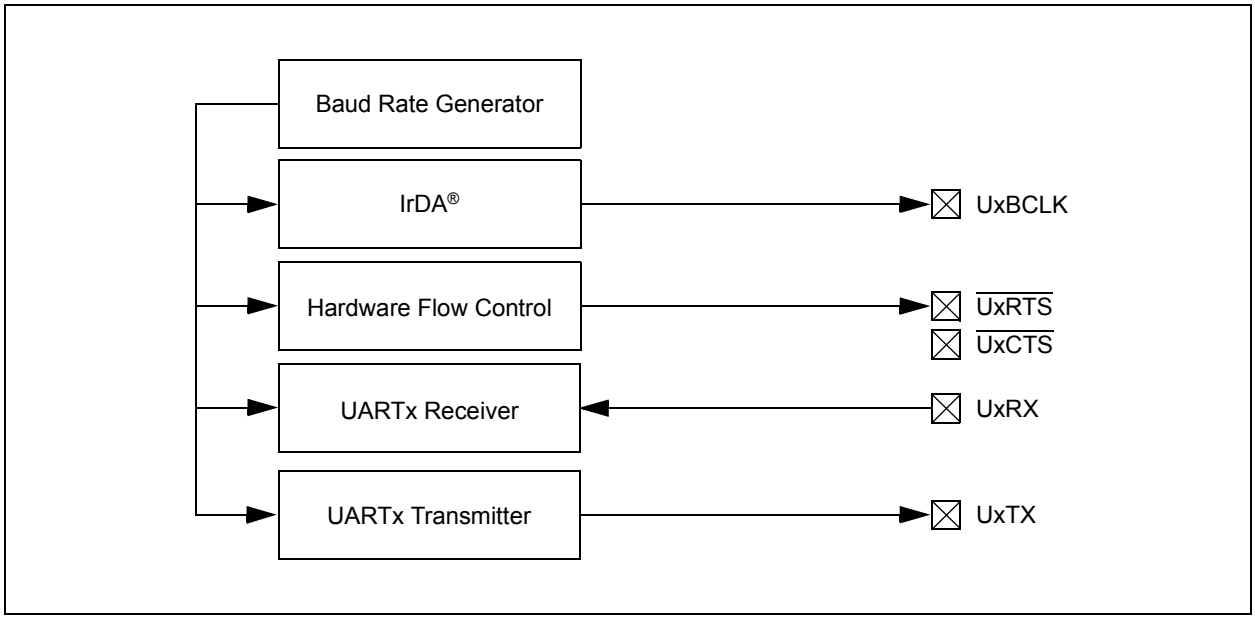
- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9^{th} bit = 1)
- Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 15-1. The UARTx module consists of these important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific USART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "UxSTA" might refer to the USART Status register for either USART1 or USART2.

FIGURE 15-1: UARTx MODULE SIMPLIFIED BLOCK DIAGRAM



19.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

19.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSH and AD1CSSL: A/D Input Scan Select Registers
- AD1CTMENH and AD1CTMENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 19-1, Register 19-2 and Register 19-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion Triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 19-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 19-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 19-6 and Register 19-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases, indicates if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 19-8 and Register 19-9) select the channels to be included for sequential scanning.

The AD1CTMENH/L registers (Register 19-10 and Register 19-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMENL is always implemented, whereas AD1CTMENH may not be implemented in devices with 16 or fewer channels.

19.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port buffer, called ADC1BUFx. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFx (x = up to 17).

The A/D result buffers are both readable and writable. When the module is active (AD1CON<15> = 1), the buffers are read-only and store the results of A/D conversions. When the module is inactive (AD1CON<15> = 0), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1<15>). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

REGISTER 19-1: AD1CON1: A/DA/D CONTROL REGISTER 1 (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This version of the TMR1 Trigger allows A/D conversions to be triggered from TMR1 while the device is operating in Sleep mode. The SSRC<3:0> = 0101 option allows conversions to be triggered in Run or Idle modes only.

REGISTER 19-10: AD1CTMENH: CTMU ENABLE REGISTER (HIGH WORD)(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN23	CTMEN22	CTMEN21	CTMEN20(2)	CTMEN19(2)	CTMEN18	CTMEN17	CTMEN16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'.

bit 7-0 **CTMEN<23:16>:** CTMU Enabled During Conversion bits(2)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as '0'.
2: The CTMEN<20:19> bits are not implemented in 20-pin devices.

REGISTER 19-11: AD1CTMENL: CTMU ENABLE REGISTER (LOW WORD)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN15	CTMEN14	CTMEN13	CTMEN12	CTMEN11	CTMEN10	CTMEN9	CTMEN8(2,3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN7(2,3)	CTMEN6(2,3)	CTMEN5(2)	CTMEN4	CTMEN3	CTMEN2	CTMEN1	CTMEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CTMEN<15:0>:** CTMU Enabled During Conversion bits(2,3)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: Unimplemented channels are read as '0'.
2: The CTMEN<8:5> bits are not implemented in 20-pin devices.
3: The CTMEN<8:6> bits are not implemented in 28-pin devices.

NOTES:

22.0 COMPARATOR MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator module, refer to the *"PIC24F Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734).

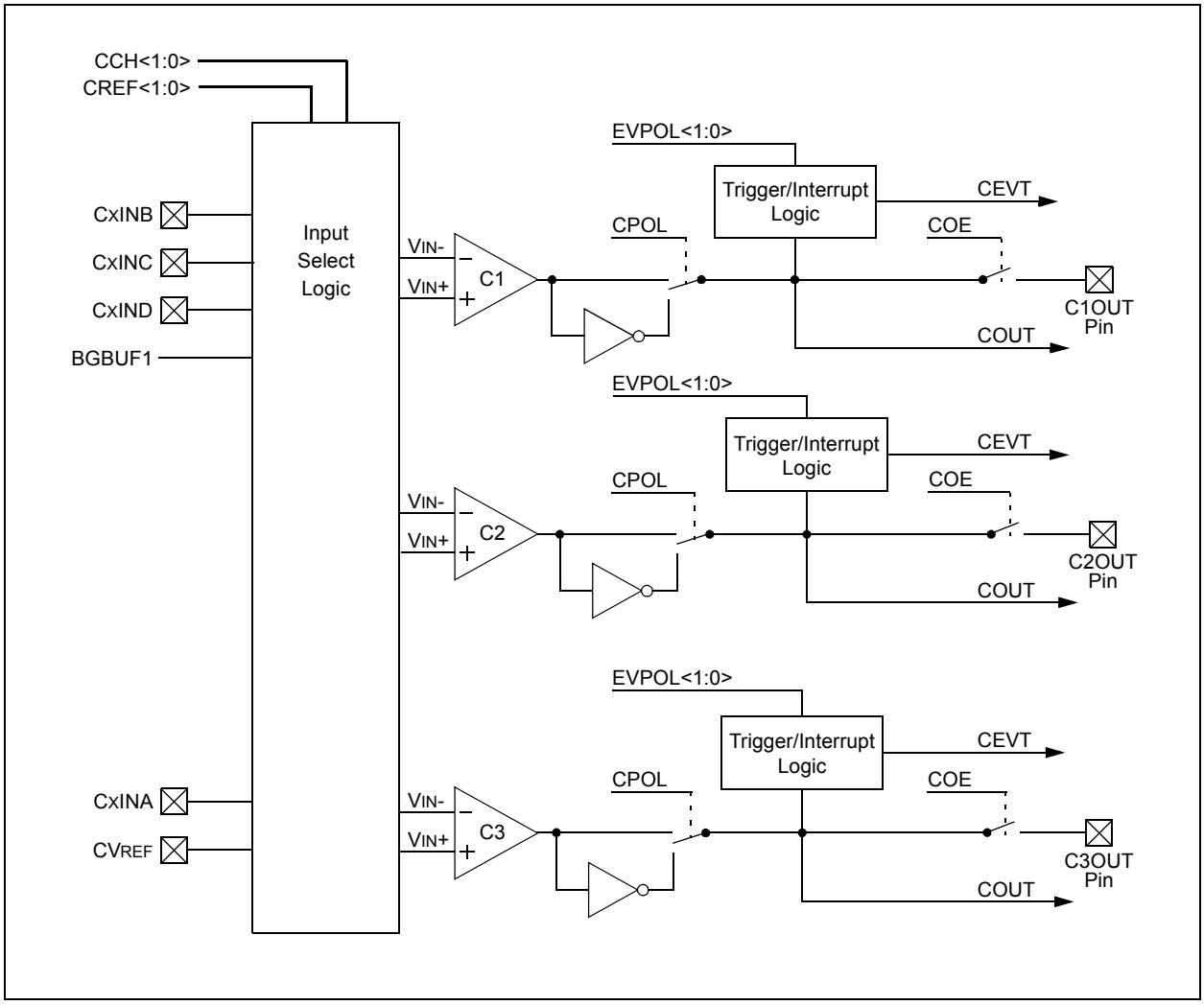
The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as a voltage reference input from either the Internal Band Gap Buffer 1 (BGBUF1) or the comparator voltage reference generator.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 22-1. Diagrams of the possible individual comparator configurations are shown in Figure 22-2.

Each comparator has its own control register, CMxCON (Register 22-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 22-2).

FIGURE 22-1: COMPARATOR x MODULE BLOCK DIAGRAM



REGISTER 25-4: FOSC: OSCILLATOR CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCKSM1	FCKSM0	SOSCSEL	POSCFREQ1	POSCFREQ0	OSCIOFNC	POSCMD1	POSCMD0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **SOSCSEL:** Secondary Oscillator Power Selection Configuration bit
1 = Secondary Oscillator is configured for high-power operation
0 = Secondary Oscillator is configured for low-power operation

bit 4-3 **POSCFREQ<1:0>:** Primary Oscillator Frequency Range Configuration bits
11 = Primary Oscillator/External Clock input frequency is greater than 8 MHz
10 = Primary Oscillator/External Clock input frequency is between 100 kHz and 8 MHz
01 = Primary Oscillator/External Clock input frequency is less than 100 kHz
00 = Reserved; do not use

bit 2 **OSCIOFNC:** CLKO Enable Configuration bit
1 = CLKO output signal is active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock (EC) mode for the CLKO to be active (POSCMD<1:0> = 11 or 00)
0 = CLKO output is disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator mode is disabled
10 = HS Oscillator mode is selected
01 = XT Oscillator mode is selected
00 = External Clock mode is selected

REGISTER 25-5: FWDT: WATCHDOG TIMER CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN1	WINDIS	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7,5 **FWDTEN<1:0>:** Watchdog Timer Enable bits

11 = WDT is enabled in hardware
10 = WDT is controlled with the SWDTEN bit setting
01 = WDT is enabled only while the device is active, WDT is disabled in Sleep; SWDTEN bit is disabled
00 = WDT is disabled in hardware; SWDTEN bit is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit

1 = Standard WDT is selected; windowed WDT is disabled
0 = Windowed WDT is enabled; note that executing a CLRWDT instruction while the WDT is disabled in hardware and software (FWDTEN<1:0> = 00 and SWDTEN (RCON<5>) = 0) will not cause a device Reset

bit 4 **FWPSA:** WDT Prescaler bit

1 = WDT prescaler ratio of 1:128
0 = WDT prescaler ratio of 1:32

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscale Select bits

1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

If the WDT is enabled in hardware (FWDTEN<1:0> = 11), it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) will need to be cleared in software after the device wakes up.

The WDT Flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

25.3.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

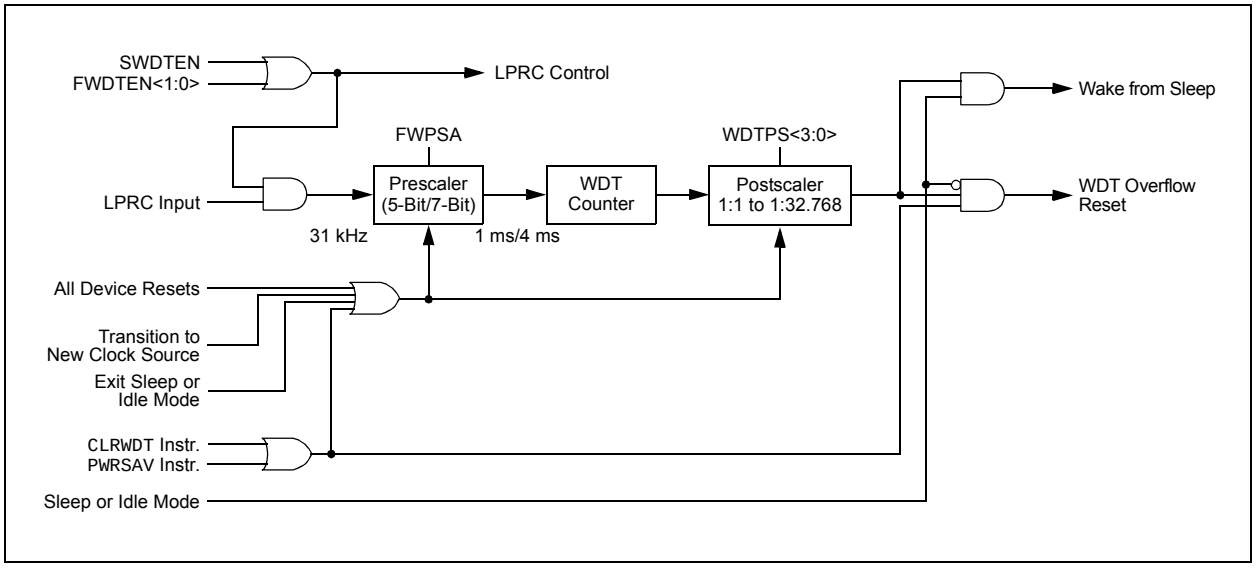
Windowed WDT mode is enabled by programming the Configuration bit, WINDIS (FWDT<6>), to '0'.

25.3.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN<1:0> Configuration bits. When both of the FWDTEN<1:0> Configuration bits are set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN<1:0> Configuration bits have been programmed to '10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments, and disable the WDT during non-critical segments, for maximum power savings. When the FWDTEN<1:0> bits are set to '01', the WDT is only enabled in Run and Idle modes, and is disabled in Sleep. Software control of the SWDTEN bit (RCON<5>) is disabled with this setting.

FIGURE 25-2: WDT BLOCK DIAGRAM



27.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FV16KM204 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FV16KM204 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} (PIC24FXXKMXXX) ..... -0.3V to +4.5V
Voltage on V_{DD} with respect to V_{SS} (PIC24FVXXKMXXX) ..... -0.3V to +6.5V
Voltage on any combined analog and digital pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any digital only pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on $\overline{MCLR}/V_{PP}$ pin with respect to V_{SS} ..... -0.3V to +9.0V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin(1) ..... 250 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(1) ..... 200 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 27-1).

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 27-17: OPERATIONAL AMPLIFIER SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**
	GBWP	Gain Bandwidth Product	—	5	—	MHz	SPDSEL = 1
			—	0.5	—	MHz	SPDSEL = 0
	SR	Slew Rate	—	1.2	—	V/µs	SPDSEL = 1
			—	0.3	—	V/µs	SPDSEL = 0
	AOL	DC Open-Loop Gain	—	90	—	dB	
	VIOFF	Input Offset Voltage	—	±2	±10	mV	
	VIBC	Input Bias Current	—	—	—	nA	**(Note 1)**
	VICM	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
	CMRR	Common-Mode Rejection Ratio	—	60	—	db	
	PSRR	Power Supply Rejection Ratio	—	60	—	dB	
	VOR	Output Voltage Range	AVSS + 200	AVSS + 5 to AVDD – 5	AVDD – 200	mV	0.5V input overdrive, no output loading

Note 1: The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI50.

TABLE 27-26: COMPARATOR TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
300	TRESP	Response Time*(1)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	μs	

* Parameters are characterized but not tested.

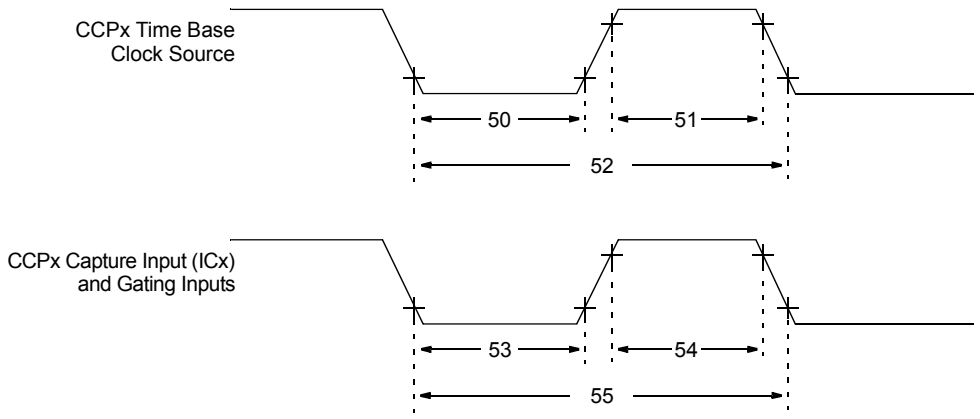
Note 1: Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 27-27: COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
VR310	TSET	Settling Time(1)	—	—	10	μs	

Note 1: Settling time is measured while CVRSS = 1 and the CVR<3:0> bits transition from '0000' to '1111'.

FIGURE 27-10: CAPTURE/COMPARE/PWM TIMINGS (MCCPx, SCCPx MODULES)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-28: CAPTURE/COMPARE/PWM REQUIREMENTS (MCCPx, SCCPx MODULES)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
50	TCLKL	CCPx Time Base Clock Source Low Time	TCY/2	—	ns	
51	TCLKH	CCPx Time Base Clock Source High Time	TCY/2	—	ns	
52	TCLK	CCPx Time Base Clock Source Period	TCY	—	ns	
53	TCCL	CCPx Capture or Gating Input Low Time	TCLK	—	ns	
54	TCCH	CCPx Capture or Gating Input High Time	TCLK	—	ns	
55	TCCP	CCPx Capture or Gating Input Period	2 * TCLK/N	—	ns	N = Prescale Value (1, 4 or 16)