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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km102-i-so

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
AN0	2	2	27	19	21	2	2	27	19	21	I	ANA	A/D Analog Inputs
AN1	3	3	28	20	22	3	3	28	20	22	I	ANA	A/D Analog Inputs
AN2	4	4	1	21	23	4	4	1	21	23	I	ANA	A/D Analog Inputs
AN3	5	5	2	22	24	5	5	2	22	24	I	ANA	A/D Analog Inputs
AN4	6	6	3	23	25	6	6	3	23	25	I	ANA	A/D Analog Inputs
AN5	—	7	4	24	26	—	7	4	24	26	I	ANA	A/D Analog Inputs
AN6	—	—	—	25	27	—	—	—	25	27	I	ANA	A/D Analog Inputs
AN7	—	—	—	26	28	—	—	—	26	28	I	ANA	A/D Analog Inputs
AN8	—	—	—	27	29	—	—	—	27	29	I	ANA	A/D Analog Inputs
AN9	18	26	23	15	16	18	26	23	15	16	I	ANA	A/D Analog Inputs
AN10	17	25	22	14	15	17	25	22	14	15	I	ANA	A/D Analog Inputs
AN11	16	24	21	11	12	16	24	21	11	12	I	ANA	A/D Analog Inputs
AN12	15	23	20	10	11	15	23	20	10	11	I	ANA	A/D Analog Inputs
AN13	7	9	6	30	33	7	9	6	30	33	I	ANA	A/D Analog Inputs
AN14	8	10	7	31	34	8	10	7	31	34	I	ANA	A/D Analog Inputs
AN15	9	11	8	33	36	9	11	8	33	36	I	ANA	A/D Analog Inputs
AN16	10	12	9	34	37	10	12	9	34	37	I	ANA	A/D Analog Inputs
AN17	—	14	11	41	45	—	14	11	41	45	I	ANA	A/D Analog Inputs
AN18	—	15	12	42	46	—	15	12	42	46	I	ANA	A/D Analog Inputs
AN19	11	16	13	43	47	11	16	13	43	47	I	ANA	A/D Analog Inputs
AN20	12	17	14	44	48	12	17	14	44	48	I	ANA	A/D Analog Inputs
AN21	13	18	15	1	1	13	18	15	1	1	I	ANA	A/D Analog Inputs
ASCL1	—	15	12	42	46	—	15	12	42	46	I/O	I ² C™	Alternate I2C1 Clock Input/Output
ASDA1	—	14	11	41	45	—	14	11	41	45	I/O	I ² C	Alternate I2C1 Data Input/Output
AVDD	20	28	25	17	18	20	28	25	17	18	P	—	A/D Supply Pins
AVSS	19	27	24	16	17	19	27	24	16	17	P	—	A/D Supply Pins
C1INA	8	7	4	24	26	8	7	4	24	26	I	ANA	Comparator 1 Input A (+)
C1INB	7	6	3	23	25	7	6	3	23	25	I	ANA	Comparator 1 Input B (-)
C1INC	5	5	2	22	24	5	5	2	22	24	I	ANA	Comparator 1 Input C (+)
C1IND	4	4	1	21	23	4	4	1	21	23	I	ANA	Comparator 1 Input D (-)

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I²C™ = I²C/SMBus input buffer

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REGISTER 7-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0, HS	R/W-0, HS	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	SBOREN	RETEN ⁽³⁾	—	—	CM	PMSLP
bit 15						bit 8	

R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						bit 0	

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
 1 = A Trap Conflict Reset has occurred
 0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
 1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
 0 = An illegal opcode or Uninitialized W Reset has not occurred
- bit 13 **SBOREN:** Software Enable/Disable of BOR bit
 1 = BOR is turned on in software
 0 = BOR is turned off in software
- bit 12 **RETEN:** Retention Sleep Mode⁽³⁾
 1 = Regulated voltage supply provided by the Retention Regulator (RETREG) during Sleep
 0 = Regulated voltage supply provided by the main Voltage Regulator (VREG) during Sleep
- bit 11-10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Word Mismatch Reset Flag bit
 1 = A Configuration Word Mismatch Reset has occurred
 0 = A Configuration Word Mismatch Reset has not occurred
- bit 8 **PMSLP:** Program Memory Power During Sleep bit
 1 = Program memory bias voltage remains powered during Sleep
 0 = Program memory bias voltage is powered down during Sleep and the voltage regulator enters Standby mode
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
 1 = A Master Clear (pin) Reset has occurred
 0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
 1 = A RESET instruction has been executed
 0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
 1 = WDT is enabled
 0 = WDT is disabled

- Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.
- 3:** This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

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7.1 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 7-2. If clock switching is disabled, the system clock source is always selected according to the Oscillator Configuration bits. For more information, see **Section 9.0 “Oscillator Configuration”**.

TABLE 7-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC<2:0> Configuration bits (FOSCSEL<2:0>)
BOR	
MCLR	COSC<2:0> Control bits (OSCCON<14:12>)
WDTO	
SWR	

7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-3. Note that the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR and PWRT delay times expire.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR ⁽⁶⁾	EC	TPOR + TPWRT	—	1, 2
	FRC, FRCDIV	TPOR + TPWRT	TFRC	1, 2, 3
	LPRC	TPOR + TPWRT	TLPRC	1, 2, 3
	ECPLL	TPOR + TPWRT	TLOCK	1, 2, 4
	FRCPLL	TPOR + TPWRT	TFRC + TLOCK	1, 2, 3, 4
	XT, HS, SOSC	TPOR + TPWRT	TOST	1, 2, 5
	XTPLL, HSPLL	TPOR + TPWRT	TOST + TLOCK	1, 2, 4, 5
BOR	EC	TPWRT	—	2
	FRC, FRCDIV	TPWRT	TFRC	2, 3
	LPRC	TPWRT	TLPRC	2, 3
	ECPLL	TPWRT	TLOCK	2, 4
	FRCPLL	TPWRT	TFRC + TLOCK	2, 3, 4
	XT, HS, SOSC	TPWRT	TOST	2, 5
	XTPLL, HSPLL	TPWRT	TFRC + TLOCK	2, 3, 4
All Others	Any Clock	—	—	None

Note 1: TPOR = Power-on Reset delay.

2: TPWRT = 64 ms nominal if the Power-up Timer is enabled; otherwise, it is zero.

3: TFRC and TLPRC = RC Oscillator start-up times.

4: TLOCK = PLL Lock time.

5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

6: If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

Note: For detailed operating frequency and timing specifications, see **Section 27.0 “Electrical Characteristics”**.

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REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	R/W-0, HS
NVMIF	—	AD1IF	U1TXIF	U1RXIF	—	—	CCT2IF
bit 15							bit 8

R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
CCT1IF	CCP4IF	CCP3IF	—	T1IF	CCP2IF	CCP1IF	INT0IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	NVMIF: NVM Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 14	Unimplemented: Read as '0'
bit 13	AD1IF: A/D Conversion Complete Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 12	U1TXIF: UART1 Transmitter Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 11	U1RXIF: UART1 Receiver Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 10-9	Unimplemented: Read as '0'
bit 8	CCT2IF: Capture/Compare 2 Timer Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 7	CCT1IF: Capture/Compare 1 Timer Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 6	CCP4IF: Capture/Compare 4 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 5	CCP3IF: Capture/Compare 3 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	T1IF: Timer1 Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	CCP2IF: Capture/Compare 2 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 1	CCP1IF: Capture/Compare 1 Event Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	INT0IF: External Interrupt 0 Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

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REGISTER 8-9: IFS4: INTERRUPT FLAG STATUS REGISTER 4

R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	U-0	R/W-0, HS
DAC2IF	DAC1IF	CTMUIF	—	—	—	—	HLVDIF
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
—	—	—	—	—	U2ERIF	U1ERIF	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **DAC2IF:** Digital-to-Analog Converter 2 Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 14 **DAC1IF:** Digital-to-Analog Converter 1 Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 13 **CTMUIF:** CTMU Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 12-9 **Unimplemented:** Read as '0'
- bit 8 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 7-3 **Unimplemented:** Read as '0'
- bit 2 **U2ERIF:** UART2 Error Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 1 **U1ERIF:** UART1 Error Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 0 **Unimplemented:** Read as '0'

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REGISTER 8-14: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	CCT5IE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **CCT5IE:** Capture/Compare 5 Timer Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 8-0 **Unimplemented:** Read as '0'

REGISTER 8-15: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	RTCIE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0
—	—	—	—	—	BCL2IE	SSP2IE	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 13-3 **Unimplemented:** Read as '0'

bit 2 **BCL2IE:** MSSP2 I²C™ Bus Collision Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 1 **SSP2IE:** MSSP2 SPI/I²C Event Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

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11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

11.2 Configuring Analog Port Pins

The use of the ANSx and TRISx registers controls the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

11.2.1 ANALOG SELECTION REGISTER

I/O pins with shared analog functionality, such as A/D inputs and comparator inputs, must have their digital inputs shut off when analog functionality is used. Note that analog functionality includes an analog voltage being applied to the pin externally.

To allow for analog control, the ANSx registers are provided. There is one ANSx register for each port (ANSA, ANSB and ANSC). Within each ANSx register, there is a bit for each pin that shares analog functionality with the digital I/O functionality.

If a particular pin does not have an analog function, that bit is unimplemented. See Register 11-1 to Register 11-3 for implementation.

REGISTER 11-1: ANSA: PORTA ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	ANSA4 ⁽¹⁾	ANSA3	ANSA2	ANSA1	ANSA0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **ANSA<4:0>:** Analog Select Control bits⁽¹⁾

1 = Digital input buffer is not active (use for analog input)

0 = Digital input buffer is active

Note 1: The ANSA4 bit is not available on 20-pin devices.

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REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1 ⁽¹⁾	TECS0 ⁽¹⁾
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TON:** Timer1 On bit
 1 = Starts 16-bit Timer1
 0 = Stops 16-bit Timer1
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Select bits⁽¹⁾
 11 = Reserved; do not use
 10 = Timer1 uses the LPRC as the clock source
 01 = Timer1 uses the External Clock (EC) from T1CK
 00 = Timer1 uses the Secondary Oscillator (SOSC) as the clock source
- bit 7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
 When TCS = 1:
 1 = Synchronizes External Clock input
 0 = Does not synchronize External Clock input
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer1 Clock Source Select bit
 1 = Timer1 clock source is selected by TECS<1:0>
 0 = Internal clock (FOSC/2)
- bit 0 **Unimplemented:** Read as '0'

Note 1: The TECSx bits are valid only when TCS = 1.

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TABLE 13-6: SYNCHRONIZATION SOURCES

SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPR Match or FFFFh
00001	MCCP1 or SCCP1 Sync Output
00010	MCCP2 or SCCP2 Sync Output
00011	MCCP3 or SCCP3 Sync Output
00100	MCCP4 or SCCP4 Sync Output
00101	MCCP5 or SCCP5 Sync Output
00110 to 01010	Unused
01011	Timer1 Sync Output ⁽¹⁾
01100 to 10000	Unused
10001	CLC1 Output ⁽¹⁾
10010	CLC2 Output ⁽¹⁾
10011 to 11010	Unused
11011	A/D ⁽¹⁾
11110	Unused
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

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16.2 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

16.2.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTRx bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 16-1).

By writing the RTCVALH byte, the RTCC Pointer value, the RTCPTR<1:0> bits decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 16-1: RTCVAL REGISTER MAPPING

RTCPTR<1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTRx bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 16-2).

By writing the ALRMVALH byte, the ALRMPTR<1:0> bits (Alarm Pointer value) decrement by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL, until the pointer value is manually changed.

TABLE 16-2: ALRMVAL REGISTER MAPPING

ALRMPTR<1:0>	Alarm Value Register Window	
	ALRMVALH<15:8>	ALRMVALL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	PWCSTAB	PWCSAMP

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes, the ALRMPTR<1:0> value will be decremented. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations.

16.2.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (see Example 16-1 and Example 16-2).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN. Therefore, it is recommended that code follow the procedure in Example 16-2.

16.2.3 SELECTING RTCC CLOCK SOURCE

There are four reference source clock options that can be selected for the RTCC using the RTCCLK<1:0> bits (RTCPWC<11:10>): 00 = Secondary Oscillator, 01 = LPRC, 10 = 50 Hz External Clock and 11 = 60 Hz External Clock.

EXAMPLE 16-1: SETTING THE RTCWREN BIT IN ASSEMBLY

```
push    w7           ; Store W7 and W8 values on the stack.
push    w8
disi    #5           ; Disable interrupts until sequence is complete.
mov     #0x55, w7     ; Write 0x55 unlock value to NVMKEY.
mov     w7, NVMKEY
mov     #0xAA, w8     ; Write 0xAA unlock value to NVMKEY.
mov     w8, NVMKEY
bset    RCFGCAL, #13  ; Set the RTCWREN bit.
pop     w8           ; Restore the original W register values from the stack.
pop     w7
```

EXAMPLE 16-2: SETTING THE RTCWREN BIT IN 'C'

```
//This builtin function executes implements the unlock sequence and sets
//the RTCWREN bit.
__builtin_write_RTCWREN();
```

FIGURE 16-2: ALARM MASK SETTINGS

Alarm Mask Setting (AMASK<3:0>)	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 - Every half second 0001 - Every second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> : <input type="checkbox"/> <input type="checkbox"/>	: <input type="checkbox"/> <input type="checkbox"/>	: <input type="checkbox"/> <input type="checkbox"/>
0010 - Every 10 seconds	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> : <input type="checkbox"/> <input type="checkbox"/>	: <input type="checkbox"/> <input type="checkbox"/>	: <input type="checkbox"/> <input type="checkbox"/> s
0011 - Every minute	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> : <input type="checkbox"/> <input type="checkbox"/>	: <input type="checkbox"/> <input type="checkbox"/>	: s <input type="checkbox"/> s
0100 - Every 10 minutes	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> : <input type="checkbox"/> m	: s	: s s
0101 - Every hour	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> : m	m	: s s
0110 - Every day	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	h h : m	m	: s s
0111 - Every week	d	<input type="checkbox"/> <input type="checkbox"/>	/ <input type="checkbox"/> <input type="checkbox"/>	h h : m	m	: s s
1000 - Every month	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	/ d d	h h : m	m	: s s
1001 - Every year ⁽¹⁾	<input type="checkbox"/>	m m / d d		h h : m	m	: s s

Note 1: Annually, except when configured for February 29.

16.5 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current low-power mode (Sleep, Deep Sleep, etc.).

To enable this feature, the RTCC must be enabled (RTCEN = 1), the PWCEN register bit must be set and the RTCC pin must be driving the PWC control signal (RTC OE = 1 and RTCCLK<1:0> = 11).

The polarity of the PWC control signal may be chosen using the PWCPOL register bit. Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin. This setting is able to drive the GND pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

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REGISTER 17-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

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REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER (CONTINUED)

- bit 7-5 **CH0NA<2:0>**: Sample A Channel 0 Negative Input Select bits
The same definitions as for CHONB<2:0>.
- bit 4-0 **CH0SA<4:0>**: Sample A Channel 0 Positive Input Select bits
The same definitions as for CHONA<4:0>.

- Note 1:** This is implemented on 44-pin devices only.
- 2:** This is implemented on 28-pin and 44-pin devices only.
- 3:** The band gap value used for this input is 2x or 4x the internal VBG, which is selected when PVCFG<1:0> = 1x.

REGISTER 19-6: AD1CHITH: A/D SCAN COMPARE HIT REGISTER (HIGH WORD)⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH23	CHH22	CHH21	CHH20 ⁽²⁾	CHH19 ⁽²⁾	CHH18	CHH17	CHH16
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'.
- bit 7-0 **CHH<23:16>**: A/D Compare Hit bits⁽²⁾
- If CM<1:0> = 11:
- 1 = A/D Result Buffer x has been written with data or a match has occurred
- 0 = A/D Result Buffer x has not been written with data
- For All Other Values of CM<1:0>:
- 1 = A match has occurred on A/D Result Channel x
- 0 = No match has occurred on A/D Result Channel x

- Note 1:** Unimplemented channels are read as '0'.
- 2:** The CHH<20:19> bits are not implemented in 20-pin devices.

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NOTES:

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REGISTER 21-1: AMPxCON: OP AMP x CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—
bit 15				bit 8			

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **AMPEN:** Op Amp x Control Module Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **AMPSIDL:** Op Amp x Peripheral Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **AMPSLP:** Op Amp x Peripheral Enabled in Sleep Mode bit
 1 = Continues module operation when device enters Sleep mode
 0 = Discontinues module operation in Sleep mode
- bit 11-8 **Unimplemented:** Read as '0'
- bit 7 **SPDSEL:** Op Amp x Power/Speed Select bit
 1 = Higher power and bandwidth (faster response time)
 0 = Lower power and bandwidth (slower response time)
- bit 6 **Unimplemented:** Read as '0'
- bit 5-3 **NINSEL<2:0>:** Negative Op Amp Input Select bits
 111 = Reserved; do not use
 110 = Reserved; do not use
 101 = Op amp negative input is connected to the op amp output (voltage follower)
 100 = Reserved; do not use
 011 = Reserved; do not use
 010 = Op amp negative input is connected to the OAxIND pin
 001 = Op amp negative input is connected to the OAxINB pin
 000 = Op amp negative input is connected to AVss
- bit 2-0 **PINSEL<2:0>:** Positive Op Amp Input Select bits
 111 = Op amp positive input is connected to the output of the A/D input multiplexer
 110 = Reserved; do not use
 101 = Op amp positive input is connected to the DAC1 output for OA1 (DAC2 output for OA2)
 100 = Reserved; do not use
 011 = Reserved; do not use
 010 = Op amp positive input is connected to the OAxINC pin
 001 = Op amp positive input is connected to the OAxINA pin
 000 = Op amp positive input is connected to AVss

Note 1: This register is available only on PIC24F(V)16KM2XX devices.

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REGISTER 24-1: CTMUCON1L: CTMU CONTROL 1 LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit

1 = Enables edge delay generation

0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit

1 = Edges are not blocked

0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit

1 = Edge 1 event must occur before Edge 2 event can occur

0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit

1 = Analog current source output is grounded

0 = Analog current source output is not grounded

bit 8 **CTTRIG:** CTMU Trigger Control bit

1 = Trigger output is enabled

0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits

011111 = Maximum positive change from nominal current

011110

•

•

•

000001 = Minimum positive change from nominal current

000000 = Nominal current output specified by IRNG<1:0>

111111 = Minimum negative change from nominal current

•

•

•

100010

100001 = Maximum negative change from nominal current

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REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER (CONTINUED)

- bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge
0 = Edge 2 is programmed for a negative edge
- bit 5-2 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = Edge 2 source is the Comparator 3 output
1110 = Edge 2 source is the Comparator 2 output
1101 = Edge 2 source is the Comparator 1 output
1100 = Unimplemented; do not use
1011 = Edge 2 source is CLC1
1010 = Edge 2 source is the MCCP2 Compare Event (CCP2IF)
1001 = Unimplemented; do not use
1000 = Edge 2 source is CTED13
0111 = Edge 2 source is CTED12
0110 = Edge 2 source is CTED11⁽²⁾
0101 = Edge 2 source is CTED10
0100 = Edge 2 source is CTED9⁽²⁾
0011 = Edge 2 source is CTED1
0010 = Edge 2 source is CTED2
0001 = Edge 2 source is the MCCP1 Compare Event (CCP1IF)
0000 = Edge 2 source is Timer1
- bit 1-0 **Unimplemented:** Read as '0'

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.

2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

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FIGURE 27-3: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)

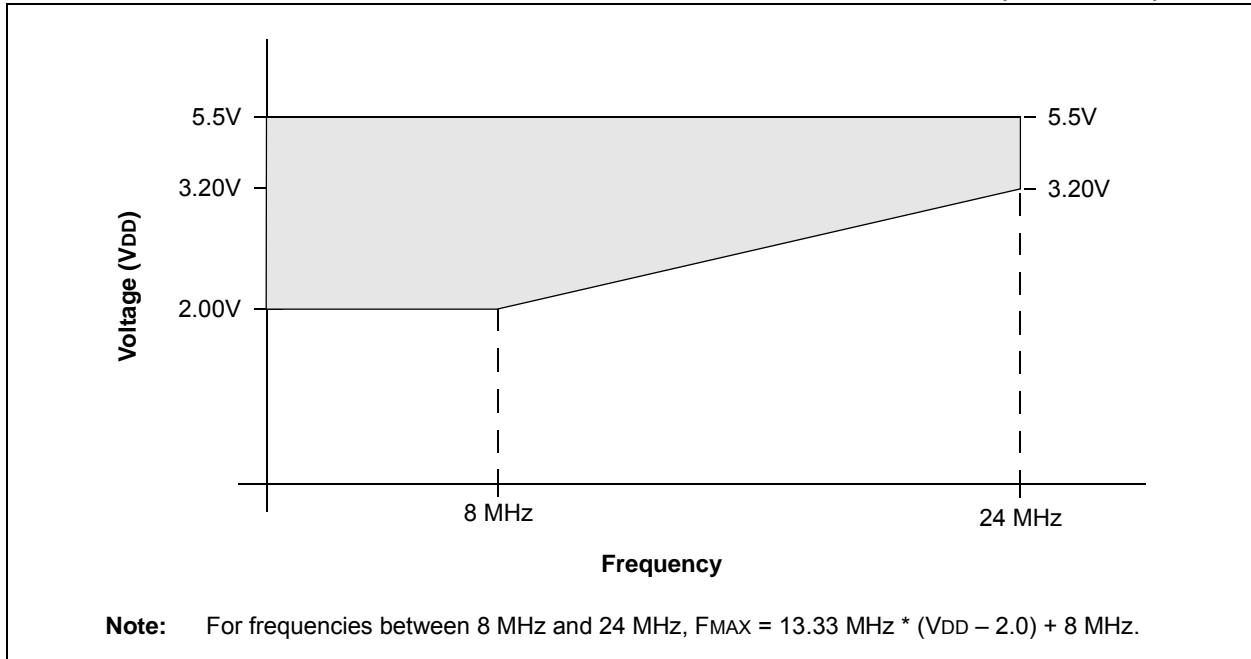
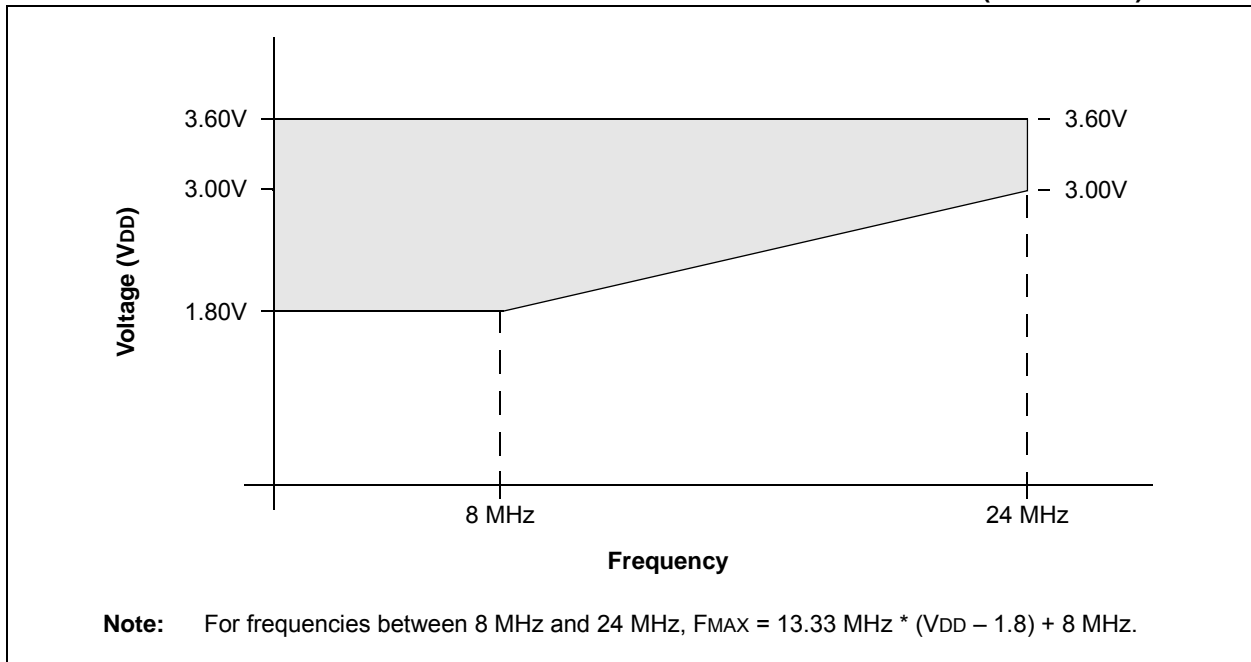


FIGURE 27-4: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)



PIC24FV16KM204 FAMILY

FIGURE 27-6: EXTERNAL CLOCK TIMING

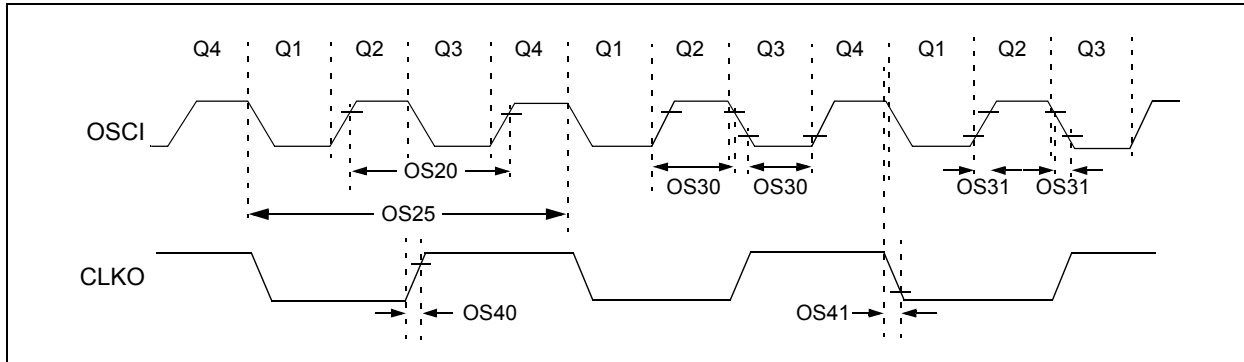


TABLE 27-20: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204)				
			Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS10	Fosc	External CLKI Frequency (External Clocks allowed only in EC mode)	DC 4 DC 4	— — — —	32 8 24 6	MHz MHz MHz MHz	EC, -40°C < T _A < +85°C ECPLL, -40°C < T _A < +85°C EC, -40°C < T _A < +125°C ECPLL, -40°C < T _A < +125°C
		Oscillator Frequency	0.2 4 4 4 31	— — — — —	4 25 8 6 33	MHz MHz MHz MHz kHz	XT HS XTPLL, -40°C < T _A < +85°C XTPLL, -40°C < T _A < +125°C SOSC
OS20	Tosc	Tosc = 1/Fosc	—	—	—	—	See Parameter OS10 for Fosc value
OS25	Tcy	Instruction Cycle Time ⁽²⁾	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x Tosc	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ⁽³⁾	—	6	10	ns	
OS41	TckF	CLKO Fall Time ⁽³⁾	—	6	10	ns	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an External Clock applied to the OSCI/CLKI pin. When an External Clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.
- Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 Tcy) and high for the Q3-Q4 period (1/2 Tcy).

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