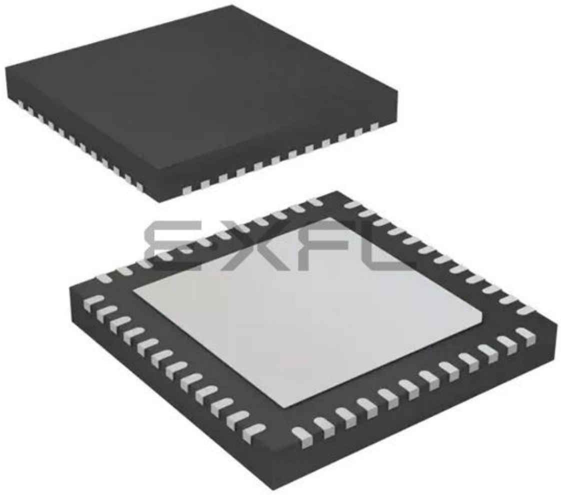

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### What is "Embedded - Microcontrollers"?

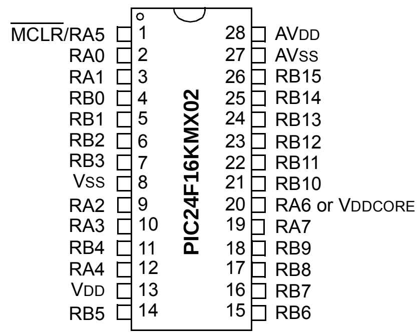
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 16KB (5.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5V |
| Data Converters | A/D 22x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UFQFN Exposed Pad |
| Supplier Device Package | 48-UQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km104-i-mv |

## Pin Diagrams (Continued)

**28-Pin SPDIP/SSOP/SOIC**




| Pin | Pin Features | |
|---|---|---|
| | PIC24FXXKMX02 | PIC24FVXXKMX02 |
| 1 | MCLR/VPP/RA5 | |
| 2 | CVREF+/VREF+/ /AN0/ /CN2/RA0 | |
| 3 | CVREF-/VREF-/AN1/CN3/RA1 | CVREF-/VREF-/AN1/RA1 |
| 4 | PGED1/AN2/CTCMP/ULPWU/C1IND/ / / /CN4/RB0 | |
| 5 | PGEC1/ / /AN3/C1INC/ / /CTED12/CN5/RB1 | |
| 6 | / /AN4/C1INB/ / /U1RX/TCKIB/CTED13/CN6/RB2 | |
| 7 | /AN5/C1INA/ / /CN7/RB3 | |
| 8 | VSS | |
| 9 | OSCI/CLKI/AN13/CN30/RA2 | |
| 10 | OSCO/CLKO/AN14/CN29/RA3 | |
| 11 | SOSCI/AN15/ / /CN1/RB4 | |
| 12 | SOSCO/SCLKI/AN16/PWRLCLK/ /CN0/RA4 | |
| 13 | VDD | |
| 14 | PGED3/AN17/ASDA1/ / /OC1E/CLCINA/CN27/RB5 | |
| 15 | PGEC3/AN18/ASCL1/ / /OC1F/CLCINB/CN24/RB6 | |
| 16 | AN19/U1TX/INT0/CN23/RB7 | AN19/U1TX/ / /INT0/CN23/RB7 |
| 17 | AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8 | |
| 18 | AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/ /CLC1O/CTED4/CN21/RB9 | |
| 19 | /IC1/ / /CTED3/CN9/RA7 | |
| 20 | /OC1A/CTED1/INT2/CN8/RA6 | VCAP OR VDDCORE |
| 21 | PGED2/SDI1/ /OC1C/CTED11/CN16/RB10 | |
| 22 | PGEC2/SCK1/OC2A/CTED9/CN15/RB11 | |
| 23 | /AN12/HLVDIN/ / / /CTED2/CN14/RB12 | /AN12/HLVDIN/ / / /CTED2/INT2/CN14/RB12 |
| 24 | / /AN11/SDO1/OCFB/ /OC1D/CTPLS/CN13/RB13 | |
| 25 | /CVREF/ / /AN10/ / /C1OUT/OCFA/CTED5/INT1/CN12/RB14 | |
| 26 | / /AN9/ /REFO/SS1/TCKIA/CTED6/CN11/RB15 | |
| 27 | VSS/AVSS | |
| 28 | VDD/AVDD | |

**Legend:** Values in indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.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### 1.1.4 EASY MIGRATION

The PIC24FV16KM204 family devices have two variants. The KM20X variant provides the full feature set of the device, while the KM10X offers a reduced peripheral set, allowing for the balance of features and cost (refer to Table 1-1). Both variants allow for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, different die variants, or even moving from 20-pin or 28-pin devices to 44-pin/48-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple to the powerful and complex, yet still selecting a Microchip device.

## 1.2 Other Special Features

- Communications: The PIC24FV16KM204 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an MSSP module which implements both SPI and I$^2$C™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- Analog Features: Select members of the PIC24FV16KM204 family include two 8-bit Digital-to-Analog Converters which offer support in Idle mode, and left and right justified input data, as well as up to two operational amplifiers with selectable power and speed modes.
- Real-Time Clock/Calendar (RTCC): This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- 12-Bit A/D Converter: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep, to reduce power, or in Active mode to improve throughput.
- Charge Time Measurement Unit (CTMU) Interface: The PIC24FV16KM204 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing, and also for precision time measurement and pulse generation. The CTMU can also be connected to the operational amplifiers to provide active guarding, which provides increased robustness in the presence of noise in capacitive touch applications.

## 1.3 Details on Individual Family Members

Devices in the PIC24FV16KM204 family are available in 20-pin, 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

Members of the PIC24FV16KM204 family are available as both standard and high-voltage devices. High-voltage devices, designated with an “FV” in the part number (such as PIC24FV16KM204), accommodate an operating VDD range of 2.0V to 5.5V and have an on-board voltage regulator that powers the core. Peripherals operate at VDD.

Standard devices, designated by “F” (such as PIC24F16KM204), function over a lower VDD range of 1.8V to 3.6V. These parts do not have an internal regulator, and both the core and peripherals operate directly from VDD.

The PIC24FV16KM204 family may be thought of as two different device groups, both offering slightly different sets of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The number of external analog channels available
- The number of Digital-to-Analog Converters
- The number of operational amplifiers
- The number of analog comparators
- The presence of a Real-Time Clock and Calendar (RTCC)
- The number and type of CCP modules (i.e., MCCP vs. SCCP)
- The number of serial communication modules (both MSSPs and UARTs)
- The number of Configurable Logic Cell (CLC) modules

The general differences between the different sub-families are shown in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FV16KM204 family devices, sorted by function, is provided in Table 1-5.


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**TABLE 1-1: DEVICE FEATURES FOR THE PIC24F16KM204 FAMILY**

| Features | PIC24F16KM204 | PIC24F08KM204 | PIC24F16KM202 | PIC24F08KM202 |
|---|---|---|---|---|
| Operating Frequency | DC-32 MHz | | | |
| Program Memory (bytes) | 16K | 8K | 16K | 8K |
| Program Memory (instructions) | 5632 | 2816 | 5632 | 2816 |
| Data Memory (bytes) | 2048 | | | |
| Data EEPROM Memory (bytes) | 512 | | | |
| Interrupt Sources (soft vectors/NMI traps) | 40 (36/4) | | | |
| Voltage Range | 1.8-3.6V | | | |
| I/O Ports | PORTA<11:0><br>PORTB<15:0><br>PORTC<9:0> | | PORTA<7:0><br>PORTB<15:0> | |
| Total I/O Pins | 38 | | 24 | |
| Timers | 11<br>(One 16-bit timer, five MCCPs/SCCPs with up to two 16/32 timers each) | | | |
| Capture/Compare/PWM modules<br>MCCP<br>SCCP | <br>3<br>2 | | | |
| Serial Communications<br>MSSP<br>UART | <br>2<br>2 | | | |
| Input Change Notification Interrupt | 37 | | 23 | |
| 12-Bit Analog-to-Digital Module (input channels) | 22 | 22 | 19 | 19 |
| Analog Comparators | 3 | | | |
| 8-Bit Digital-to-Analog Converters | 2 | | | |
| Operational Amplifiers | 2 | | | |
| Charge Time Measurement Unit (CTMU) | Yes | | | |
| Real-Time Clock and Calendar (RTCC) | Yes | | | |
| Configurable Logic Cell (CLC) | 2 | | | |
| Resets (and delays) | POR, BOR, RESET Instruction, $\overline{\text{MCLR}}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (PWRT, OST, PLL Lock) | | | |
| Instruction Set | 76 Base Instructions, Multiple Addressing Mode Variations | | | |
| Packages | 44-Pin QFN/TQFP,<br>48-Pin UQFN | | 28-Pin<br>SPDIP/SSOP/SOIC/QFN | |

**NOTES:**


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## TABLE 4-25: A/D REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 300h | A/D Data Buffer 0/Threshold for Channel 0/Threshold for Channel 0 & 12 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 302h | A/D Data Buffer 1/Threshold for Channel 1/Threshold for Channel 1 & 13 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 304h | A/D Data Buffer 2/Threshold for Channel 2/Threshold for Channel 2 & 14 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 306h | A/D Data Buffer 3/Threshold for Channel 3/Threshold for Channel 3 & 15 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 308h | A/D Data Buffer 4/Threshold for Channel 4/Threshold for Channel 4 & 16 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 30Ah | A/D Data Buffer 5/Threshold for Channel 5/Threshold for Channel 5 & 17 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 30Ch | A/D Data Buffer 6/Threshold for Channel 6/Threshold for Channel 6 & 18 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 30Eh | A/D Data Buffer 7/Threshold for Channel 7/Threshold for Channel 7 & 19 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 310h | A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 8 & 20 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 312h | A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 9 & 21 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF10 | 314h | A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 10 & 22 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF11 | 316h | A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 11 & 23 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF12 | 318h | A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 0 & 12 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF13 | 31Ah | A/D Data Buffer 13/Threshold for Channel 13/Threshold for Channel 1 & 13 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF14 | 31Ch | A/D Data Buffer 14/Threshold for Channel 14/Threshold for Channel 2 & 14 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF15 | 31Eh | A/D Data Buffer 15/Threshold for Channel 15/Threshold for Channel 3 & 15 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF16 | 320h | A/D Data Buffer 16/Threshold for Channel 16/Threshold for Channel 4 & 16 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF17 | 322h | A/D Data Buffer 17/Threshold for Channel 17/Threshold for Channel 5 & 17 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF18 | 324h | A/D Data Buffer 18/Threshold for Channel 18/Threshold for Channel 6 & 18 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF19 | 326h | A/D Data Buffer 19/Threshold for Channel 19/Threshold for Channel 7 & 19 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF20 | 328h | A/D Data Buffer 20/Threshold for Channel 20/Threshold for Channel 8 & 20 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF21 | 32Ah | A/D Data Buffer 21/Threshold for Channel 21/Threshold for Channel 9 & 21 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF22 | 32Ch | A/D Data Buffer 22/Threshold for Channel 22/Threshold for Channel 10 & 22 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF23 | 32Eh | A/D Data Buffer 23/Threshold for Channel 23/Threshold for Channel 11 & 23 in Window Compare | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 340h | ADON | — | ADSIDL | — | — | MODE12 | FORM1 | FORM0 | SSRC3 | SSRC2 | SSRC1 | SSRC0 | — | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 342h | PVCFG1 | PVCFG0 | NVCFG0 | — | BUFREGEN | CSCNA | — | — | BUFS | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS | 0000 |
| AD1CON3 | 344h | ADRC | EXTSAM | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 |
| AD1CHS | 348h | CH0NB2 | CH0NB1 | CH0NB0 | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 | CH0NA2 | CH0NA1 | CH0NA0 | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 | 0000 |
| AD1CSSH | 34Eh | — | CSS30 | CSS29 | CSS28 | CSS27 | CSS26 | — | — | CSS23 | CSS22 | CSS21 | CSS20[1] | CSS19[1] | CSS18 | CSS17 | CSS16 | 0000 |
| AD1CSSL | 350h | CSS15 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8[1,2] | CSS7[1,2] | CSS6[1,2] | CSS5[1] | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 | 0000 |
| AD1CON5 | 354h | ASEN | LPEN | CTMREQ | BGREQ | r | — | ASINT1 | ASINT0 | — | — | — | — | WM1 | WM0 | CM1 | CM0 | 0000 |
| AD1CHITH | 356h | — | — | — | — | — | — | — | — | CHH23 | CHH22 | CHH21 | CHH20[1] | CHH19[1] | CHH18 | CHH17 | CHH16 | 0000 |
| AD1CHITL | 358h | CHH15 | CHH14 | CHH13 | CHH12 | CHH11 | CHH10 | CHH9 | CHH8[1,2] | CHH7[1,2] | CHH6[1,2] | CHH5[1] | CHH4 | CHH3 | CHH2 | CHH1 | CHH0 | 0000 |
| AD1CTMENH | 360h | — | — | — | — | — | — | — | — | CTMEN23 | CTMEN22 | CTMEN21 | CTMEN20[1] | CTMEN19[1] | CTMEN18 | CTMEN17 | CTMEN16 | 0000 |
| AD1CTMENL | 362h | CTMEN15 | CTMEN14 | CTMEN13 | CTMEN12 | CTMEN11 | CTMEN10 | CTMEN9 | CTMEN8[(1,2] | CTMEN7[1,2] | CTMEN6[1,2] | CTMEN5[1] | CTMEN4 | CTMEN3 | CTMEN2 | CTMEN1 | CTMEN0 | 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

**Note 1:** These bits are not implemented in 20-pin devices.

**2:** These bits are not implemented in 28-pin devices.

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## 5.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 32 instructions or 96 bytes. RTSP allows the user to erase blocks of 1 row, 2 rows and 4 rows (32, 64 and 128 instructions) at a time, and to program one row at a time. It is also possible to program single words.

The 1-row (96 bytes), 2-row (192 bytes) and 4-row (384 bytes) erase blocks, and single row write block (96 bytes) are edge-aligned, from the beginning of program memory.

When data is written to program memory using `TBLWT` instructions, the data is not written directly to memory. Instead, data written using Table Writes is stored in holding latches until the programming sequence is executed.

Any number of `TBLWT` instructions can be executed and a write will be successfully performed. However, 32 `TBLWT` instructions are required to write the full row of memory.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

| **Note:** | Writing to a location multiple times, without erasing it, is not recommended. |
|---|---|

All of the Table Write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

## 5.3 Enhanced In-Circuit Serial Programming

Enhanced ICSP uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

## 5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls the blocks that need to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to **Section 5.5 “Programming Operations”** for further details.

## 5.5 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.


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**REGISTER 7-1: RCON: RESET CONTROL REGISTER(1)**

| R/W-0, HS | R/W-0, HS | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | SBOREN | RETEN(3) | — | — | CM | PMSLP |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-1, HS | R/W-1, HS |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN(2) | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN:** Retention Sleep Mode(3)
1 = Regulated voltage supply provided by the Retention Regulator (RETREG) during Sleep
0 = Regulated voltage supply provided by the main Voltage Regulator (VREG) during Sleep

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **PMSLP:** Program Memory Power During Sleep bit
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep and the voltage regulator enters Standby mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
**2:** If the FWDTEN<1:0> Configuration bits are ‘11’ (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.
**3:** This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.


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### REGISTER 7-1: RCON: RESET CONTROL REGISTER[1] (CONTINUED)

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
**2:** If the FWDTEN<1:0> Configuration bits are ‘11’ (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.
**3:** This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

### TABLE 7-1: RESET FLAG BIT OPERATION

| Flag Bit | Setting Event | Clearing Event |
|---|---|---|
| TRAPR (RCON<15>) | Trap Conflict Event | POR |
| IOPUWR (RCON<14>) | Illegal Opcode or Uninitialized W Register Access | POR |
| CM (RCON<9>) | Configuration Mismatch Reset | POR |
| EXTR (RCON<7>) | $\overline{\text{MCLR}}$ Reset | POR |
| SWR (RCON<6>) | RESET Instruction | POR |
| WDTO (RCON<4>) | WDT Time-out | PWRSAV Instruction, POR |
| SLEEP (RCON<3>) | PWRSAV #SLEEP Instruction | POR |
| IDLE (RCON<2>) | PWRSAV #IDLE Instruction | POR |
| BOR (RCON<1>) | POR, BOR | — |
| POR (RCON<0>) | POR | — |

**Note:** All Reset flag bits may be set or cleared by the user software.

**REGISTER 8-31: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | HLVDIP2 | HLVDIP1 | HLVDIP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **HLVDIP<2:0>:** High/Low-Voltage Detect Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

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## REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| ROI | DOZE2 | DOZE1 | DOZE0 | DOZEN(1) | RCDIV2 | RCDIV1 | RCDIV0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts clear the DOZEN bit, and reset the CPU and peripheral clock ratio to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU and Peripheral Clock Ratio Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8
010 = 1:4
001 = 1:2
000 = 1:1

bit 11 **DOZEN:** Doze Enable bit(1)
1 = DOZE<2:0> bits specify the CPU and peripheral clock ratio
0 = CPU and peripheral clock ratio are set to 1:1

bit 10-8 **RCDIV<2:0>:** FRC Postscaler Select bits
When COSC<2:0> (OSCCON<14:12>) = 111:
111 = 31.25 kHz (divide-by-256)
110 = 125 kHz (divide-by-64)
101 = 250 kHz (divide-by-32)
100 = 500 kHz (divide-by-16)
011 = 1 MHz (divide-by-8)
010 = 2 MHz (divide-by-4)
001 = 4 MHz (divide-by-2) – default
000 = 8 MHz (divide-by-1)
When COSC<2:0> (OSCCON<14:12>) = 110:
111 = 1.95 kHz (divide-by-256)
110 = 7.81 kHz (divide-by-64)
101 = 15.62 kHz (divide-by-32)
100 = 31.25 kHz (divide-by-16)
011 = 62.5 kHz (divide-by-8)
010 = 125 kHz (divide-by-4)
001 = 250 kHz (divide-by-2) – default
000 = 500 kHz (divide-by-1)

bit 7-0 **Unimplemented:** Read as ‘0’

**Note 1:** This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

#### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum $V_{IH}$ specification.

### 11.2 Configuring Analog Port Pins

The use of the ANSx and TRISx registers controls the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level ($V_{OH}$ or $V_{OL}$) will be converted.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

#### 11.2.1 ANALOG SELECTION REGISTER

I/O pins with shared analog functionality, such as A/D inputs and comparator inputs, must have their digital inputs shut off when analog functionality is used. Note that analog functionality includes an analog voltage being applied to the pin externally.

To allow for analog control, the ANSx registers are provided. There is one ANSx register for each port (ANSA, ANSB and ANSC). Within each ANSx register, there is a bit for each pin that shares analog functionality with the digital I/O functionality.

If a particular pin does not have an analog function, that bit is unimplemented. See Register 11-1 to Register 11-3 for implementation.

**REGISTER 11-1: ANSA: PORTA ANALOG SELECTION REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | ANSA4[(1)] | ANSA3 | ANSA2 | ANSA1 | ANSA0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **ANSA<4:0>:** Analog Select Control bits[(1)]
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

**Note 1:** The ANSA4 bit is not available on 20-pin devices.

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## 13.2 General Purpose Timer

Timer mode is selected when CCSEL = `0` and MOD<3:0> = `0000`. The timer can function as a 32-bit timer or a dual 16-bit timer, depending on the setting of the T32 bit (Table 13-2).

**TABLE 13-2: TIMER OPERATION MODE**

| T32 (CCPxCON1L<5>) | Operating Mode |
|---|---|
| `0` | Dual Timer Mode (16-bit) |
| `1` | Timer Mode (32-bit) |

Dual 16-Bit Timer mode provides a simple timer function with two independent 16-bit timer/counters. The primary timer uses CCPxTMRL and CCPxPRL. Only the primary timer can interact with other modules on the device. It generates the MCCPx Sync out signals for use by other MCCP modules. It can also use the SYNC<4:0> bits signal generated by other modules.

The secondary timer uses CCPxTMRH and CCPxPRH. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an Output Sync/Trigger signal like the primary time base. In Dual Timer mode, the Secondary Timer Period register, CCPxPRH, generates the MCCP Compare Event (CCPxIF) used by many other modules on the device.

The 32-Bit Timer mode uses the CCPxTMRL and CCPxTMRH registers, together, as a single 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments by one. This mode provides a simple timer function when it is important to track long time periods. Note that the T32 bit (CCPxCON1L<5>) should be set before the CCPxTMRL or CCPxPRH registers are written to initialize the 32-bit timer.

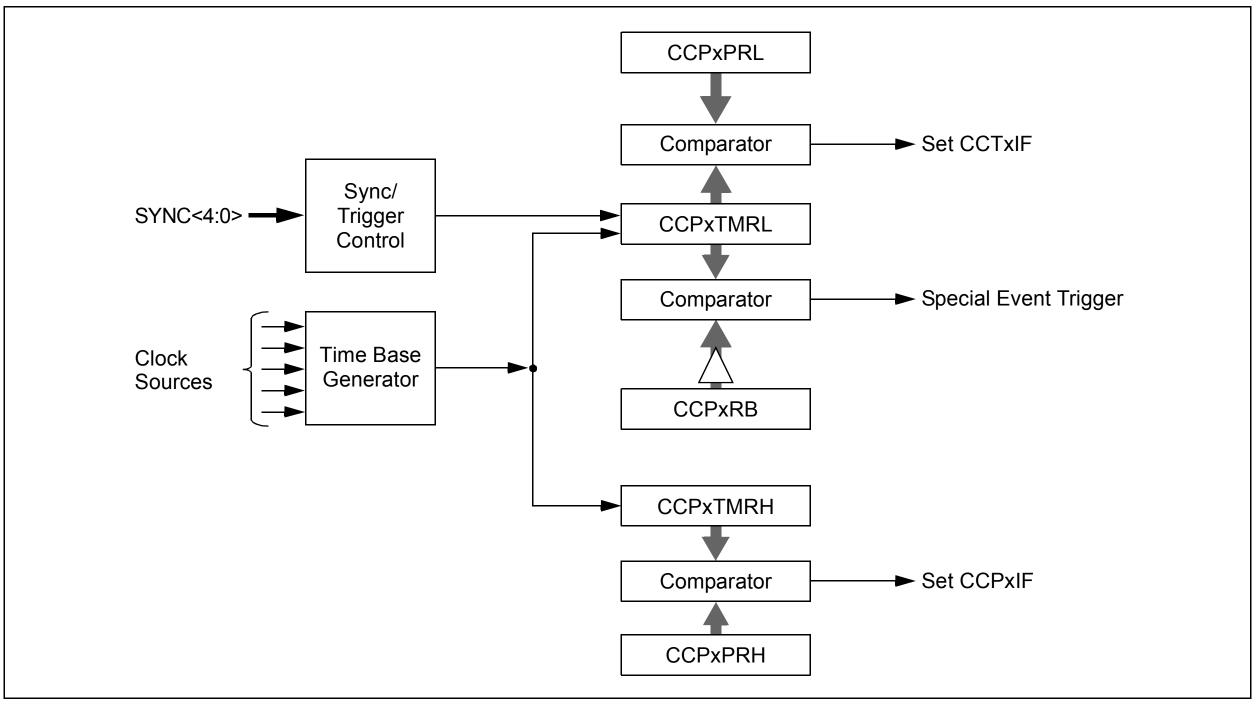
### 13.2.1 SYNC AND TRIGGER OPERATION

In both 16-bit and 32-bit modes, the timer can also function in either Synchronization ("Sync") or Trigger operation. Both use the SYNC<4:0> bits (CCPxCON1H<4:0>) to determine the input signal source. The difference is how that signal affects the timer.

In Sync operation, the timer Reset or clear occurs when the input selected by SYNC<4:0> is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H<7>) is cleared. SYNC<4:0> can have any value except '`11111`'.

In Trigger operation, the timer is held in Reset until the input selected by SYNC<4:0> is asserted; when it occurs, the timer starts counting. Trigger operation is used whenever the TRIGEN bit is set. In Trigger mode, the timer will continue running after a Trigger event as long as the CCPTRIG bit (CCPxSTATL< 7>) is set. To clear CCPTRIG, the TRCLR bit (CCPxSTATL<5>) must be set to clear the Trigger event, reset the timer and hold it at zero until another Trigger event occurs. On PIC24FV16KM204 family devices, Trigger operation can only be used when the system clock is the time base source (CLKSEL<2:0> = `000`).

**FIGURE 13-3: DUAL 16-BIT TIMER MODE**

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## 13.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal Trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 13-6 depicts a simplified block diagram of Input Capture mode.

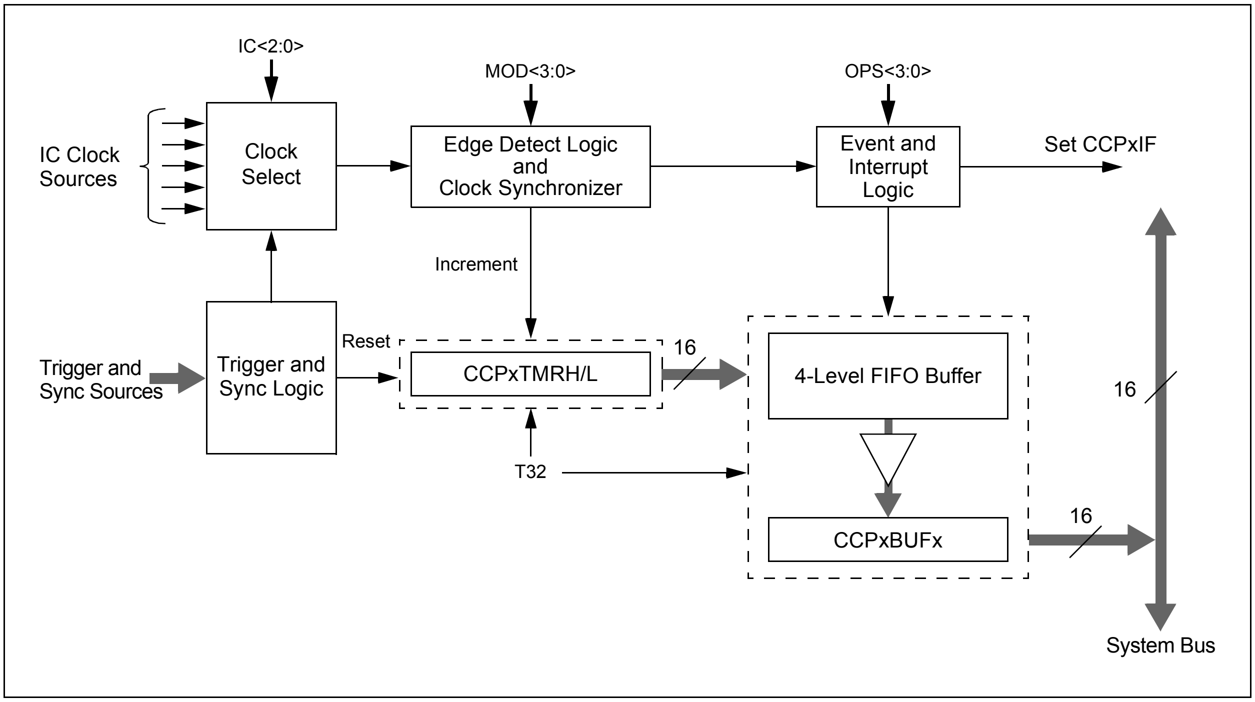
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and the MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 13-4.

**TABLE 13-4: INPUT CAPTURE MODES**

| MOD<3:0> (CCPxCON1L<3:0>) | T32 (CCPxCON1L<5>) | Operating Mode |
|---|---|---|
| 0000 | 0 | Edge Detect (16-bit capture) |
| 0000 | 1 | Edge Detect (32-bit capture) |
| 0001 | 0 | Every Rising (16-bit capture) |
| 0001 | 1 | Every Rising (32-bit capture) |
| 0010 | 0 | Every Falling (16-bit capture) |
| 0010 | 1 | Every Falling (32-bit capture) |
| 0011 | 0 | Every Rise/Fall (16-bit capture) |
| 0011 | 1 | Every Rise/Fall (32-bit capture) |
| 0100 | 0 | Every 4th Rising (16-bit capture) |
| 0100 | 1 | Every 4th Rising (32-bit capture) |
| 0101 | 0 | Every 16th Rising (16-bit capture) |
| 0101 | 1 | Every 16th Rising (32-bit capture) |

**FIGURE 13-6: INPUT CAPTURE x BLOCK DIAGRAM**





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### REGISTER 14-6: SSPxCON3: MSSPx CONTROL REGISTER 3 (SPI MODE)

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACKTIM | PCIE | SCIE | BOEN(1) | SDAHT | SBCDE | AHEN | DHEN |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ACKTIM:** Acknowledge Time Status bit ($I^2C$™ mode only)
Unused in SPI mode.

bit 6 **PCIE**: Stop Condition Interrupt Enable bit ($I^2C$ mode only)
Unused in SPI mode.

bit 5 **SCIE**: Start Condition Interrupt Enable bit ($I^2C$ mode only)
Unused in SPI mode.

bit 4 **BOEN:** Buffer Overwrite Enable bit(1)
<u>In SPI Slave mode:</u>
1 = SSPxBUF updates every time that a new data byte is shifted in, ignoring the BF bit
0 = If a new byte is received with the BF bit of the SSPxSTAT register already set, the SSPOV bit of the SSPxCON1 register is set and the buffer is not updated

bit 3 **SDAHT:** SDAx Hold Time Selection bit ($I^2C$ mode only)
Unused in SPI mode.

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit ($I^2C$ Slave mode only)
Unused in SPI mode.

bit 1 **AHEN:** Address Hold Enable bit ($I^2C$ Slave mode only)
Unused in SPI mode.

bit 0 **DHEN:** Data Hold Enable bit (Slave mode only)
Unused in SPI mode.

**Note 1:** For Daisy-Chained SPI Operation: Allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.


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# 16.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

| **Note:** | This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"PIC24F Family Reference Manual"*, **"Real-Time Clock and Calendar (RTCC)"** (DS39696). |
|---|---|

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

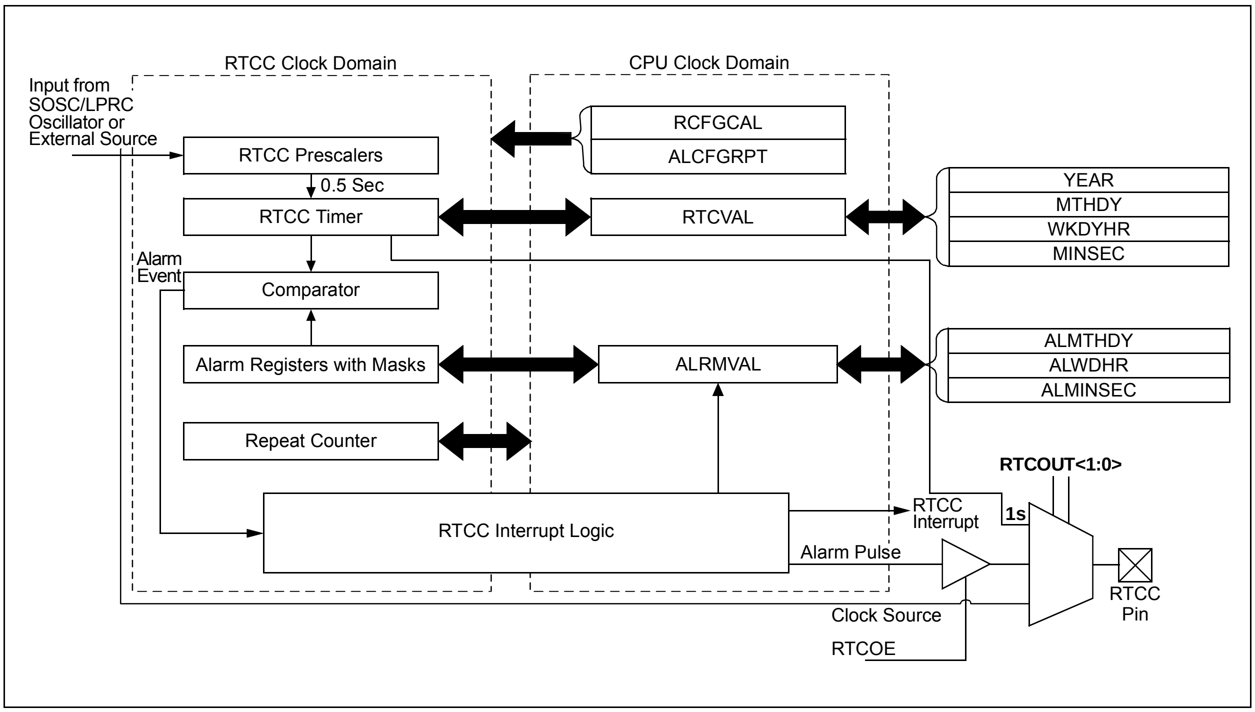
Key features of the RTCC module are:

- Operates in Sleep and Retention Sleep modes
- Selectable clock source
- Provides hours, minutes and seconds using 24-hour format
- Visibility of one half second period
- Provides calendar – weekday, date, month and year
- Alarm-configurable for half a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month or one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat chime
- Year 2000 to 2099 leap year correction
- BCD format for smaller software overhead
- Optimized for long term battery operation
- User calibration of the 32.768 kHz clock crystal/32K INTRC frequency with periodic auto-adjust
- Optimized for long term battery operation
- Fractional second synchronization
- Calibration to within ±2.64 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Ability to periodically wake-up external devices without CPU intervention (external power control)
- Power control output for external circuit control
- Calibration takes effect every 15 seconds
- Runs from any one of the following:
  - External Real-Time Clock of 32.768 kHz
  - Internal 31.25 kHz LPRC Clock
  - 50 Hz or 60 Hz External Input

## 16.1 RTCC Source Clock

The user can select between the SOSC crystal oscillator, LPRC internal oscillator or an external 50 Hz/60 Hz power line input as the clock reference for the RTCC module. This gives the user an option to trade off system cost, accuracy and power consumption, based on the overall system needs.

**FIGURE 16-1: RTCC BLOCK DIAGRAM**



To perform an A/D conversion:

1. Configure the A/D module:
   a) Configure the port pins as analog inputs and/or select band gap reference inputs (ANSx registers).
   b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2<15:13>).
   c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   d) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   e) Configure the MODE12 bit to select A/D resolution (AD1CON1<10>).
   f) Select how conversion results are presented in the buffer (AD1CON1<9:8>).
   g) Select the interrupt rate (AD1CON2<6:2>).
   h) Turn on the A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit.
   b) Select the A/D interrupt priority.

To perform an A/D sample and conversion using Threshold Detect scanning:

1. Configure the A/D module:
   a) Configure the port pins as analog inputs (ANSx registers).
   b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2<15:13>).
   c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   d) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   e) Configure the MODE12 bit to select A/D resolution (AD1CON1<10>).
   f) Select how the conversion results are presented in the buffer (AD1CON1<9:8>).
   g) Select the interrupt rate (AD1CON2<6:2>).
2. Configure the threshold compare channels:
   a) Enable auto-scan; set the ASEN bit (AD1CON5<15>).
   b) Select the Compare mode, “Greater Than, Less Than or Windowed”; set the CMx bits (AD1CON5<1:0>).
   c) Select the threshold compare channels to be scanned (AD1CSSH, AD1CSSL).
   d) If the CTMU is required as a current source for a threshold compare channel, enable the corresponding CTMU channel (AD1CTMENH, AD1CTMENL).
   e) Write the threshold values into the corresponding ADC1BUFx registers.
   f) Turn on the A/D module (AD1CON1<15>).

| | |
|---|---|
| **Note:** | If performing an A/D sample and conversion, using Threshold Detect in Sleep Mode, the RC A/D clock source must be selected before entering into Sleep mode. |

3. Configure the A/D interrupt (OPTIONAL):
   a) Clear the AD1IF bit.
   b) Select the A/D interrupt priority.

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## 25.0 SPECIAL FEATURES

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Watchdog Timer, High-Level Device Integration and Programming Diagnostics, refer to the individual sections of the *"PIC24F Family Reference Manual"* provided below:
> - **"Watchdog Timer (WDT)"** (DS39697)
> - **"Programming and Diagnostics"** (DS39716)

PIC24FXXXXX family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

## 25.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped, starting at program memory location, F80000h. A complete list of Configuration register locations is provided in Table 25-1. A detailed explanation of the various bit functions is provided in Register 25-1 through Register 25-9.

The address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using Table Reads and Table Writes.

**TABLE 25-1: CONFIGURATION REGISTERS LOCATIONS**

| Configuration Register | Address |
|---|---|
| FBS | F80000 |
| FGS | F80004 |
| FOSCSEL | F80006 |
| FOSC | F80008 |
| FWDT | F8000A |
| FPOR | F8000C |
| FICD | F8000E |

**REGISTER 25-1: FBS: BOOT SEGMENT CONFIGURATION REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | BSS2 | BSS1 | BSS0 | BWRP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-4 **Unimplemented:** Read as '0'

bit 3-1 **BSS<2:0>:** Boot Segment Program Flash Code Protection bits
111 = No boot program Flash segment
011 = Reserved
110 = Standard security, boot program Flash segment starts at 200h, ends at 000AFEh
010 = High-security, boot program Flash segment starts at 200h, ends at 000AFEh
101 = Standard security, boot program Flash segment starts at 200h, ends at 0015FEh(1)
001 = High-security, boot program Flash segment starts at 200h, ends at 0015FEh(1)
100 = Reserved
000 = Reserved

bit 0 **BWRP:** Boot Segment Program Flash Write Protection bit
1 = Boot Segment may be written
0 = Boot Segment is write-protected

**Note 1:** This selection should not be used in PIC24FV08KMXXX devices.

### REGISTER 25-9: DEVREV: DEVICE REVISION REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R | R | R | R |
|---|---|---|---|---|---|---|---|
| — | — | — | — | REV3 | REV2 | REV1 | REV0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

| | |
|---|---|
| bit 23-4 | **Unimplemented:** Read as ‘0’ |
| bit 3-0 | **REV<3:0>:** Minor Revision Identifier bits |


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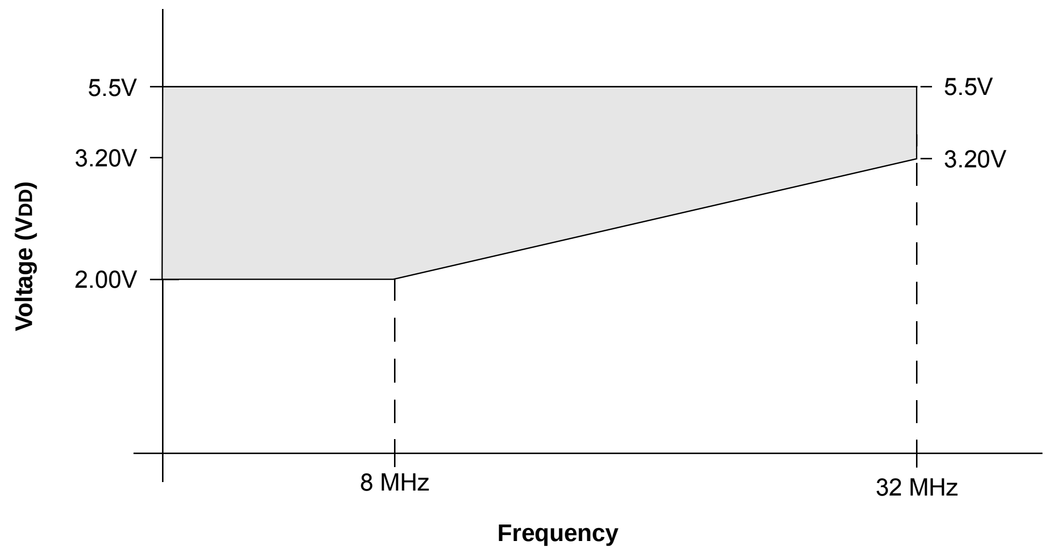
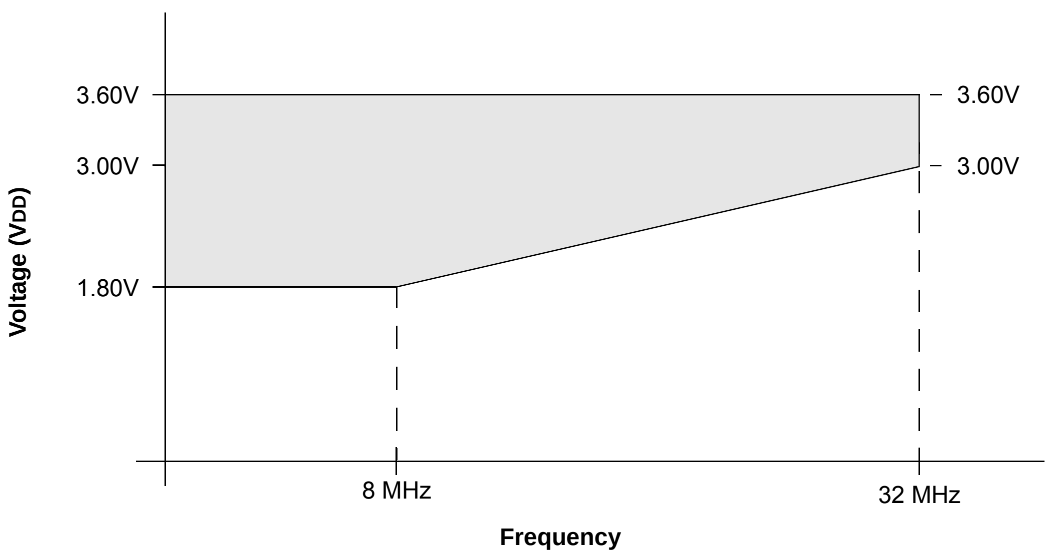
## 27.1 DC Characteristics

FIGURE 27-1: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)




**Note:** For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 2.0) + 8 MHz.

FIGURE 27-2: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)




**Note:** For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 1.8) + 8 MHz.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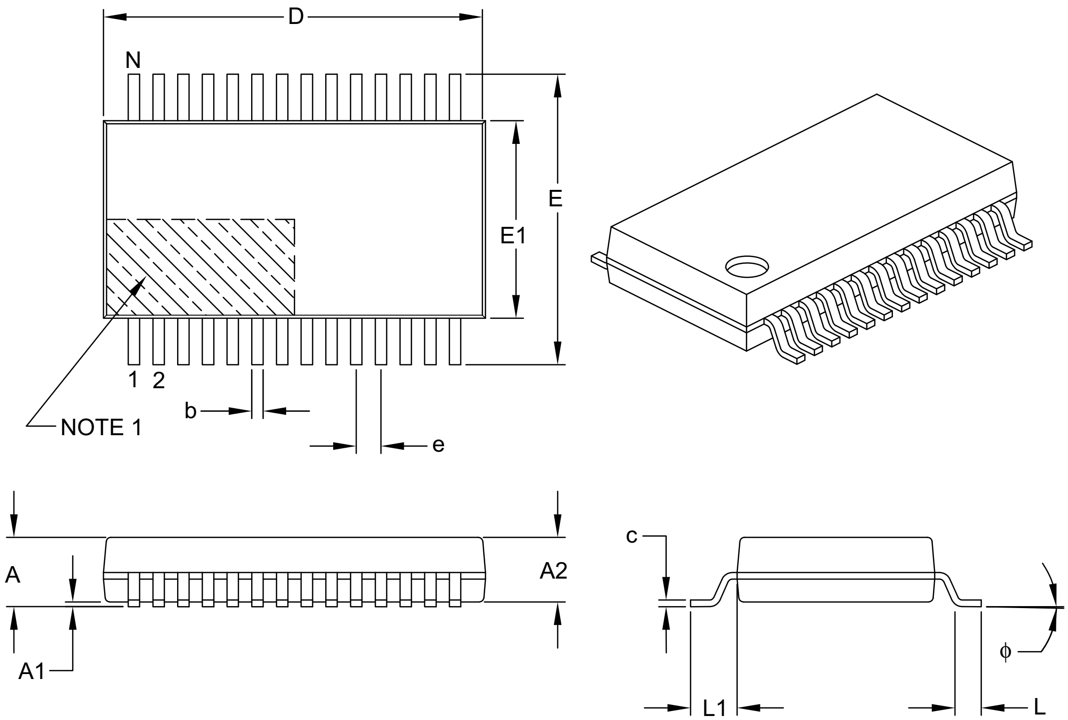
## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




| | | Units | MILLIMETERS | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B