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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km202-e-sp

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CTED1	11	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	CTMU Trigger Edge Inputs
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	CTMU Trigger Edge Inputs
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	CTMU Trigger Edge Inputs
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	CTMU Trigger Edge Inputs
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	CTMU Trigger Edge Inputs
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	CTMU Trigger Edge Inputs
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	CTMU Trigger Edge Inputs
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	CTMU Trigger Edge Inputs
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	CTMU Trigger Edge Inputs
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	CTMU Trigger Edge Inputs
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	CTMU Trigger Edge Inputs
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	CTMU Trigger Edge Inputs
CTPLS	16	24	21	11	12	16	24	21	11	12	O	—	CTMU Pulse Output
CVREF	17	25	22	14	15	17	25	22	14	15	O	ANA	Comparator Voltage Reference Output
CVREF+	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Voltage Reference Positive Input
CVREF-	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Voltage Reference Negative Input
DAC1OUT	—	23	20	10	11	—	23	20	10	11	O	ANA	DAC1 Output
DAC1REF+	—	2	27	19	21	—	2	27	19	21	I	ANA	DAC1 Positive Voltage Reference Input
DAC2OUT	—	25	22	14	15	—	25	22	14	15	O	ANA	DAC2 Output
DAC2REF+	—	26	23	15	16	—	26	23	15	16	I	ANA	DAC2 Positive Voltage Reference Input
HLVDIN	15	23	20	10	11	15	23	20	10	11	I	ANA	External High/Low-Voltage Detect Input
IC1	14	19	16	6	6	11	19	16	6	6	I	ST	MCCP1 Input Capture Input
IC2	13	18	15	1	1	13	18	15	1	1	I	ST	MCCP2 Input Capture Input
IC3	—	23	20	13	14	—	23	20	13	14	I	ST	MCCP3 Input Capture Input
IC4	—	14	11	5	5	—	14	11	5	5	I	ST	SCCP4 Input Capture Input
IC5	—	15	12	12	13	—	15	12	12	13	I	ST	SCCP5 Input Capture Input
INT0	11	16	13	43	47	11	16	13	43	47	I	ST	External Interrupt 0 Input
INT1	17	25	22	14	15	17	25	22	14	15	I	ST	External Interrupt 1 Input
INT2	14	20	17	7	7	15	23	20	10	11	I	ST	External Interrupt 2 Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C^TM = I^2C/SMBus$ input buffer

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2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

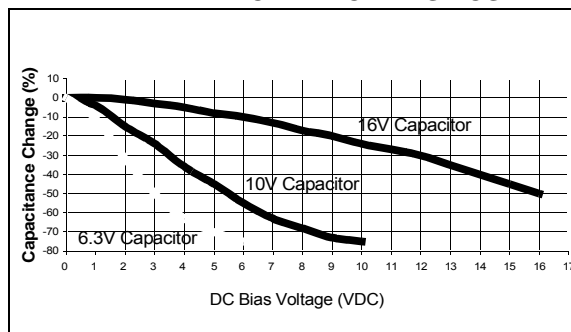
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as $\pm 10\%$ to $\pm 20\%$ (X5R and X7R), or $-20\%/+80\%$ (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: $\pm 15\%$ over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of $+22\%/ -82\%$. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 3.3V or 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100 Ω .

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pins, Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 26.0 "Development Support"**.

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to for **Section 9.0 “Oscillator Configuration”** details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals, in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

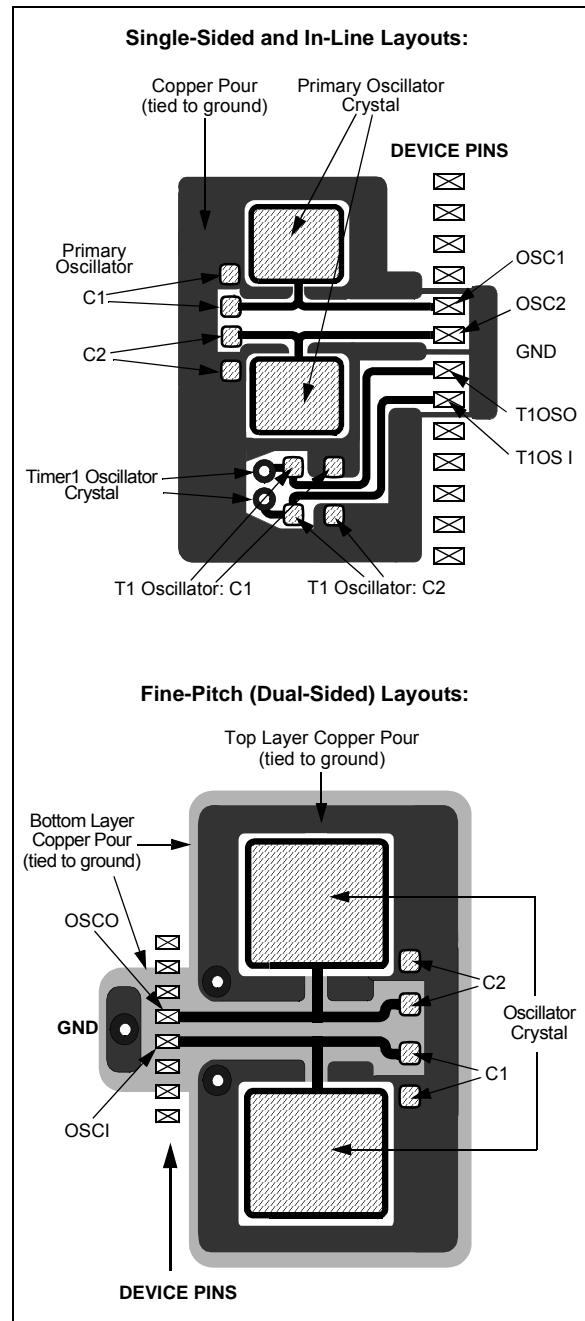


TABLE 4-3: CPU CORE REGISTERS MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
WREG0	0h	WREG0																0000
WREG1	2h	WREG1																0000
WREG2	4h	WREG2																0000
WREG3	6h	WREG3																0000
WREG4	8h	WREG4																0000
WREG5	Ah	WREG5																0000
WREG6	Ch	WREG6																0000
WREG7	Eh	WREG7																0000
WREG8	10h	WREG8																0000
WREG9	12h	WREG9																0000
WREG10	14h	WREG10																0000
WREG11	16h	WREG11																0000
WREG12	18h	WREG12																0000
WREG13	1Ah	WREG13																0000
WREG14	1Ch	WREG14																0000
WREG15	1Eh	WREG15																0800
SPLIM	20h	SPLIM Register																xxxx
PCL	2Eh	PCL Register																0000
PCH	30h	—	—	—	—	—	—	—	—	PCH7	PCH6	PCH5	PCH4	PCH3	PCH2	PCH1	PCH0	0000
TBLPAG	32h	—	—	—	—	—	—	—	—	TBLPAG7	TBLPAG6	TBLPAG5	TBLPAG4	TBLPAG3	TBLPAG2	TBLPAG1	TBLPAG0	0000
PSVPAG	34h	—	—	—	—	—	—	—	—	PSVPAG7	PSVPAG6	PSVPAG5	PSVPAG4	PSVPAG3	PSVPAG2	PSVPAG1	PSVPAG0	0000
RCOUNT	36h	RCOUNT Register																xxxx
SR	42h	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	44h	—	—	—	—	—	—	—	—	—	—	—	—	IPL3	PSV	—	—	0000
DISICNT	52h	—	—	DISICNT13	DISICNT12	DISICNT11	DISICNT10	DISICNT9	DISICNT8	DISICNT7	DISICNT6	DISICNT5	DISICNT4	DISICNT3	DISICNT2	DISICNT1	DISICNT0	xxxx

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

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6.4.1.1 Data EEPROM Bulk Erase

To erase the entire data EEPROM (bulk erase), the address registers do not need to be configured because this operation affects the entire data EEPROM. The following sequence helps in performing a bulk erase:

1. Configure NVMCON to Bulk Erase mode.
2. Clear the NVMIF status bit and enable the NVM interrupt (optional).
3. Write the key sequence to NVMKEY.
4. Set the WR bit to begin the erase cycle.
5. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical bulk erase sequence is provided in Example 6-3.

6.4.2 SINGLE-WORD WRITE

To write a single word in the data EEPROM, the following sequence must be followed:

1. Erase one data EEPROM word (as mentioned in the previous section) if the PGONLY bit (NVMCON<12>) is set to '1'.
2. Write the data word into the data EEPROM latch.
3. Program the data word into the EEPROM:
 - Configure the NVMCON register to program one EEPROM word (NVMCON<5:0> = 0001xx).
 - Clear the NVMIF status bit and enable the NVM interrupt (optional).
 - Write the key sequence to NVMKEY.
 - Set the WR bit to begin the erase cycle.
 - Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).
 - To get cleared, wait until NVMIF is set.

A typical single-word write sequence is provided in Example 6-4.

EXAMPLE 6-3: DATA EEPROM BULK ERASE

```
// Set up NVMCON to bulk erase the data EEPROM
NVMCON = 0x4050;

// Disable Interrupts For 5 Instructions
asm volatile ("disi #5");

// Issue Unlock Sequence and Start Erase Cycle
__builtin_write_NVM();
```

EXAMPLE 6-4: SINGLE-WORD WRITE TO DATA EEPROM

```
int __attribute__((space(eedata))) eeData = 0x1234;
int newData; // New data to write to EEPROM
/*-----
The variable eeData must be a Global variable declared outside of any method
the code following this comment can be written inside the method that will execute the write
-----*/
unsigned int offset;

// Set up NVMCON to erase one word of data EEPROM
NVMCON = 0x4004;

// Set up a pointer to the EEPROM location to be erased
TBLPAG = __builtin_tblpage(&eeData); // Initialize EE Data page pointer
offset = __builtin_tbloffset(&eeData); // Initizlize lower word of address
__builtin_tblwtl(offset, newData); // Write EEPROM data to write latch

asm volatile ("disi #5"); // Disable Interrupts For 5 Instructions
__builtin_write_NVM(); // Issue Unlock Sequence & Start Write Cycle
while(NVMCONbits.WR=1); // Optional: Poll WR bit to wait for
// write sequence to complete
```

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REGISTER 7-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
 1 = WDT time-out has occurred
 0 = WDT time-out has not occurred
- bit 3 **SLEEP:** Wake-up from Sleep Flag bit
 1 = Device has been in Sleep mode
 0 = Device has not been in Sleep mode
- bit 2 **IDLE:** Wake-up from Idle Flag bit
 1 = Device has been in Idle mode
 0 = Device has not been in Idle mode
- bit 1 **BOR:** Brown-out Reset Flag bit
 1 = A Brown-out Reset has occurred (the BOR is also set after a POR)
 0 = A Brown-out Reset has not occurred
- bit 0 **POR:** Power-on Reset Flag bit
 1 = A Power-on Reset has occurred
 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.
- 3:** This is implemented on PIC24FV16KMXXX parts only; not used on PIC24F16KMXXX devices.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSV Instruction, POR
SLEEP (RCON<3>)	PWRSV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

7.2.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after `SYSRST` is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer (OST) has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.2.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when `SYSRST` is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

7.3 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, `RCON`, will depend on the type of device Reset. The Reset value for the Oscillator Control register, `OSCCON`, will depend on the type of Reset and the programmed values of the `FNOSCx` bits in the Flash Configuration Word (`FOSCSEL<2:0>`); see Table 7-2. The `RCFGCAL` and `NVMCON` registers are only affected by a POR.

7.4 Brown-out Reset (BOR)

The PIC24FXXXXX family devices implement a BOR circuit, which provides the user several configuration and power-saving options. The BOR is controlled by the `BORV<1:0>` and `BOREN<1:0>` Configuration bits (`FPOR<6:5,1:0>`). There are a total of four BOR configurations, which are provided in Table 7-3.

The BOR threshold is set by the `BORV<1:0>` bits. If BOR is enabled (any values of `BOREN<1:0>`, except '00'), any drop of `VDD` below the set threshold point will reset the device. The chip will remain in BOR until `VDD` rises above the threshold.

If the Power-up Timer is enabled, it will be invoked after `VDD` rises above the threshold. Then, it will keep the chip in Reset for an additional time delay, `TPWRT`, if `VDD` drops below the threshold while the Power-up Timer is running. The chip goes back into a BOR and the Power-up Timer will be initialized. Once `VDD` rises above the threshold, the Power-up Timer will execute the additional time delay.

BOR and the Power-up Timer (`PWRT`) are independently configured. Enabling the Brown-out Reset does not automatically enable the `PWRT`.

7.4.1 LOW-POWER BOR (LPBOR)

The Low-Power BOR is an alternate setting for the BOR, designed to consume minimal power. In LPBOR mode, `BORV<1:0>` (`FPOR<6:5>`) = 00. The BOR trip point is approximately 2.0V. Due to the low current consumption, the accuracy of the LPBOR mode can vary.

Unlike the other BOR modes, LPBOR mode will not cause a device Reset when `VDD` drops below the trip point. Instead, it re-arms the POR circuit to ensure that the device will reset properly in the event that `VDD` continues to drop below the minimum operating voltage.

The device will continue to execute code when `VDD` is below the level of the LPBOR trip point. A device that requires falling edge BOR protection to prevent code from improperly executing should use one of the other BOR voltage settings.

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REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0, HSC	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽²⁾	PSV ⁽¹⁾	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15-4 **Unimplemented:** Read as '0'
- bit 3 **IPL3:** CPU Interrupt Priority Level Status bit⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less
- bit 1-0 **Unimplemented:** Read as '0'

- Note 1:** See Register 3-2 for the description of this bit, which is not dedicated to interrupt control functions.
- 2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

Note: Bit 2 is described in **Section 3.0 “CPU”**.

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NOTES:

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REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1 ⁽¹⁾	TECS0 ⁽¹⁾
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TON:** Timer1 On bit
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Select bits⁽¹⁾
11 = Reserved; do not use
10 = Timer1 uses the LPRC as the clock source
01 = Timer1 uses the External Clock (EC) from T1CK
00 = Timer1 uses the Secondary Oscillator (SOSC) as the clock source
- bit 7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronizes External Clock input
0 = Does not synchronize External Clock input
When TCS = 0:
This bit is ignored.
- bit 1 **TCS:** Timer1 Clock Source Select bit
1 = Timer1 clock source is selected by TECS<1:0>
0 = Internal clock (FOSC/2)
- bit 0 **Unimplemented:** Read as '0'

Note 1: The TECSx bits are valid only when TCS = 1.

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13.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base, using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 13-2.

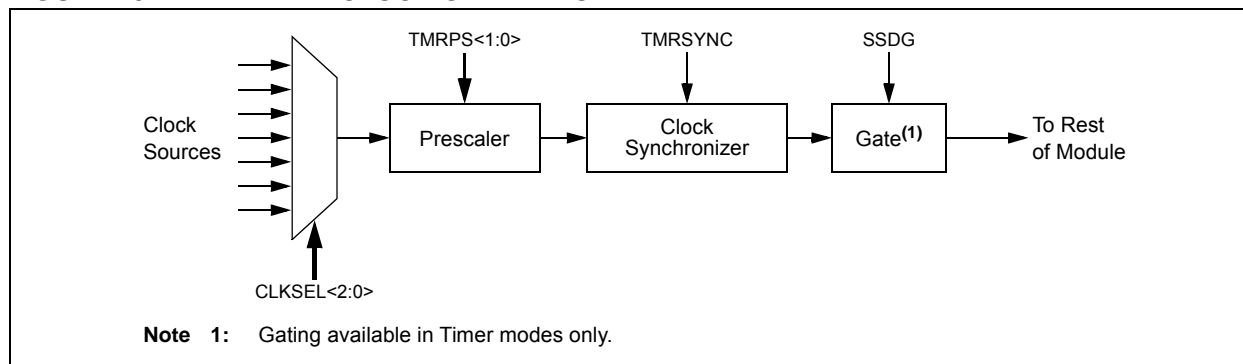
There are eight inputs available to the clock generator, which are selected using the CLKSEL<2:0> bits (CCPxCON1L<10:8>). Available sources include the FRC and LPRC, the Secondary Oscillator, and the TCLKI External Clock inputs. The system clock is the default source (CLKSEL<2:0> = 000). On PIC24FV16KM204 family devices, clock sources to the MCCPx module must be synchronized with the system clock; as a result, when clock sources are selected, clock input timing restrictions or module operating restrictions may exist. Table 13-1 describes which time base sources are valid for the various operating modes.

TABLE 13-1: VALID TIMER OPTIONS FOR MCCPx/SCCPx MODES

CLKSEL<2:0> ⁽¹⁾	Timer		Input Capture	Output Compare
	Sync ⁽²⁾	Async ⁽³⁾		
111	X	—	—	—
110	X	—	—	—
101	X	—	—	—
011	X	—	—	—
010	X	—	—	—
001	X	—	—	—
000 ⁽⁴⁾	—	X	X	X

- Note 1:** See Register 13-1 for the description of the time base sources.
- 2:** Synchronous Operation: TMRSYNC (CCPxCON1L<11>) = 1 and TRIGEN (CCPxCON1H<7>) = 0.
- 3:** Asynchronous Operation: (TMRSYNC = 0) or Triggered mode (TRIGEN = 1).
- 4:** When CLKSEL<2:0> = 000, the TMRSYNC bit must be cleared.

FIGURE 13-2: TIMER CLOCK GENERATOR



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REGISTER 14-8: SSPxADD: MSSPx SLAVE ADDRESS/BAUD RATE GENERATOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **ADD<7:0>:** Slave Address/Baud Rate Generator Value bits

SPI Master and I²C™ Master modes:

Reload value for the Baud Rate Generator. Clock period is $(([SPxADD] + 1) * 2) / F_{osc}$.

I²C Slave modes:

Represents 7 or 8 bits of the slave address, depending on the addressing mode used:

7-Bit mode: Address is ADD<7:1>; ADD<0> is ignored.

10-Bit LSb mode: ADD<7:0> are the Least Significant bits of the address.

10-Bit MSb mode: ADD<2:1> are the two Most Significant bits of the address; ADD<7:3> are always '11110' as a specification requirement; ADD<0> is ignored.

REGISTER 14-9: SSPxMSK: I²C™ SLAVE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **MSK<7:0>:** Slave Address Mask Select bits⁽¹⁾

1 = Masking of corresponding bit of SSPxADD is enabled

0 = Masking of corresponding bit of SSPxADD is disabled

Note 1: MSK0 is not used as a mask bit in 7-bit addressing.

15.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the “PIC24F Family Reference Manual”, “UART” (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler

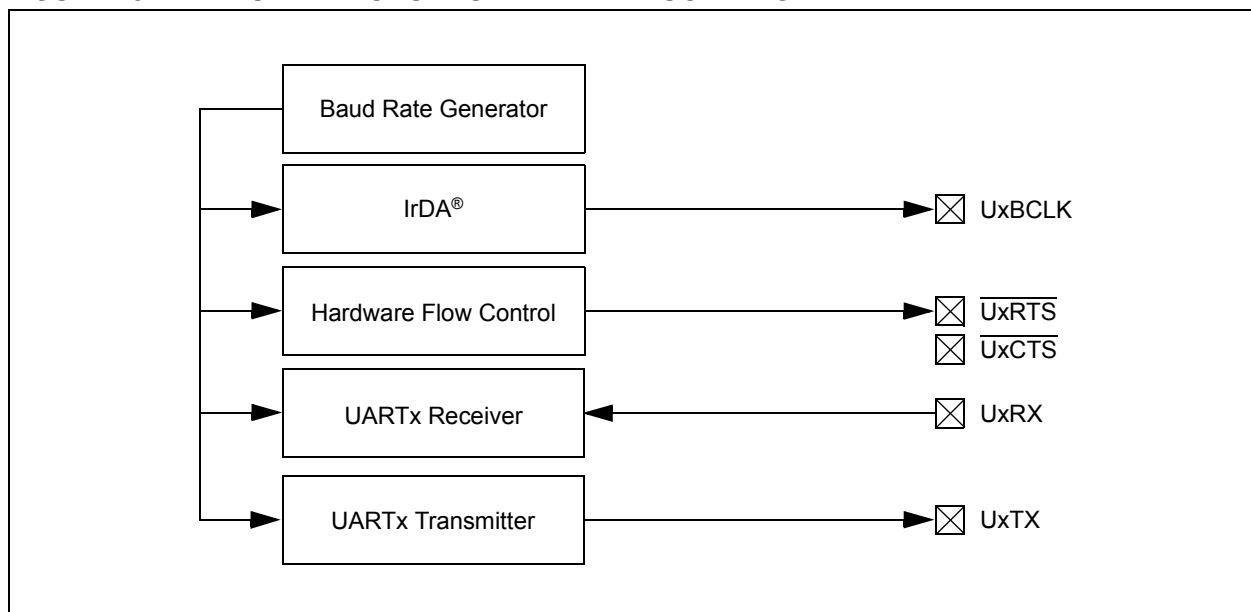
- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 15-1. The UARTx module consists of these important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific USART module are referred to generically by the use of ‘x’ in place of the specific module number. Thus, “UxSTA” might refer to the USART Status register for either USART1 or USART2.

FIGURE 15-1: UARTx MODULE SIMPLIFIED BLOCK DIAGRAM



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REGISTER 15-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	OERR: Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the empty state)
bit 0	URXDA: UARTx Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data; at least one more characters can be read 0 = Receive buffer is empty

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REGISTER 17-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>**: CLCx Mode bits

- 111 = Cell is a 1-input transparent latch with S and R
- 110 = Cell is a JK flip-flop with R
- 101 = Cell is a 2-input D flip-flop with R
- 100 = Cell is a 1-input D flip-flop with S and R
- 011 = Cell is an SR latch
- 010 = Cell is a 4-input AND
- 001 = Cell is an OR-XOR
- 000 = Cell is a AND-OR

REGISTER 17-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Polarity Control bit

- 1 = The output of Channel 4 logic is inverted when applied to the logic cell
- 0 = The output of Channel 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit

- 1 = The output of Channel 3 logic is inverted when applied to the logic cell
- 0 = The output of Channel 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit

- 1 = The output of Channel 2 logic is inverted when applied to the logic cell
- 0 = The output of Channel 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit

- 1 = The output of Channel 1 logic is inverted when applied to the logic cell
- 0 = The output of Channel 1 logic is not inverted

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REGISTER 17-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

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REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **CH0NB<2:0>**: Sample B Channel 0 Negative Input Select bits

111 = AN6⁽¹⁾

110 = AN5⁽²⁾

101 = AN4

100 = AN3

011 = AN2

010 = AN1

001 = AN0

000 = AVss

bit 12-8 **CH0SB<4:0>**: S/H Amplifier Positive Input Select for MUX B Multiplexer Setting bits

11111 = Unimplemented, do not use

11110 = AVDD⁽³⁾

11101 = AVss⁽³⁾

11100 = Upper guardband rail ($0.785 * V_{DD}$)

11011 = Lower guardband rail ($0.215 * V_{DD}$)

11010 = Internal Band Gap Reference (V_{BG})⁽³⁾

11000-11001 = Unimplemented, do not use

10001 = No channels are connected, all inputs are floating (used for CTMU)

10111 = No channels are connected, all inputs are floating (used for CTMU)

10110 = No channels are connected, all inputs are floating (used for CTMU temperature sensor input); does not require the corresponding CTMEN22 (AD1CTMENH<6>) bit)

10101 = Channel 0 positive input is AN21

10100 = Channel 0 positive input is AN20

10011 = Channel 0 positive input is AN19

10010 = Channel 0 positive input is AN18⁽²⁾

10001 = Channel 0 positive input is AN17⁽²⁾

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01001 = Channel 0 positive input is AN9

01000 = Channel 0 positive input is AN8⁽¹⁾

00111 = Channel 0 positive input is AN7⁽¹⁾

00110 = Channel 0 positive input is AN6⁽¹⁾

00101 = Channel 0 positive input is AN5⁽²⁾

00100 = Channel 0 positive input is AN4

00011 = Channel 0 positive input is AN3

00010 = Channel 0 positive input is AN2

00001 = Channel 0 positive input is AN1

00000 = Channel 0 positive input is AN0

Note 1: This is implemented on 44-pin devices only.

Note 2: This is implemented on 28-pin and 44-pin devices only.

Note 3: The band gap value used for this input is 2x or 4x the internal V_{BG}, which is selected when PVCFG<1:0> = 1x.

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TABLE 27-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KMXXX) 2.0V to 5.5V (PIC24FV16KMXXX) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	Device	Typical	Max	Units	Conditions	
IDD Current						
D20	PIC24FV16KMXXX	269	450	μA	2.0V	0.5 MIPS, Fosc = 1 MHz ⁽¹⁾
		465	830	μA	5.0V	
	PIC24F16KMXXX	200	330	μA	1.8V	
		410	750	μA	3.3V	
DC22	PIC24FV16KMXXX	490	—	μA	2.0V	1 MIPS, Fosc = 2 MHz ⁽¹⁾
		880	—	μA	5.0V	
	PIC24F16KMXXX	407	—	μA	1.8V	
		800	—	μA	3.3V	
DC24	PIC24FV16KMXXX	13.0	15.0	mA	5.0V	16 MIPS, Fosc = 32 MHz ⁽¹⁾
	PIC24F16KMXXX	12.0	13.0	mA	3.3V	
DC26	PIC24FV16KMXXX	2.0	—	mA	2.0V	FRC (4 MIPS), Fosc = 8 MHz
		3.5	—	mA	5.0V	
	PIC24F16KMXXX	1.80	—	mA	1.8V	
		3.40	—	mA	3.3V	
DC30	PIC24FV16KMXXX	48.0	250	μA	2.0V	LPRC (15.5 KIPS), Fosc = 31 kHz
		75.0	275	μA	5.0V	
	PIC24F16KMXXX	8.1	28.0	μA	1.8V	
		13.50	55.00	μA	3.3V	

Legend: Unshaded rows represent PIC24F16KMXXX devices and shaded rows represent PIC24FV16KMXXX devices.

Note 1: The oscillator is in External Clock mode (FOSCSEL<2:0> = 010, FOSC<1:0> = 00).

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FIGURE 27-19: A/D CONVERSION TIMING

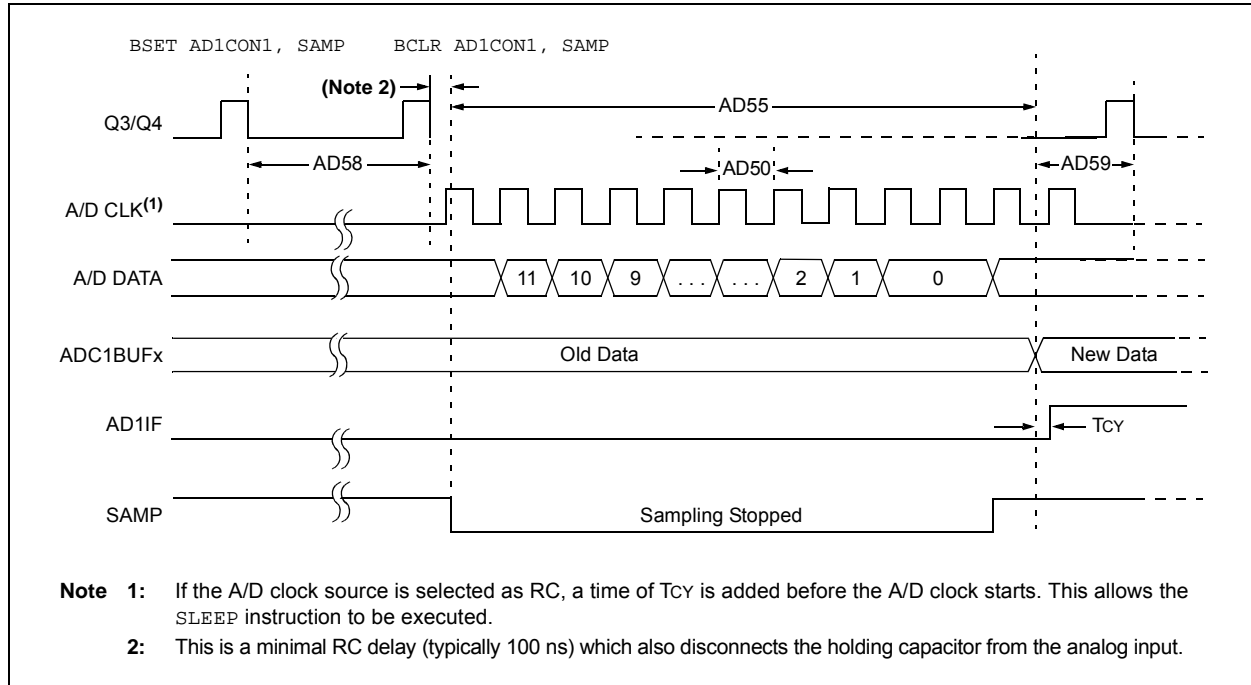


TABLE 27-38: A/D CONVERSION TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ Ta ≤ +85°C for Industrial -40°C ≤ Ta ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	A/D Clock Period	600	—	—	ns	Tcy = 75 ns, AD1CON3 in default state
AD51	TRC	A/D Internal RC Oscillator Period	—	1.67	—	μs	
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 14	—	TAD TAD	10-bit results 12-bit results
AD56	FCNV	Throughput Rate	—	—	100	ksps	
AD57	TSAMP	Sample Time	—	1	—	TAD	
AD58	TACQ	Acquisition Time	750	—	—	ns	(Note 2)
AD59	TSWC	Switching Time from Convert to Sample	—	—	(Note 3)		
AD60	TDIS	Discharge Time	12	—	—	TAD	
Clock Parameters							
AD61	TPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

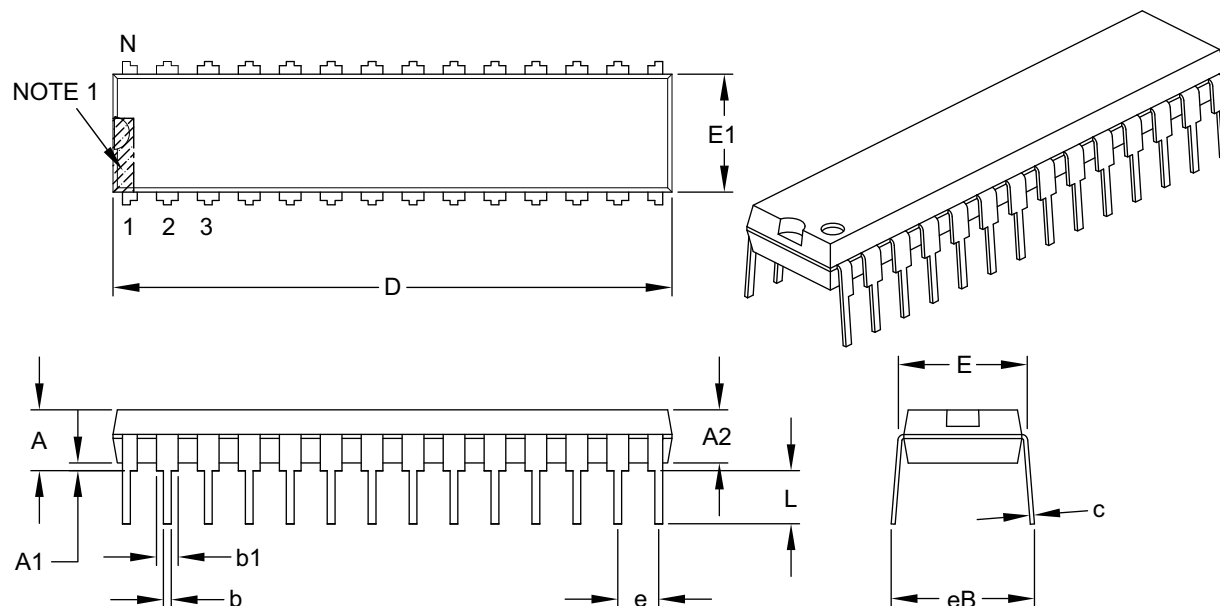
2: The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD).

3: On the following cycle of the device clock.

PIC24FV16KM204 FAMILY

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	—	—	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	—	—
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	—	—	.430

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B