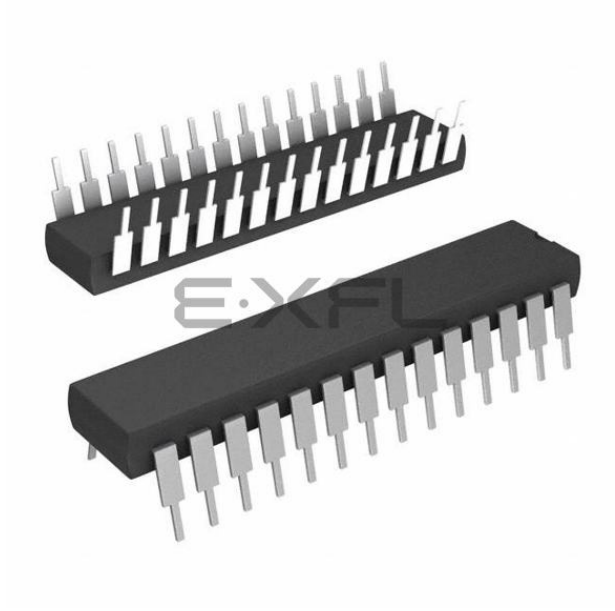

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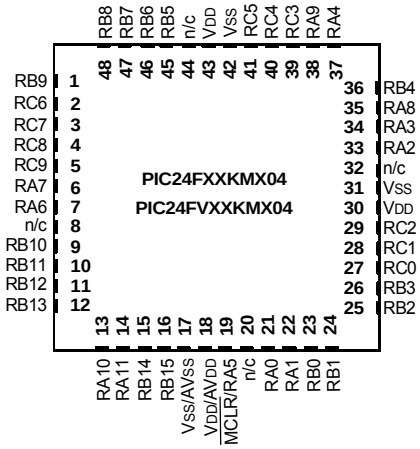
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km202-i-sp

Pin Diagrams (Continued)

48-Pin UQFN(1)



Legend: Values in indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Note 1: Exposed pad on underside of device is connected to VSS.

Pin	Pin Features	
	PIC24FXXKMX04	PIC24FVXXKMX04
1	AN21/SDA1/T1CK/U1RTS/U1BCLK/IC2/ /CLC1O/CTED4/CN21/RB9	
2	U1RX/ /CN18/RC6	
3	U1TX/ /CN17/RC7	
4	OC2/CN20/RC8	
5	IC4/OC2F/CTED7/CN19/RC9	
6	IC1/ / /CTED3/CN9/RA7	
7	/OC1A/CTED1/INT2/CN8/RA6	VDDCORE or VCAP
8	n/c	n/c
9	PGED2/SDI1/OC1C/CTED11/CN16/RB10	
10	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
11	/AN12/HLVDIN/ /CTED2/ CN14/RB12	/AN12/HLVDIN/ /CTED2/ INT2/CN14/RB12
12	/ /AN11/SDO1/OC1D/CTPLS/CN13/RB13	
13	/ /CN35/RA10	
14	/ /CTED8/CN36/RA11	
15	/CVREF/ / /AN10/ / /C1OUT/OCFA/CTED5/INT1/ CN12/RB14	
16	/ /AN9/ /REFO/SS1/TCKIA/CTED6/CN11/RB15	
17	VSS/AVSS	
18	VDD/AVDD	
19	MCLR/VPP/RA5	
20	n/c	
21	CVREF+/VREF+/ +/AN0/ / CN2/RA0	CVREF+/VREF+/ +/AN0/ / CTED1/CN2/RA0
22	CVREF-/VREF-/AN1/CN3/RA1	
23	PGED1/AN2/CTCMP/ULPWU/C1IND/ / / /CN4/RB0	
24	PGEC1/ / /AN3/C1INC/ / /CTED12/CN5/RB1	
25	/ /AN4/C1INB/ / /TCKIB/CTED13/CN6/RB2	
26	/AN5/C1INA/ / /CN7/RB3	
27	AN6/CN32/RC0	
28	AN7/CN31/RC1	
29	AN8/CN10/RC2	
30	VDD	
31	VSS	
32	n/c	
33	OSCI/AN13/CLKI/CN30/RA2	
34	OSCO/CLKO/AN14/CN29/RA3	
35	OCFB/CN33/RA8	
36	SOSCI/AN15/ / /CN1/RB4	
37	SOSCO/SCLKI/AN16/PWRLCLK/ /CN0/RA4	
38	/CN34/RA9	
39	/CN28/RC3	
40	/CN25/RC4	
41	/CN26/RC5	
42	VSS	
43	VDD	
44	n/c	
45	PGED3/AN17/ASDA1/OC1E/CLCINA/CN27/RB5	
46	PGEC3/AN18/ASCL1/OC1F/CLCINB/CN24/RB6	
47	AN19/INT0/CN23/RB7	AN19/ /OC1A/INT0/CN23/RB7
48	AN20/SCL1/U1CTS/C3OUT/OC1B/CTED10/CN22/RB8	

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1.1.4 EASY MIGRATION

The PIC24FV16KM204 family devices have two variants. The KM20X variant provides the full feature set of the device, while the KM10X offers a reduced peripheral set, allowing for the balance of features and cost (refer to Table 1-1). Both variants allow for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also helps in migrating to the next larger device. This is true when moving between devices with the same pin count, different die variants, or even moving from 20-pin or 28-pin devices to 44-pin/48-pin devices.

The PIC24F family is pin compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple to the powerful and complex, yet still selecting a Microchip device.

1.2 Other Special Features

- Communications: The PIC24FV16KM204 family incorporates a range of serial communication peripherals to handle a range of application requirements. There is an MSSP module which implements both SPI and I^2C™ protocols, and supports both Master and Slave modes of operation for each. Devices also include one of two UARTs with built-in IrDA® encoders/decoders.
- Analog Features: Select members of the PIC24FV16KM204 family include two 8-bit Digital-to-Analog Converters which offer support in Idle mode, and left and right justified input data, as well as up to two operational amplifiers with selectable power and speed modes.
- Real-Time Clock/Calendar (RTCC): This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- 12-Bit A/D Converter: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and faster sampling speed. The 16-deep result buffer can be used either in Sleep, to reduce power, or in Active mode to improve throughput.
- Charge Time Measurement Unit (CTMU) Interface: The PIC24FV16KM204 family includes the new CTMU interface module, which can be used for capacitive touch sensing, proximity sensing, and also for precision time measurement and pulse generation. The CTMU can also be connected to the operational amplifiers to provide active guarding, which provides increased robustness in the presence of noise in capacitive touch applications.

1.3 Details on Individual Family Members

Devices in the PIC24FV16KM204 family are available in 20-pin, 28-pin, 44-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1.

Members of the PIC24FV16KM204 family are available as both standard and high-voltage devices. High-voltage devices, designated with an “FV” in the part number (such as PIC24FV16KM204), accommodate an operating V_{DD} range of 2.0V to 5.5V and have an on-board voltage regulator that powers the core. Peripherals operate at V_{DD}.

Standard devices, designated by “F” (such as PIC24F16KM204), function over a lower V_{DD} range of 1.8V to 3.6V. These parts do not have an internal regulator, and both the core and peripherals operate directly from V_{DD}.

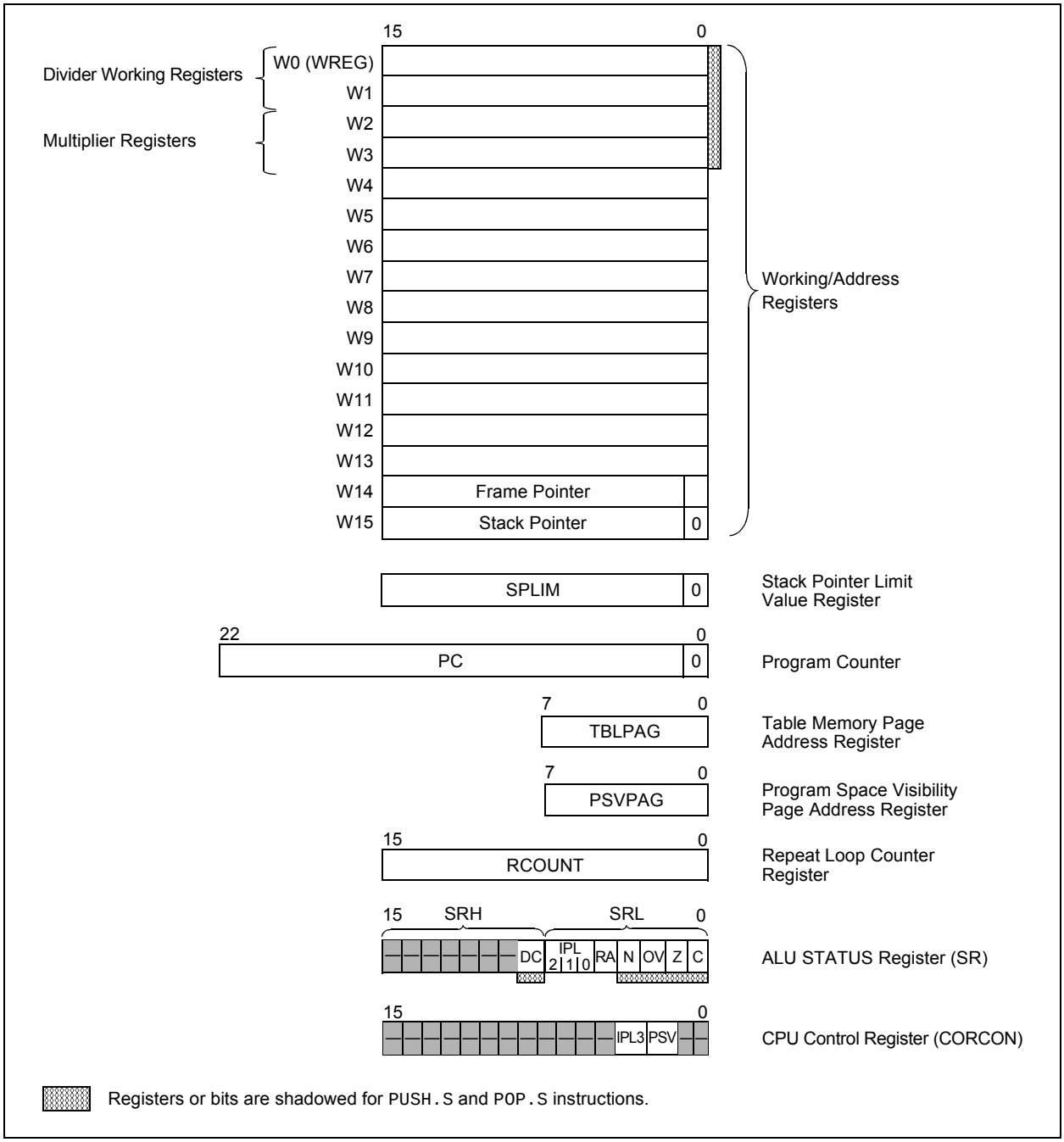
The PIC24FV16KM204 family may be thought of as two different device groups, both offering slightly different sets of features. These differ from each other in multiple ways:

- The size of the Flash program memory
- The number of external analog channels available
- The number of Digital-to-Analog Converters
- The number of operational amplifiers
- The number of analog comparators
- The presence of a Real-Time Clock and Calendar (RTCC)
- The number and type of CCP modules (i.e., MCCP vs. SCCP)
- The number of serial communication modules (both MSSPs and UARTs)
- The number of Configurable Logic Cell (CLC) modules

The general differences between the different sub-families are shown in Table 1-1 and Table 1-2.

A list of the pin features available on the PIC24FV16KM204 family devices, sorted by function, is provided in Table 1-5.

FIGURE 3-2: PROGRAMMER'S MODEL



REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
If FSCM is Enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is Disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **Unimplemented:** Read as '0'

bit 5 **LOCK:** PLL Lock Status bit(2)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **SOSCDRV**: Secondary Oscillator Drive Strength bit(3)
1 = High-power SOSC circuit is selected
0 = Low/high-power select is done via the SOSCSRC Configuration bit

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enables the Secondary Oscillator
0 = Disables the Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiates an oscillator switch to the clock source specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.
2: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
3: When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSCSRC = 0), this bit has no effect.

The following code sequence for a clock switch is recommended:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8>, in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0>, in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1 and Example 9-2.

EXAMPLE 9-1: ASSEMBLY CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON,#0
```

EXAMPLE 9-2: BASIC 'C' CODE SEQUENCE FOR CLOCK SWITCHING

```
//Use compiler built-in function to write
new clock setting
__builtin_write_OSCCONH(0x01); //0x01
switches to FRCPLL

//Use compiler built-in function to set the
OSWEN bit.
__builtin_write_OSCCONL(OSCCONL | 0x01);

//Optional: Wait for clock switch sequence
to complete
while(OSCCONbits.OSWEN == 1);
```

9.5 Reference Clock Output

In addition to the CLKO output (FOSC/2) available in certain oscillator modes, the device clock in the PIC24FXXXXX family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 9-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV<3:0> bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSC1 and OSC2, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the primary modes (EC, HS or XT); otherwise, if the ROSEL bit is not also set, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum VIH specification.

11.2 Configuring Analog Port Pins

The use of the ANSx and TRISx registers controls the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (VOH or VOL) will be converted.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

11.2.1 ANALOG SELECTION REGISTER

I/O pins with shared analog functionality, such as A/D inputs and comparator inputs, must have their digital inputs shut off when analog functionality is used. Note that analog functionality includes an analog voltage being applied to the pin externally.

To allow for analog control, the ANSx registers are provided. There is one ANSx register for each port (ANSA, ANSB and ANSC). Within each ANSx register, there is a bit for each pin that shares analog functionality with the digital I/O functionality.

If a particular pin does not have an analog function, that bit is unimplemented. See Register 11-1 to Register 11-3 for implementation.

REGISTER 11-1: ANSA: PORTA ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	ANSA4(1)	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **ANSA<4:0>:** Analog Select Control bits(1)

1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: The ANSA4 bit is not available on 20-pin devices.

13.5 Auxiliary Output

The MCCPx and SCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other MCCP or SCCP modules, or other digital peripherals, to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT<1:0> control bits (CCPxCON2H<4:3>). The type of output signal is also dependent on the module operating mode.

On the PIC24FV16KM204 family of devices, only the CTMU discharge trigger has access to the auxiliary output signal.

TABLE 13-5: AUXILIARY OUTPUT

AUXOUT<1:0>	CCSEL	MOD<3:0>	Comments	Signal Description
00	x	xxxx	Auxiliary output disabled	No Output
01	0	0000	Time Base modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

REGISTER 14-2: SSPxSTAT: MSSPx STATUS REGISTER (I^2C™ MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P(1)	S(1)	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **SMP:** Slew Rate Control bit
In Master or Slave mode:
1 = Slew rate control is disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)

bit 6 **CKE:** SMBus Select bit
In Master or Slave mode:
1 = Enables SMBus-specific inputs
0 = Disables SMBus-specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit
In Master mode:
Reserved.
In Slave mode:
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit(1)
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

bit 3 **S:** Start bit(1)
1 = Indicates that a Start bit has been detected last
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ Information bit
In Slave mode:(2)
1 = Read
0 = Write
In Master mode:(3)
1 = Transmit is in progress
0 = Transmit is not in progress

bit 1 **UA:** Update Address bit (10-Bit Slave mode only)
1 = Indicates that the user needs to update the address in the SSPxADD register
0 = Address does not need to be updated

Note 1: This bit is cleared on Reset and when SSPEN is cleared.

2: This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.

3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Active mode.

REGISTER 14-2: SSPxSTAT: MSSPx STATUS REGISTER (I^2C™ MODE) (CONTINUED)

bit 0 **BF:** Buffer Full Status bit

In Transmit mode:
1 = Transmit is in progress, SSPxBUF is full
0 = Transmit is complete, SSPxBUF is empty

In Receive mode:
1 = SSPxBUF is full (does not include the $\overline{ACK}$ and Stop bits)
0 = SSPxBUF is empty (does not include the $\overline{ACK}$ and Stop bits)

Note 1: This bit is cleared on Reset and when SSPEN is cleared.

2: This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.

3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Active mode.

FIGURE 19-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM

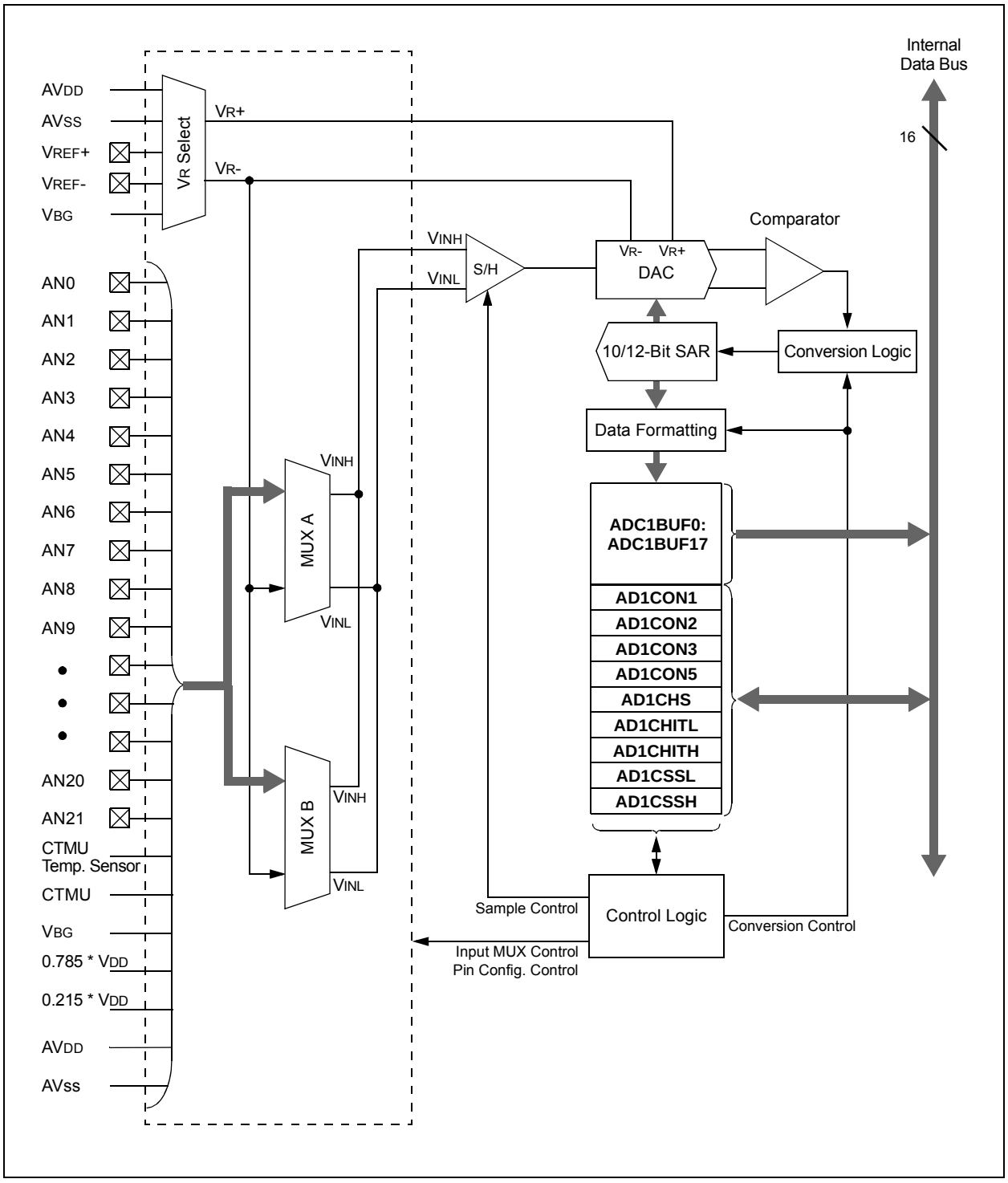


TABLE 19-4: NUMERICAL EQUIVALENTS OF VARIOUS RESULT CODES: 10-BIT FRACTIONAL FORMATS

VIN/VREF	10-Bit Differential Output Code (11-bit result)	16-Bit Fractional Format/ Equivalent Decimal Value		16-Bit Signed Fractional Format/ Equivalent Decimal Value	
+1023/1024	011 1111 1111	1111 1111 1100 0000	0.999	0111 1111 1110 0000	0.999
+1022/1024	011 1111 1110	1111 1111 1000 0000	0.998	0111 1111 1000 0000	0.998
•••					
+1/1024	000 0000 0001	0000 0000 0100 0000	0.001	0000 0000 0010 0000	0.001
0/1024	000 0000 0000	0000 0000 0000 0000	0.000	0000 0000 0000 0000	0.000
-1/1024	101 1111 1111	0000 0000 0000 0000	0.000	1111 1111 1110 0000	-0.001
•••					
-1023/1024	100 0000 0001	0000 0000 0000 0000	0.000	1000 0000 0010 0000	-0.999
-1024/1024	100 0000 0000	0000 0000 0000 0000	0.000	1000 0000 0000 0000	-1.000

REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Edge 1 source is the Comparator 3 output
1110 = Edge 1 source is the Comparator 2 output
1101 = Edge 1 source is the Comparator 1 output
1100 = Edge 1 source is CLC2
1011 = Edge 1 source is CLC1
1010 = Edge 1 source is the MCCP2 Compare Event (CCP2IF)
1001 = Edge 1 source is CTED8(1)
1000 = Edge 1 source is CTED7(1)
0111 = Edge 1 source is CTED6
0110 = Edge 1 source is CTED5
0101 = Edge 1 source is CTED4
0100 = Edge 1 source is CTED3(2)
0011 = Edge 1 source is CTED1
0010 = Edge 1 source is CTED2
0001 = Edge 1 source is the MCCP1 Compare Event (CCP1IF)
0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the current source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the current source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

25.4 Program Verification and Code Protection

For all devices in the PIC24FXXXXX family, code protection for the Boot Segment is controlled by the Configuration bit, BSS0, and the General Segment by the Configuration bit, GCP. These bits inhibit external reads and writes to the program memory space This has no direct effect in normal execution mode.

Write protection is controlled by bit, BWRP, for the Boot Segment and bit, GWRP, for the General Segment in the Configuration Word. When these bits are programmed to '0', internal write and erase operations to program memory are blocked.

25.5 In-Circuit Serial Programming

PIC24FXXXXX family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

25.6 In-Circuit Debugger

When MPLAB® ICD 3, MPLAB REAL ICE™ or PICkit™ 3 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx and PGEDx pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS}, PGECx, PGEDx and the pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

26.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

26.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

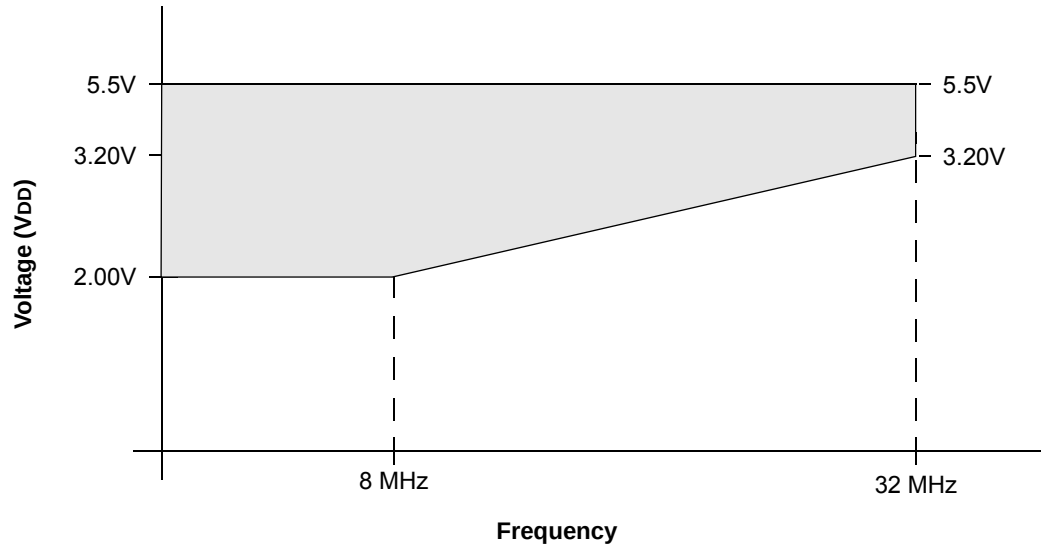
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

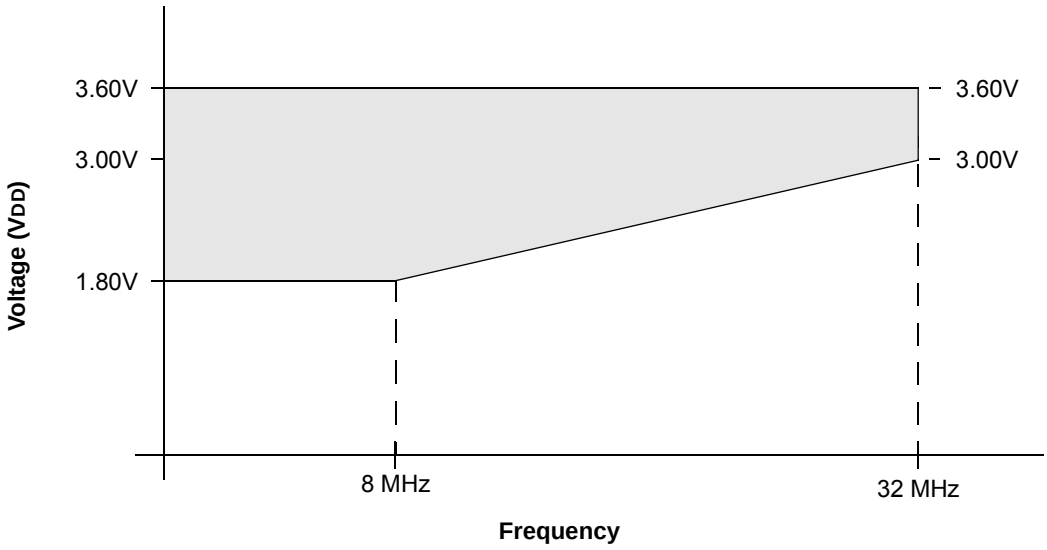
27.1 DC Characteristics

FIGURE 27-1: PIC24FV16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



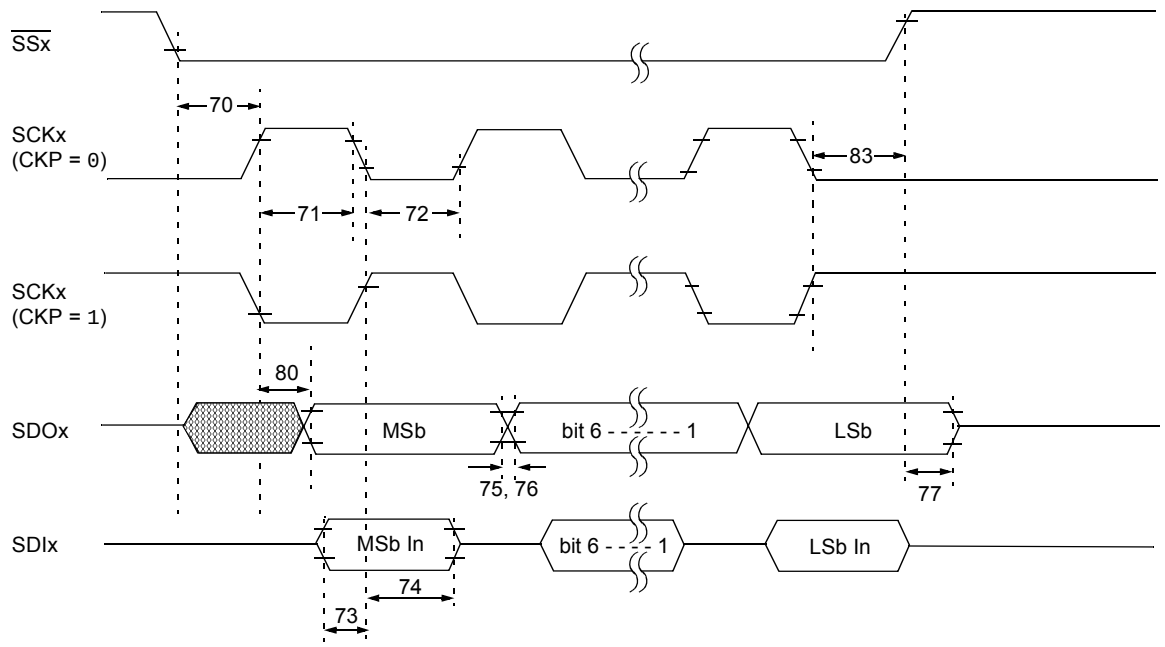
Note: For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 2.0) + 8 MHz.

FIGURE 27-2: PIC24F16KM204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note: For frequencies between 8 MHz and 32 MHz, FMAX = 20 MHz * (VDD – 1.8) + 8 MHz.

FIGURE 27-13: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)



Note: Refer to Figure 27-5 for load conditions.

TABLE 27-31: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input		3 Tcy	—	ns	
70A	TssL2WB	$\overline{SSx}$ to Write to SSPxBUF		3 Tcy	—	ns	
71	TscH	SCKx Input High Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
71A			Single Byte	40	—	ns	**(Note 1)**
72	TscL	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	—	ns	**(Note 1)**
73	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge		20	—	ns	
73A	Tb2b	Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2		1.5 Tcy + 40	—	ns	**(Note 2)**
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time		—	25	ns	
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
77	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance		10	50	ns	
80	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge		—	50	ns	
83	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge		1.5 Tcy + 40	—	ns	
	Fsck	SCKx Frequency		—	10	MHz	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameters 71A and 72A are used.

TABLE 27-34: I²C™ BUS DATA REQUIREMENTS (SLAVE MODE)

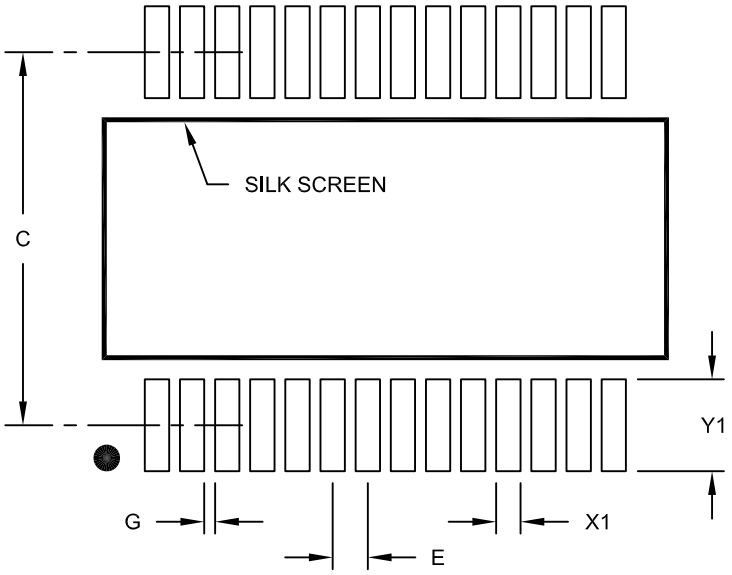
Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	4.0	—	μs	Must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Must operate at a minimum of 10 MHz
			MSSPx module	1.5 TCY	—	—	
101	TLOW	Clock Low Time	100 kHz mode	4.7	—	μs	Must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Must operate at a minimum of 10 MHz
			MSSPx module	1.5 TCY	—	—	
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 to 400 pF
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 to 400 pF
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
91	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
D102	CB	Bus Capacitive Loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode I²C™ bus device can be used in a Standard mode I²C bus system, but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A