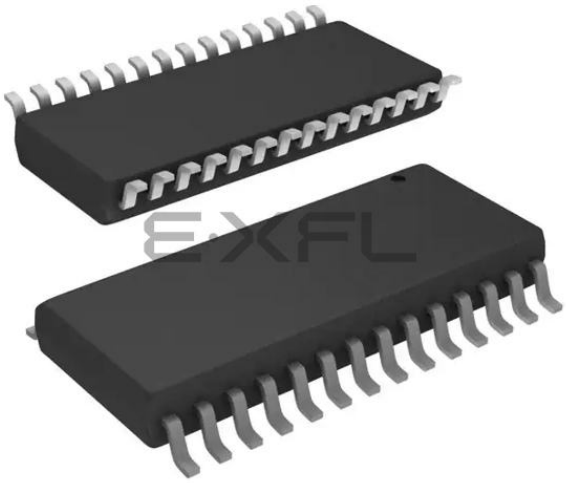


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 19x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km202t-i-so

Peripheral Features

- High-Current Sink/Source, 18 mA/18 mA All Ports
- Independent Ultra Low-Power, 32 kHz Timer Oscillator
- Up to Two Master Synchronous Serial Ports (MSSPs) with SPI and I^2C™ modes:

  In SPI mode:
  - User-configurable SCKx and SDOx pin outputs
  - Daisy-chaining of SPI slave devices

  In I^2C mode:
  - Serial clock synchronization (clock stretching)
  - Bus collision detection and will arbitrate accordingly
  - Support for 16-bit read/write interface
- Up to Two Enhanced Addressable UARTs:
  - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect, Break character support)
  - High and low speed (SCI)
  - IrDA® mode (hardware encoder/decoder function)
- Two External Interrupt Pins
- Hardware Real-Time Clock and Calendar (RTCC)
- Configurable Reference Clock Output (REFO)
- Two Configurable Logic Cells (CLC)
- Up to Two Single Output Capture/Compare/PWM (SCCP) modules and up to Three Multiple Output Capture/Compare/PWM (MCCP) modules

Special Microcontroller Features

- Wide Operating Voltage Range Options:
  - 1.8V to 3.6V (PIC24F devices)
  - 2.0V to 5.0V (PIC24FV devices)
- Selectable Power Management modes:
  - Idle: CPU shuts down, allowing for significant power reduction
  - Sleep: CPU and peripherals shut down for substantial power reduction and fast wake-up
  - Retention Sleep mode: PIC24FV devices can enter Sleep mode, employing the Retention Regulator, further reducing power consumption
  - Doze: CPU can run at a lower frequency than peripherals, a user-programmable feature
  - Alternate Clock modes allow on-the-fly switching to a lower clock speed for selective power reduction
- Fail-Safe Clock Monitor:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Ultra Low-Power Wake-up Pin Provides an External Trigger for Wake from Sleep
- 10,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- 100,000 Erase/Write Cycle Endurance Data EEPROM, Typical
- Flash and Data EEPROM Data Retention: 20 Years Minimum
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its Own On-Chip RC Oscillator for Reliable Operation
- On-Chip Regulator for 5V Operation
- Selectable Windowed WDT Feature
- Selectable Oscillator Options including:
  - 4x Phase Locked Loop (PLL)
- 8 MHz (FRC) Internal RC Oscillator:
  - HS/EC, High-Speed Crystal/Resonator Oscillator or External Clock
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) – via Two Pins
- In-Circuit Debugging
- Programmable High/Low-Voltage Detect (HLVD) module
- Programmable Brown-out Reset (BOR):
  - Software enable feature
  - Configurable shutdown in Sleep
  - Auto-configures power mode and sensitivity based on device operating speed
  - LPBOR available for re-arming of the POR

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FV08KM101
- PIC24FV08KM102
- PIC24FV16KM102
- PIC24FV16KM104
- PIC24FV08KM202
- PIC24FV08KM204
- PIC24FV16KM202
- PIC24FV16KM204
- PIC24F08KM101
- PIC24F08KM102
- PIC24F16KM102
- PIC24F16KM104
- PIC24F08KM202
- PIC24F08KM204
- PIC24F16KM202
- PIC24F16KM204

The PIC24FV16KM204 family introduces many new analog features to the extreme low-power Microchip devices. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSC).

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers. The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear Addressing of up to 16 Mbytes (program space) and 16 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32-bit by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as C
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FV16KM204 family incorporate a range of features that can significantly reduce power consumption during operation. Key features include:

- On-the-Fly Clock Switching, to allow the device clock to be changed under software control to the Timer1 source or the internal, low-power RC Oscillator during operation, allowing users to incorporate power-saving ideas into their software designs.
- Doze Mode Operation, when timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- Instruction-Based Power-Saving Modes, to allow the microcontroller to suspend all operations or selectively shut down its core while leaving its peripherals active with a single instruction in software.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

The PIC24FV16KM204 family offers five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock (EC) modes offering the option of a divide-by-2 clock output.
- Two Fast Internal Oscillators (FRCs), one with a nominal 8 MHz output and the other with a nominal 500 kHz output. These outputs can also be divided under software control to provide clock speed as low as 31 kHz or 2 kHz.
- A Phase Locked Loop (PLL) frequency multiplier, available to the external oscillator modes and the 8 MHz FRC Oscillator, which allows clock speeds of up to 32 MHz.
- A separate internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

NOTES:

3.0 CPU

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the *"PIC24F Family Reference Manual"*, **"CPU"** (DS39703).

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16^{th} working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory, defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to Data Space mapping feature lets any instruction access program space as if it were Data Space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (i.e., A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, the data memory and the registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register, which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed, but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow the users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.2.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using `MOV` instructions, which support Memory Direct Addressing (MDA) with a 16-bit address field. For PIC24FV16KM204 family devices, the entire implemented data memory lies in Near Data Space (NDS).

4.2.4 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by that module. Much of the SFR space contains unused addresses; these are read as '0'. The SFR space, where the SFRs are actually implemented, is provided in Table 4-2. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete listing of implemented SFRs, including their addresses, is provided in Table 4-3 through Table 4-26.

TABLE 4-2: IMPLEMENTED REGIONS OF SFR DATA SPACE

	SFR Space Address							
	xx00	**xx20**	**xx40**	**xx60**	**xx80**	**xxA0**	**xxC0**	**xxE0**
000h	Core			ICN	Interrupts			—
100h	Timers	CLC	MCCP/SCCP					
200h	MSSP	UART	Op Amp	DAC	—	—	I/O	
300h	A/D/CMTU				—	—	—	—
400h	—	—	—	—	—	—	—	ANSEL
500h	—	—	—	—	—	—	—	—
600h	—	RTCC/Comp	—	Band Gap	—			
700h	—	—	System/ HLVD	NVM/PMD	—	—	—	—

Legend: — = No implemented SFRs in this block.

TABLE 4-10: MCCP3 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CCP3CON1L(1)	188h	CCPON	—	CCPSIDL	r	TMRSYNC	CLKSEL2	CLKSEL1	CLKSEL0	TMRPS1	TMRPS0	T32	CCSEL	MOD3	MOD2	MOD1	MOD0	0000
CCP3CON1H(1)	18Ah	OPSSRC	RTRGEN	—	—	IOPS3	IOPS2	IOPS1	IOPS0	TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	0000
CCP3CON2L(1)	18Ch	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0	0000
CCP3CON2H(1)	18Eh	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0	0100
CCP3CON3L(1)	190h	—	—	—	—	—	—	—	—	—	—	DT5	DT4	DT3	DT2	DT1	DT0	0000
CCP3CON3H(1)	192h	OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2	OUTM1	OUTM0	—	—	POLACE	POLBDF	PSSACE1	PSSACE0	PSSBDF1	PSSBDF0	0000
CCP3STAT(1)	194h	—	—	—	—	—	—	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
CCP3TMRL(1)	198h	MCCP3 Time Base Register Low Word																0000
CCP3TMRH(1)	19Ah	MCCP3 Time Base Register High Word																0000
CCP3PRL(1)	19Ch	MCCP3 Time Base Period Register Low Word																FFFF
CCP3PRH(1)	19Eh	MCCP3 Time Base Period Register High Word																FFFF
CCP3RAL(1)	1A0h	Output Compare 3 Data Word A																0000
CCP3RBL(1)	1A4h	Output Compare 3 Data Word B																0000
CCP3BUFL(1)	1A8h	Input Capture 3 Data Buffer Low Word																0000
CCP3BUFH(1)	1AAh	Input Capture 3 Data Buffer High Word																0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-13: MSSP1 (I²C™/SPI) REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SSP1BUF	200h	—	—	—	—	—	—	—	—	MSSP1 Receive Buffer/Transmit Register								00xx
SSP1CON1	202h	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP1CON2	204h	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP1CON3	206h	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP1STAT	208h	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP1ADD	20Ah	—	—	—	—	—	—	—	—	MSSP1 Address Register in I²C Slave Mode MSSP1 Baud Rate Reload Register in I²C Master Mode								0000
SSP1MSK	20Ch	—	—	—	—	—	—	—	—	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	00FF

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-14: MSSP2 (I²C™/SPI) REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SSP2BUF(1)	210h	—	—	—	—	—	—	—	—	MSSP2 Receive Buffer/Transmit Register								00xx
SSP2CON1(1)	212h	—	—	—	—	—	—	—	—	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000
SSP2CON2(1)	214h	—	—	—	—	—	—	—	—	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000
SSP2CON3(1)	216h	—	—	—	—	—	—	—	—	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
SSP2STAT(1)	218h	—	—	—	—	—	—	—	—	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000
SSP2ADD(1)	21Ah	—	—	—	—	—	—	—	—	MSSP2 Address Register in I²C Slave Mode MSSP2 Baud Rate Reload Register in I²C Master Mode								0000
SSP2MSK(1)	21Ch	—	—	—	—	—	—	—	—	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	00FF

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These registers are available only on PIC24F(V)16KM2XX devices.

TABLE 4-24: PAD CONFIGURATION REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	2FCh	—	—	—	—	SDO2DIS(1)	SCK2DIS(1)	SDO1DIS	SCK1DIS	—	—	—	—	—	—	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These bits are not available on the PIC24F(V)08KM101 device, read as '0'.

6.4.1.1 Data EEPROM Bulk Erase

To erase the entire data EEPROM (bulk erase), the address registers do not need to be configured because this operation affects the entire data EEPROM. The following sequence helps in performing a bulk erase:

1. Configure NVMCON to Bulk Erase mode.
2. Clear the NVMIF status bit and enable the NVM interrupt (optional).
3. Write the key sequence to NVMKEY.
4. Set the WR bit to begin the erase cycle.
5. Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).

A typical bulk erase sequence is provided in Example 6-3.

6.4.2 SINGLE-WORD WRITE

To write a single word in the data EEPROM, the following sequence must be followed:

1. Erase one data EEPROM word (as mentioned in the previous section) if the PGMONLY bit (NVMCON<12>) is set to '1'.
2. Write the data word into the data EEPROM latch.
3. Program the data word into the EEPROM:
   - Configure the NVMCON register to program one EEPROM word (NVMCON<5:0> = 0001xx).
   - Clear the NVMIF status bit and enable the NVM interrupt (optional).
   - Write the key sequence to NVMKEY.
   - Set the WR bit to begin the erase cycle.
   - Either poll the WR bit or wait for the NVM interrupt (NVMIF is set).
   - To get cleared, wait until NVMIF is set.

A typical single-word write sequence is provided in Example 6-4.

EXAMPLE 6-3: DATA EEPROM BULK ERASE

```
    // Set up NVMCON to bulk erase the data EEPROM
    NVMCON = 0x4050;

    // Disable Interrupts For 5 Instructions
    asm volatile ("disi #5");

    // Issue Unlock Sequence and Start Erase Cycle
    __builtin_write_NVM();
```

EXAMPLE 6-4: SINGLE-WORD WRITE TO DATA EEPROM

```
int __attribute__ ((space(eedata))) eeData = 0x1234;
   int newData;                                         // New data to write to EEPROM
/*--------------------------------------------------------------------------------------------------
The variable eeData must be a Global variable declared outside of any method

the code following this comment can be written inside the method that will execute the write
----------------------------------------------------------------------------------------------------
*/
   unsigned int offset;

   // Set up NVMCON to erase one word of data EEPROM
   NVMCON = 0x4004;

   // Set up a pointer to the EEPROM location to be erased
   TBLPAG = __builtin_tblpage(&eeData);                 // Initialize EE Data page pointer
   offset = __builtin_tbloffset(&eeData);               // Initizlize lower word of address
   __builtin_tblwtl(offset, newData);                   // Write EEPROM data to write latch

   asm volatile ("disi #5");                            // Disable Interrupts For 5 Instructions
   __builtin_write_NVM();                               // Issue Unlock Sequence & Start Write Cycle
   while(NVMCONbits.WR=1);                              // Optional: Poll WR bit to wait for
                                                        // write sequence to complete
```

REGISTER 9-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference Oscillator is enabled on the REFO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep
0 = Reference Oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Primary Oscillator is used as the base clock(1)
0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits
1111 = Base clock value divided by 32,768
1110 = Base clock value divided by 16,384
1101 = Base clock value divided by 8,192
1100 = Base clock value divided by 4,096
1011 = Base clock value divided by 2,048
1010 = Base clock value divided by 1,024
1001 = Base clock value divided by 512
1000 = Base clock value divided by 256
0111 = Base clock value divided by 128
0110 = Base clock value divided by 64
0101 = Base clock value divided by 32
0100 = Base clock value divided by 16
0011 = Base clock value divided by 8
0010 = Base clock value divided by 4
0001 = Base clock value divided by 2
0000 = Base clock value

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

REGISTER 10-1: ULPWCON: ULPWU CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ULPEN:** ULPWU Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ULPSIDL:** ULPWU Stop in Idle Select bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **ULPSINK:** ULPWU Current Sink Enable bit
1 = Current sink is enabled
0 = Current sink is disabled

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-2: ANSB: PORTB ANALOG SELECTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	R/W-1	R/W-1
ANSB15	ANSB14	ANSB13	ANSB12	—	—	ANSB9	ANSB8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSB7	ANSB6(1)	ANSB5(1)	ANSB4	ANSB3(1)	ANSB2	ANSB1	ANSB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **ANSB<15:12>:** Analog Select Control bits
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-0 **ANSB<9:0>:** Analog Select Control bits(1)
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: The ANSB<6:5,3> bits are not available on 20-pin devices.

REGISTER 11-3: ANSC: PORTC ANALOG SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	ANSC2(1,2)	ANSC1(1,2)	ANSC0(1,2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ANSC<2:0>:** Analog Select Control bits(1,2)
1 = Digital input buffer is not active (use for analog input)
0 = Digital input buffer is active

Note 1: These bits are not implemented in 20-pin devices.
2: These bits are not implemented in 28-pin devices.

REGISTER 19-1: AD1CON1: A/DA/D CONTROL REGISTER 1 (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This version of the TMR1 Trigger allows A/D conversions to be triggered from TMR1 while the device is operating in Sleep mode. The SSRC<3:0> = 0101 option allows conversions to be triggered in Run or Idle modes only.

REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS(1)	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM(1)	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG<1:0>:** A/D Converter Positive Voltage Reference Configuration bits
11 = 4 * Internal VBG(2)
10 = 2 * Internal VBG(3)
01 = External VREF+
00 = AVDD

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bits
1 = External VREF-
0 = AVSS

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into a buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ S/H Input for MUX A Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **BUFS:** A/D Buffer Fill Status bit(1)
1 = A/D is filling the upper half of the buffer; user should access data in the lower half
0 = A/D is filling the lower half of the buffer; user should access data in the upper half

bit 6-2 **SMPI<4:0>:** Interrupt Sample Rate Select bits
11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
•
•
•
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

bit 1 **BUFM:** A/D Buffer Fill Mode Select bit(1)
1 = Starts filling the buffer at address, ADC1BUF0, on the first interrupt and ADC1BUF(x/2) on the next interrupt (Split Buffer mode)
0 = Starts filling the buffer at address, ADC1BUF0, and each sequential address on successive interrupts (FIFO mode)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
0 = Always uses channel input selects for Sample A

Note 1: This is only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.
2: PIC24FV16KMXXX devices only. Reference setting will not be within specification for VDD below 4.5V.
3: Reference setting will not be within specification for VDD below 2.3V.

REGISTER 19-5: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB<2:0>:** Sample B Channel 0 Negative Input Select bits

`111` = AN6(1)
`110` = AN5(2)
`101` = AN4
`100` = AN3
`011` = AN2
`010` = AN1
`001` = AN0
`000` = AVSS

bit 12-8 **CH0SB<4:0>:** S/H Amplifier Positive Input Select for MUX B Multiplexer Setting bits

`11111` = Unimplemented, do not use
`11110` = AVDD(3)
`11101` = AVSS(3)
`11100` = Upper guardband rail (0.785 * VDD)
`11011` = Lower guardband rail (0.215 * VDD)
`11010` = Internal Band Gap Reference (VBG)(3)
`11000-11001` = Unimplemented, do not use
`10001` = No channels are connected, all inputs are floating (used for CTMU)
`10111` = No channels are connected, all inputs are floating (used for CTMU)
`10110` = No channels are connected, all inputs are floating (used for CTMU temperature sensor input); does not require the corresponding CTMEN22 (AD1CTMENH<6>) bit)
`10101` = Channel 0 positive input is AN21
`10100` = Channel 0 positive input is AN20
`10011` = Channel 0 positive input is AN19
`10010` = Channel 0 positive input is AN18(2)
`10001` = Channel 0 positive input is AN17(2)
•
•
•
`01001` = Channel 0 positive input is AN9
`01000` = Channel 0 positive input is AN8(1)
`00111` = Channel 0 positive input is AN7(1)
`00110` = Channel 0 positive input is AN6(1)
`00101` = Channel 0 positive input is AN5(2)
`00100` = Channel 0 positive input is AN4
`00011` = Channel 0 positive input is AN3
`00010` = Channel 0 positive input is AN2
`00001` = Channel 0 positive input is AN1
`00000` = Channel 0 positive input is AN0

Note 1: This is implemented on 44-pin devices only.
2: This is implemented on 28-pin and 44-pin devices only.
3: The band gap value used for this input is 2x or 4x the internal VBG, which is selected when PVCFG<1:0> = `1x`.

21.0 DUAL OPERATIONAL AMPLIFIER MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **"Operational Amplifier (Op Amp)"** (DS30505). Device-specific information in this data sheet supersedes the information in the *"PIC24F Family Reference Manual"*.

PIC24FV16KM204 family devices include two operational amplifiers to complement the microcontroller's other analog features. They may be used to provide analog signal conditioning, either as stand-alone devices or in addition to other analog peripherals.

The two op amps are functionally identical; the block diagram for a single amplifier is shown in Figure 21-1. Each op amp has these features:

- Internal unity-gain buffer option
- Multiple input options each on the inverting and non-inverting amplifier inputs
- Rail-to-rail input and output capabilities
- User-selectable option for regular or low-power operation
- User-selectable operation in Idle and Sleep modes

When using the op amps, it is recommended to set the ANSx and TRISx bits of both the input and output pins to configure them as analog pins. See **Section 11.2 "Configuring Analog Port Pins"** for more information.

FIGURE 21-1: SINGLE OPERATIONAL AMPLIFIER BLOCK DIAGRAM

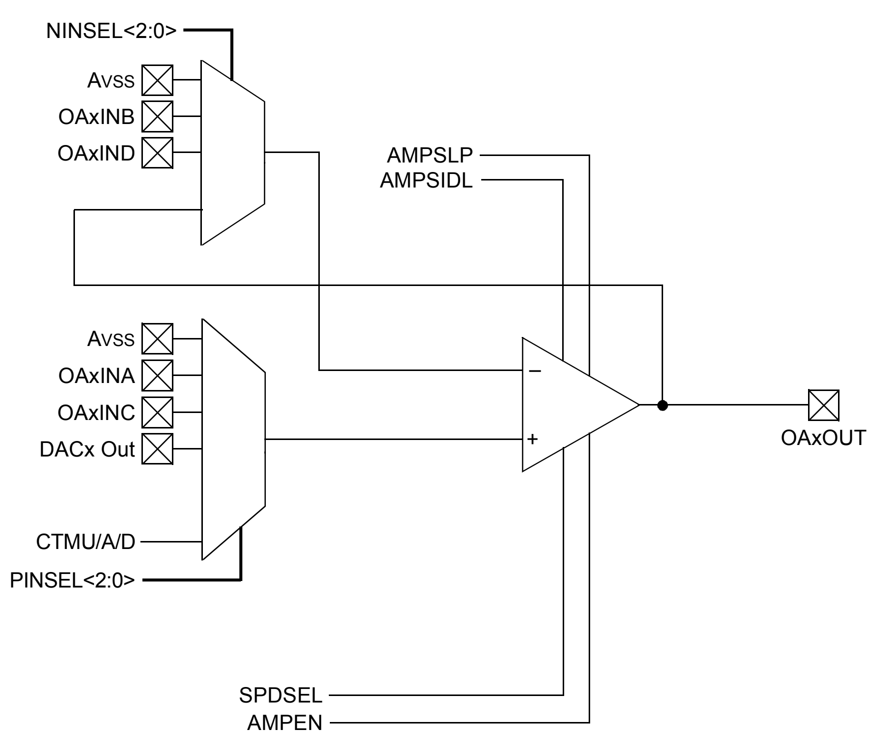


FIGURE 27-6: EXTERNAL CLOCK TIMING

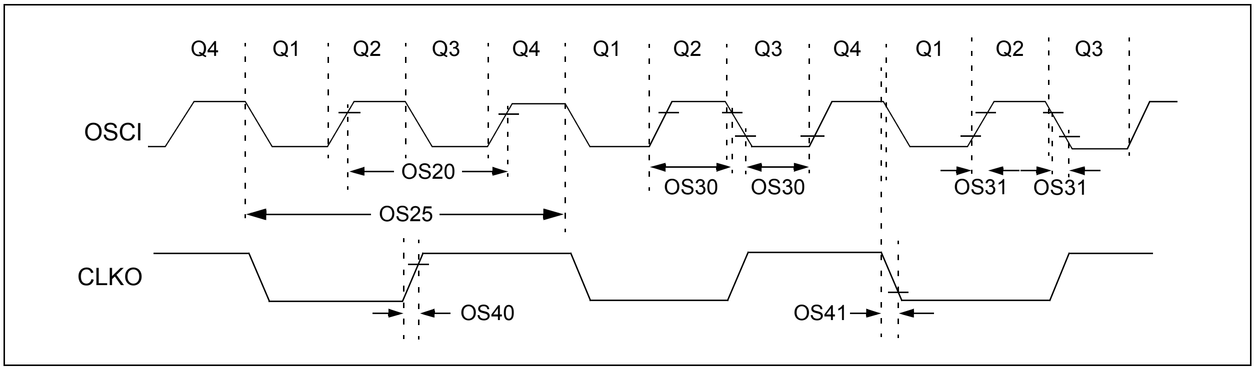


TABLE 27-20: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External Clocks allowed only in EC mode)	DC 4 DC 4	— — — —	32 8 24 6	MHz MHz MHz MHz	EC, -40°C < TA < +85°C ECPLL, -40°C < TA < +85°C EC, -40°C < TA < +125°C ECPLL, -40°C < TA < +125°C
		Oscillator Frequency	0.2 4 4 4 31	— — — — —	4 25 8 6 33	MHz MHz MHz MHz kHz	XT HS XTPLL, -40°C < TA < +85°C XTPLL, -40°C < TA < +125°C SOSC
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See Parameter OS10 for FOSC value
OS25	TCY	Instruction Cycle Time(2)	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	6	10	ns	
OS41	TckF	CLKO Fall Time(3)	—	6	10	ns	

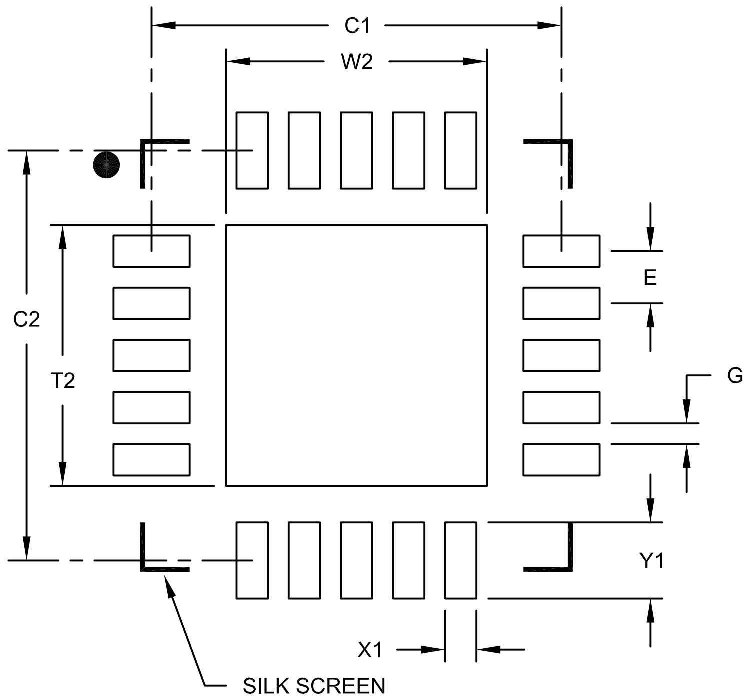
Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an External Clock applied to the OSCI/CLKI pin. When an External Clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 TCY) and high for the Q3-Q4 period (1/2 TCY).

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

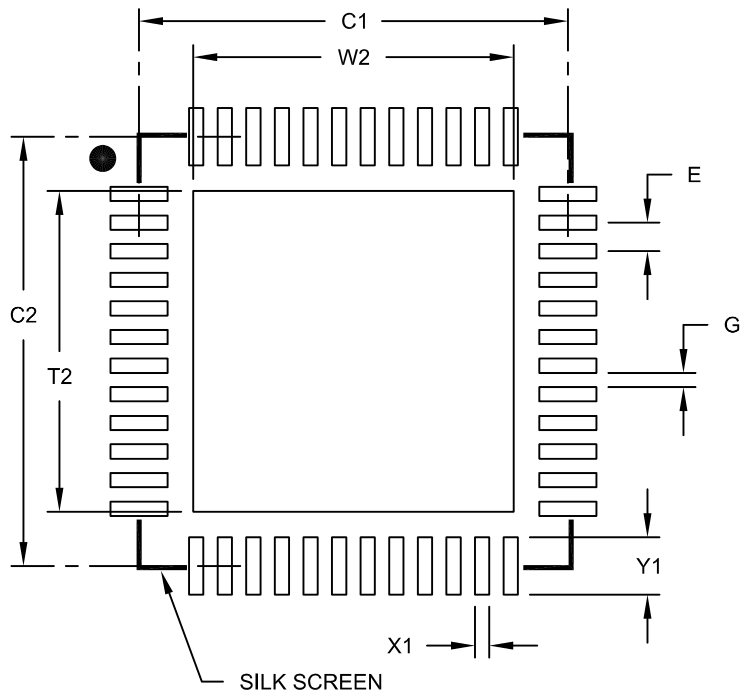
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

