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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km204-i-pt

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NOTES:

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

			F					FV					
			Pin Numb	er			I	Pin Numb	er				
Function	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	I/O	Buffer	Description
RB9	13	18	15	1	1	13	18	15	1	1	I/O	ST	PORTB Pins
RB10	_	21	18	8	9	_	21	18	8	9	I/O	ST	PORTB Pins
RB11	_	22	19	9	10	_	22	19	9	10	I/O	ST	PORTB Pins
RB12	15	23	20	10	11	15	23	20	10	11	I/O	ST	PORTB Pins
RB13	16	24	21	11	12	16	24	21	11	12	I/O	ST	PORTB Pins
RB14	17	25	22	14	15	17	25	22	14	15	I/O	ST	PORTB Pins
RB15	18	26	23	15	16	18	26	23	15	16	I/O	ST	PORTB Pins
RC0	_	_	_	25	27	_	_	—	25	27	I/O	ST	PORTC Pins
RC1	_	_	_	26	28	_	_	—	26	28	I/O	ST	PORTC Pins
RC2	_	_	_	27	29	_	_	—	27	29	I/O	ST	PORTC Pins
RC3			_	36	39	_		—	36	39	I/O	ST	PORTC Pins
RC4			_	37	40	_		—	37	40	I/O	ST	PORTC Pins
RC5			_	38	41	_		—	38	41	I/O	ST	PORTC Pins
RC6			_	2	2	_		_	2	2	I/O	ST	PORTC Pins
RC7			_	3	3	_		_	3	3	I/O	ST	PORTC Pins
RC8			_	4	4	_		_	4	4	I/O	ST	PORTC Pins
RC9	_	_	_	5	5	_	_	—	5	5	I/O	ST	PORTC Pins
REFO	18	26	23	15	16	18	26	23	15	16	0	_	Reference Clock Output
RTCC		25	22	14	15	_	25	22	14	15	0	_	Real-Time Clock/Calendar Output
SCK1	15	22	19	9	10	15	22	19	9	10	I/O	ST	MSSP1 SPI Clock
SDI1	17	21	18	8	9	17	21	18	8	9	I	ST	MSSP1 SPI Data Input
SDO1	16	24	21	11	12	16	24	21	11	12	0	—	MSSP1 SPI Data Output
SS1	18	26	23	15	16	18	26	23	15	16	I	ST	MSSP1 SPI Slave Select Input
SCK2	_	14	11	38	41	—	14	11	38	41	I/O	ST	MSSP2 SPI Clock
SDI2	_	19	16	36	39	_	19	16	36	39	I	ST	MSSP2 SPI Data Input
SDO2	_	15	12	37	40	_	15	12	37	40	0		MSSP2 SPI Data Output
SS2	_	23	20	35	38	_	23	20	35	38	Ι	ST	MSSP2 SPI Slave Select Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, $I^2C^{TM} = I^2C/SMBus$ input buffer

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 μ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of $0.01 \ \mu\text{F}$ to $0.001 \ \mu\text{F}$. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., $0.1 \ \mu\text{F}$ in parallel with $0.001 \ \mu\text{F}$).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



TABLE 4-4: ICN REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNPD1	56h	CN15PDE ^(1,2)	CN14PDE	CN13PDE	CN12PDE	CN11PDE	CN10PDE(2)	CN9PDE ^(1,2)	-	CN7PDE ^(1,2)	CN6PDE	CN5PDE	CN4PDE	CN3PDE	CN2PDE	CN1PDE	CN0PDE	0000
CNPD2	58h	CN31PDE ⁽²⁾	CN30PDE	CN29PDE	CN28PDE(2)	CN27PDE ^(1,2)	CN26PDE ⁽²⁾	CN25PDE ⁽²⁾	CN24PDE ^(1,2)	CN23PDE	CN22PDE	CN21PDE	CN20PDE(2)	CN19PDE ⁽²⁾	CN18PDE ⁽²⁾	CN17PDE ⁽²⁾	CN16PDE ^(1,2)	0000
CNPD3	5Ah	_	_	_	_	_	_	_	_	_	_	_	CN36PDE ⁽²⁾	CN35PDE ⁽²⁾	CN34PDE ⁽²⁾	CN33PDE ⁽²⁾	CN32PDE ⁽²⁾	0000
CNEN1	62h	CN15IE ^(1,2)	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE ⁽²⁾	CN9IE ^(1,2)	_	CN7IE ^(1,2)	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	64h	CN31IE ⁽²⁾	CN30IE	CN29IE	CN28IE ⁽²⁾	CN27IE ^(1,2)	CN26IE ⁽²⁾	CN25IE ⁽²⁾	CN24IE ^(1,2)	CN23IE	CN22IE	CN21IE	CN20IE ⁽²⁾	CN19IE ⁽²⁾	CN18IE ⁽²⁾	CN17IE ⁽²⁾	CN16IE ^(1,2)	0000
CNEN3	66h	-	_	—	_	_	_	—	—	—	_	_	CN36IE ⁽²⁾	CN35IE ⁽²⁾	CN34IE ⁽²⁾	CN33IE ⁽²⁾	CN32IE ⁽²⁾	0000
CNPU1	6Eh	CN15PUE ^(1,2)	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE ⁽²⁾	CN9PUE ^(1,2)	—	CN7PUE ^(1,2)	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	70h	CN31PUE ⁽²⁾	CN30PUE	CN29PUE	CN28PUE(2)	CN27PUE ^(1,2)	CN26PUE ⁽²⁾	CN25PUE ⁽²⁾	CN24PUE ^(1,2)	CN23PUE	CN22PUE	CN21PUE	CN20PUE ⁽²⁾	CN19PUE ⁽²⁾	CN18PUE ⁽²⁾	CN17PUE ⁽²⁾	CN16PUE ^(1,2)	0000
CNPU3	72h	_	_	_		_	_	_	_	_	_	_	CN36PUE ⁽²⁾	CN35PUE ⁽²⁾	CN34PUE ⁽²⁾	CN33PUE ⁽²⁾	CN32PUE ⁽²⁾	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

Note 1: These bits are available only on 28-pin devices

2: These bits are available only on 44-pin devices

ГABLE 4-29:	COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	630h	CMIDL		—	—		C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT	—	—			_	C3OUT ⁽¹⁾	C2OUT ⁽¹⁾	C10UT	0000
CVRCON	632h	_	_	_	_	_	_	_	_	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	634h	CON	COE	CPOL	CLPWR	_	_	CEVT	COUT	EVPOL1	EVPOL0	_	CREF1	CREF0	_	CCH1	CCH0	0000
CM2CON ⁽¹⁾	636h	CON	COE	CPOL	CLPWR		_	CEVT	COUT	EVPOL1	EVPOL0		CREF1 ⁽¹⁾	CREF0	—	CCH1	CCH0	0000
CM3CON ⁽¹⁾	638h	CON	COE	CPOL	CLPWR	_		CEVT	COUT	EVPOL1	EVPOL0	_	CREF1 ⁽¹⁾	CREF0	_	CCH1	CCH0	0000

 $\label{eq:legend: second condition, u = unchanged, --= unimplemented, q = value depends on condition, r = reserved.$

Note 1: These registers and bits are available only on PIC24F(V)16KM2XX devices.

TABLE 4-30: BAND GAP BUFFER CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
BUFCON0	670h	_	_				_			—	—			—		BUFREF1	BUFREF0	0001

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved.

EXAMPLE 5-3: LOADING THE WRITE BUFFERS – ASSEMBLY LANGUAGE CODE

;	Set up NVMCO	N for row programming operation	ıs	
	MOV	#0x4004, W0	;	
	MOV	W0, NVMCON	;	Initialize NVMCON
;	Set up a poir	nter to the first program memor	сy	location to be written
;	program memo:	ry selected, and writes enabled	1	
	MOV	#0x0000, W0	;	
	MOV	W0, TBLPAG	;	Initialize PM Page Boundary SFR
	MOV	#0x1500, W0	;	An example program memory address
;	Perform the '	TBLWT instructions to write the	2	latches
;	0th_program_	word		
	MOV	#LOW_WORD_0, W2	;	
	MOV	#HIGH_BYTE_0, W3	;	
	TBLWTL	W2, [W0]	;	Write PM low word into program latch
	TBLWTH	W3, [W0++]	;	Write PM high byte into program latch
;	lst_program_v	word		
	MOV	#LOW_WORD_1, W2	;	
	MOV	#HIGH_BYTE_1, W3	;	
	TBLWTL	W2, [W0]	;	Write PM low word into program latch
	TBLWTH	W3, [W0++]	;	Write PM high byte into program latch
;	2nd_program_v	word		
	MOV	#LOW_WORD_2, W2	;	
	MOV	#HIGH_BYTE_2, W3	;	
	TBLWTL	W2, [W0]	;	Write PM low word into program latch
	TBLWTH	W3, [W0++]	;	Write PM high byte into program latch
	•			
	•			
	•			
;	32nd_program	_word		
	MOV	#LOW_WORD_31, W2	;	
	MOV	<pre>#HIGH_BYTE_31, W3</pre>	;	
	TBLWTL	W2, [WU]	;	Write PM low word into program latch
	TBLWTH	W3, [W0]	;	Write PM high byte into program latch

EXAMPLE 5-4: LOADING THE WRITE BUFFERS – 'C' LANGUAGE CODE

```
// C example using MPLAB C30
  #define NUM_INSTRUCTION_PER_ROW 64
int __attribute__ ((space(auto_psv))) progAddr = 0x1234 // Variable located in Pgm Memory
  unsigned int offset;
  unsigned int i;
  unsigned int progData[2*NUM_INSTRUCTION_PER_ROW];
                                                            // Buffer of data to write
  //Set up NVMCON for row programming
  NVMCON = 0 \times 4004;
                                                            // Initialize NVMCON
  //Set up pointer to the first memory location to be written
  TBLPAG = __builtin_tblpage(&progAddr);
                                                           // Initialize PM Page Boundary SFR
                                                            // Initialize lower word of address
  offset = __builtin_tbloffset(&progAddr);
  //Perform TBLWT instructions to write necessary number of latches
  for(i=0; i < 2*NUM_INSTRUCTION_PER_ROW; i++)</pre>
  {
                                                          // Write to address low word
      __builtin_tblwtl(offset, progData[i++]);
       __builtin_tblwth(offset, progData[i]);
                                                            // Write to upper byte
      offset = offset + 2;
                                                            // Increment address
  }
```

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	U2TXIP2	U2TXIP1	U2TXIP0	_	U2RXIP2	U2RXIP1	U2RXIP0
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	INT2IP2	INT2IP1	INT2IP0	—	CCT4IP2	CCT4IP1	CCT4IP0
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 15	Unimplemen	ted: Read as '	D'				
bit 14-12	U2TXIP<2:0>	: UART2 Trans	smitter Interrup	ot Priority bits			
	111 = Interrup	ot is Priority 7(highest priority	interrupt)			
	•						
	•						
	001 = Interrup	ot is Priority 1	abled				
bit 11	Unimplemen	ted: Read as '	ab.ou n'				
bit 10-8	U2RXIP<2:0>	: UART2 Rece	eiver Interrupt F	Priority bits			
	111 = Interrup	ot is Priority 7 (highest priority	(interrupt)			
	•	, , , , , , , , , , , , , , , , , , ,	0 1 3	.,			
	•						
	• 001 = Interrur	ot is Priority 1					
	000 = Interrup	ot source is dis	abled				
bit 7	Unimplemen	ted: Read as '	D'				
bit 6-4	INT2IP<2:0>:	External Interr	upt 2 Priority b	oits			
	111 = Interrup	ot is Priority 7(highest priority	v interrupt)			
	•						
	•						
	001 = Interru	ot is Priority 1					
	000 = Interrup	ot source is dis	abled				
bit 3	Unimplemen	ted: Read as '	o'				
bit 2-0	CCT4IP<2:0>	: Capture/Com	pare 4 Timer I	nterrupt Priorit	y bits		
	111 = Interrup	ot is Priority 7 (highest priority	interrupt)			
	•						
	•						
	001 = Interru	ot is Priority 1					
	000 = Interrup	ot source is dis	abled				

REGISTER 8-26: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

REGISTER 13-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	_	OUTM2 ⁽¹⁾	OUTM1 ⁽¹⁾	OUTM0 ⁽¹⁾
bit 15	I						bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	POLACE	POLBDF ⁽¹⁾	PSSACE1	PSSACE0	PSSBDF1 ⁽¹⁾	PSSBDF0 ⁽¹⁾
bit 7							bit 0
Legend:	b :4		.:.		antad bit maa	L a a '0'	
R = Readable		vv = vvritable t	DIC	0 = 0 minipien	nented bit, read	ias u	011/2
	PUR	I = DILIS SEL			areu		own
bit 15	OETRIG: CCF 1 = For Trigge 0 = Normal of	Px Dead-Time S ered mode (TR utput pin opera	Select bit IGEN = 1): Mo tion	dule does not	drive enabled c	output pins until	triggered
bit 14-12	OSCNT<2:0>	: One-Shot Eve	ent Count bits				
	111 = Extend 110 = Extend 101 = Extend 100 = Extend 011 = Extend 010 = Extend 010 = Extend 011 = Extend 010 = Extend 001 = Extend 001 = Extend 000 = Do not	d one-shot ever d one-shot ever d one-shot ever d one-shot ever d one-shot ever d one-shot ever d one-shot ever e extend one-shot	at by 7 time bas at by 6 time bas at by 5 time bas at by 4 time bas at by 3 time bas at by 2 time bas at by 1 time bas ot Trigger even	se periods (8 ti se periods (7 ti se periods (6 ti se periods (5 ti se periods (4 ti se periods (3 ti se period (2 tin nt	me base period me base period me base period me base period me base period me base period	ds total) ds total) ds total) ds total) ds total) ds total) s total)	
bit 11	Unimplement	ted: Read as '0	,				
bit 10-8	OUTM<2:0>:	PWMx Output	Mode Control I	bits ⁽¹⁾			
	111 = Reserv 110 = Output 101 = Brush I 001 = Brush I 011 = Reserv 010 = Half-Bri 001 = Push-P 000 = Steerat	ed Scan mode DC Output mod DC Output mod ed idge Output mod olle Single Output	e, forward e, reverse de e ut mode				
bit 7-6	Unimplement	ted: Read as '0	,				
bit 5	POLACE: CC 1 = Output pin 0 = Output pin	Px Output Pins n polarity is act n polarity is act	, OCxA, OCxC ive-low ive-high	C and OCxE, P	olarity Control I	bit	
bit 4	POLBDF: CC	Px Output Pins	, OCxB, OCxE	and OCxF, Po	plarity Control b	oit(1)	
	1 = Output pi 0 = Output pi	n polarity is act n polarity is act	ive-low ive-high				
bit 3-2	PSSACE<1:0	>: PWMx Outp	ut Pins, OCxA	, OCxC and O	CxE, Shutdown	State Control b	oits
	11 = Pins are 10 = Pins are 0x = Pins are	driven active w driven inactive tri-stated when	hen a shutdow when a shutdo a shutdown e	vn event occurs own event occu vent occurs	s Jrs		
bit 1-0	PSSBDF<1:0	>: PWMx Outp	ut Pins, OCxB,	, OCxD, and O	CxF, Shutdown	State Control I	oits ⁽¹⁾
	11 = Pins are 10 = Pins are 0x = Pins are	driven active w driven inactive in a high-imped	hen a shutdow when a shutdo dance state wh	vn event occurs own event occu nen a shutdowr	s urs n event occurs		

Note 1: These bits are implemented in MCCPx modules only.

REGISTER 14-7: SSPxCON3: MSSPx CONTROL REGISTER 3 (I²C[™] MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
				_	_	_	_
bit 15							bit 8
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM	⁽¹⁾ PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0
Legend:							
R = Reada	able bit	W = Writable b	it	U = Unimplen	nented bit, read	d as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-8	Unimplemer	nted: Read as '0'	,				
bit 7	ACKTIM: Ac	knowledge Time	Status bit ⁽¹⁾				
	1 = Indicates	the I ² C bus is in	an Acknowle	dge sequence,	set on the 8 th f	alling edge of t	he SCLx clock
	0 = Not an A	cknowledge sequ	uence, cleared	d on the 9 th risi	ng edge of the	SCLx clock	
bit 6	PCIE: Stop C	Condition Interrup	t Enable bit				
	\perp = Enables	Interrupt on deter	ction of a Stop) condition			
bit 5	SCIE: Start (Condition Interrup	t Enable hit				
bit 0	1 = Enables i	interrupt on deter	ction of a Star	t or Restart cor	ndition		
	0 = Start dete	ection interrupts a	are disabled ⁽²)			
bit 4	BOEN: Buffe	er Overwrite Enat	ole bit				
	<u>I²C Master m</u> This bit is ign	<u>node:</u> iored.					
	I ² C Slave mo	<u>ode:</u>					
	1 = SSPxBU	JF is updated and	l an <mark>ACK</mark> is ge	enerated for a re	eceived addres	s/data byte, ign	oring the state
	of the SS	SPOV bit only if t	he BF bit = 0))/ is cloar			
hit 3		A Hold Time Sel	ection hit				
DIL O		of 300 ns hold ti	ime on SDAx	after the falling	edge of SCLx		
	0 = Minimum	of 100 ns hold ti	ime on SDAx	after the falling	edge of SCLx		
bit 2	SBCDE: Slav	ve Mode Bus Col	llision Detect	Enable bit (Sla	ve mode only)		
	1 = Enables	slave bus collisio	n interrupts				
	0 = Slave bu	s collision interru	pts are disabl	ed			
bit 1	AHEN: Addre	ess Hold Enable	bit (Slave mo	de only)			
	1 = Followin	g the 8th falling	edge of SCL	Lx for a match	ing received a	ddress byte; C	CKP bit of the
	0 = Address	holding is disabl	ed		neia iow		
bit 0	DHEN: Data	Hold Enable bit	Slave mode (onlv)			
	1 = Followin	g the 8th falling e	edge of SCLx	for a received of	data byte: slave	e hardware clea	irs the CKP bit
	of the SS	SPxCON1 registe	er and SCLx is	s held low	, ,		
	0 = Data hol	ding is disabled					
Note 1:	This bit has no e	ffect in Slave mo	des for which	Start and Stop	condition dete	ction is explicitl	y listed as
	enabled.			· · · · · ·		- F	•

2: The ACKTIM status bit is active only when the AHEN bit or DHEN bit is set.

REGISTER 15-3: UXTXREG: UARTX TRANSMIT REGISTER

U-x	U-x	U-x	U-x	U-x	U-x	U-x	W-x
—	—	—	—	—	—	—	UTX8
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
UTX7	UTX6	UTX5	UTX4	UTX3	UTX2	UTX1	UTX0
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-9 Unimplemented: Read as '0'

bit 8 **UTX8:** Data of the Transmitted Character bit (in 9-bit mode)

bit 7-0 UTX<7:0>: Data of the Transmitted Character bits

REGISTER 15-4: UxRXREG: UARTx RECEIVE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC
—	—	—	—	—	—	—	URX8
bit 15							bit 8

| R-0, HSC |
|----------|----------|----------|----------|----------|----------|----------|----------|
| URX7 | URX6 | URX5 | URX4 | URX3 | URX2 | URX1 | URX0 |
| bit 7 | | | | | | | bit 0 |

Legend:	HSC = Hardware Settable/Clearable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-9 Unimplemented: Read as '0'

bit 8 URX8: Data of the Received Character bit (in 9-bit mode)

bit 7-0 URX<7:0>: Data of the Received Character bits

16.3 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value, loaded into the lower half of RCFGCAL, is multiplied by four and will be either added or subtracted from the RTCC timer, once every minute. Refer to the steps below for RTCC calibration:

- 1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
- 2. Once the error is known, it must be converted to the number of error clock pulses per minute.
- 3. a) If the oscillator is faster than ideal (negative result from Step 2), the RCFGCAL register value must be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

b) If the oscillator is slower than ideal (positive result from Step 2), the RCFGCAL register value must be positive. This causes the specified number of clock pulses to be subtracted from the timer counter, once every minute.

EQUATION 16-1:

(Ideal Frequency [†] – Measured Frequency) *						
60 = Clocks per Minute						
† Ideal Frequency = 32,768 Hz						

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse, except when SECONDS = 00, 15, 30 or 45. This is due to the auto-adjust of the RTCC at 15 second intervals.

Note: It is up to the user to include, in the error value, the initial error of the crystal: drift due to temperature and drift due to crystal aging.

16.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>)
- One-time alarm and repeat alarm options are available

16.4.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 16-2, the interval selection of the alarm is configured through the AMASKx bits (ALCFGRPT<13:10>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ARPT<7:0> bits (ALCFGRPT<7:0>). When the value of the ARPTx bits equals 00h and the CHIME bit (ALCFGRPT<14>) is cleared, the repeat function is disabled, and only a single alarm will occur. The alarm can be repeated up to 255 times by loading ARPT<7:0> with FFh.

After each alarm is issued, the value of the ARPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ARPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

16.4.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to other peripherals.

Note: Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers, and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

17.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCONL
- CLCxCONH
- CLCxSEL
- CLCxGLSL
- CLCxGLSH

The CLCx Control registers (CLCxCONL and CLCxCONH) are used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables. The CLCx Source Select register (CLCxSEL) allows the user to select up to 4 data input sources using the 4 data input selection multiplexers. Each multiplexer has a list of 8 data sources available.

The CLCx Gate Logic Select registers (CLCxGLSL and CLCxGLSH) allow the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these 8 signals are enabled, ORed together by the logic cell input gates.

REGISTER 17-1: CLCxCONL: CLCx CONTROL REGISTER (LOW)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
LCEN		<u> </u>		INTP	INTN		
bit 15							bit 8
R-0	R-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
LCOE	LCOUT	LCPOL	—	—	MODE2	MODE1	MODE0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable b	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15	LCEN: CLCx	Enable bit					
	1 = CLCx is $0 = CLCx$ is 0	enabled and mix	king input sign s loaic zero o	ials utputs			
bit 14-12	Unimplemen	ted: Read as '0	,				
bit 11	INTP: CLCx F	Positive Edge In	terrupt Enable	e bit			
	1 = Interrupt	will be generate	d when a risir	ng edge occurs	on LCOUT		
	0 = Interrupt	will not be gene	rated				
bit 10	INTN: CLCx I	Negative Edge I	nterrupt Enab	le bit			
	1 = Interrupt 0 = Interrupt	will be generate will not be gene	ed when a falli rated	ng edge occurs	s on LCOUT		
bit 9-8	Unimplemen	ted: Read as '0	,				
bit 7	LCOE: CLCx	Port Enable bit					
	1 = CLCx por	t pin output is e	nabled				
	0 = CLCx por	t pin output is d	isabled				
bit 6	LCOUT: CLC	x Data Output S	status bit				
	1 = CLCx out	put high					
bit 5		y Output Polarit	v Control hit				
bit 0	1 = The outp	ut of the module	e is inverted				
	0 = The outp	ut of the module	e is not inverte	ed			
bit 4-3	Unimplemen	ted: Read as '0	,				

REGISTER 19-7: AD1CHITL: A/D SCAN COMPARE HIT REGISTER (LOW WORD)⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH15	CHH14	CHH13	CHH12	CHH11 CHH10		CHH9	CHH8 ^(2,3)
bit 15					- -		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH7 ^(2,3)	CHH6 ^(2,3)	CHH5 ⁽²⁾	CHH4	CHH3	CHH2	CHH1	CHH0
bit 7				-			bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1'		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-0	CHH<15:0>:	A/D Compare H	lit bits ^(2,3)				
	<u>If CM<1:0> =</u>	<u>_11:</u>					
	1 = A/D Res	ult Buffer x has	been written v	vith data or a m	atch has occur	red	

0 = A/D Result Buffer x has not been written with data

For All Other Values of CM<1:0>:

1 = A match has occurred on A/D Result Channel x

0 = No match has occurred on A/D Result Channel x

Note 1: Unimplemented channels are read as '0'.

2: The CHH<8:5> bits are not implemented in 20-pin devices.

3: The CHH<8:6> bits are not implemented in 28-pin devices.

23.0 COMPARATOR VOLTAGE REFERENCE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Comparator Voltage Reference, refer to the "PIC24F Family Reference Manual", "Comparator Voltage Reference Module" (DS39709).

23.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 23-1). The comparator voltage reference provides a range of output voltages with 32 distinct levels.

The comparator voltage reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.





24.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Time Measurement Unit, refer to the "PIC24F Family Reference Manual", "Charge Time Measurement Unit (CTMU) with Threshold Detect" (DS39743).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Thirteen external edge input Trigger sources
- · Polarity control for each edge source
- · Control of edge sequence
- Control of response to edge levels or edge transitions
- · Time measurement resolution of one nanosecond
- Accurate current source suitable for capacitive measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module and controls the mode of operation of the CTMU, as well as controlling edge sequencing. CTMUCON2 controls edge source selection and edge source polarity selection. The CTMUICON register selects the current range of current source and trims the current.

24.1 Measuring Capacitance

The CTMU module measures capacitance by generating an output pulse, with a width equal to the time between edge events, on two separate input channels. The pulse edge events to both input channels can be selected from several internal peripheral modules (OC1, Timer1, any input capture or comparator module) and up to 13 external pins (CTED1 through CTED13). This pulse is used with the module's precision current source to calculate capacitance according to the relationship:

EQUATION 24-1:

$$I = C \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an External Capacitor (CAPP) on one of its input channels after the CTMU output's pulse. A Precision Resistor (RPR) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 24-1 illustrates the external connections used for capacitance measurements, and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the "*PIC24F Family Reference Manual*".

REGISTER 24-3: CTMUCON2L: CTMU CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_			_	_				
bit 15					·		bit 8	
U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
—	—	—	IRSTEN	—	DISCHS2	DISCHS1	DISCHS0	
bit 7							bit 0	
Legend:								
R = Readab	ole bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			own	
bit 15-5	Unimplemen	ted: Read as '	0'					
bit 4	IRSTEN: CTM	MU Current So	urce Reset Ena	able bit				
	1 = Signal se detect log	elected by the gic	DISCHS<2:0>	bits or the ID	ISSEN control	bit will reset th	e CTMU edge	
	0 = CTMU ed	dge detect logic	c will not occur					
bit 3	Unimplemen	ted: Read as '	0'					
bit 2-0	DISCHS<2:0	>: Discharge S	ource Select b	its				
	111 = CLC2 output							
	110 = CLC1 (output						
	101 = Reserv	/ed; do not use						
	100 = A/D en	d of conversion	n signal					
	011 = SCCP5 auxiliary output							

- 110 = MCCP2 auxiliary output 001 = MCCP1 auxiliary output
- 000 = No discharge source selected, use the IDISSEN bit

25.0 SPECIAL FEATURES

- **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Watchdog Timer, High-Level Device Integration and Programming Diagnostics, refer to the individual sections of the *"PIC24F Family Reference Manual"* provided below:
 - "Watchdog Timer (WDT)" (DS39697)
 - "Programming and Diagnostics" (DS39716)

PIC24FXXXXX family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

25.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped, starting at program memory location, F80000h. A complete list of Configuration register locations is provided in Table 25-1. A detailed explanation of the various bit functions is provided in Register 25-1 through Register 25-9.

The address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using Table Reads and Table Writes.

TABLE 25-1: CONFIGURATION REGISTERS LOCATIONS

Configuration Register	Address			
FBS	F80000			
FGS	F80004			
FOSCSEL	F80006			
FOSC	F80008			
FWDT	F8000A			
FPOR	F8000C			
FICD	F8000E			

REGISTER 25-1: FBS: BOOT SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	BSS2	BSS1	BSS0	BWRP
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-4 Unimplemented: Read as '0'

- bit 3-1 BSS<2:0>: Boot Segment Program Flash Code Protection bits
 - 111 = No boot program Flash segment
 - 011 = Reserved
 - 110 = Standard security, boot program Flash segment starts at 200h, ends at 000AFEh
 - 010 = High-security, boot program Flash segment starts at 200h, ends at 000AFEh
 - 101 = Standard security, boot program Flash segment starts at 200h, ends at 0015FEh⁽¹⁾
 - 001 = High-security, boot program Flash segment starts at 200h, ends at 0015FEh⁽¹⁾
 - 100 = Reserved
 - 000 = Reserved

bit 0 BWRP: Boot Segment Program Flash Write Protection bit

- 1 = Boot Segment may be written
- 0 = Boot Segment is write-protected

Note 1: This selection should not be used in PIC24FV08KMXXX devices.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimension	n Limits	MIN	NOM	MAX			
Number of Pins	Ν		28				
Pitch	е		0.65 BSC				
Overall Height	Α	0.80	0.90	1.00			
Standoff	A1	0.00	0.02	0.05			
Contact Thickness	A3	0.20 REF					
Overall Width	E	6.00 BSC					
Exposed Pad Width	E2	3.65	3.70	4.20			
Overall Length	D		6.00 BSC				
Exposed Pad Length	D2	3.65	3.70	4.20			
Contact Width	b	0.23	0.30	0.35			
Contact Length	L	0.50	0.55	0.70			
Contact-to-Exposed Pad	K	0.20	-	-			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	48		
Pitch	е	0.40 BSC		
Overall Height	А	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.127 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.45	4.60	4.75
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.45	4.60	4.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	ĸ	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	Е	0.40 BSC			
Optional Center Pad Width	W2			4.45	
Optional Center Pad Length	T2			4.45	
Contact Pad Spacing	C1		6.00		
Contact Pad Spacing	C2		6.00		
Contact Pad Width (X28)	X1			0.20	
Contact Pad Length (X28)	Y1			0.80	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A