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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km204t-i-ml

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4.0 MEMORY ORGANIZATION

As with Harvard architecture devices, the PIC24F microcontrollers feature separate program and data memory space and busing. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1 **Program Address Space**

The program address memory space of the PIC24F devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from a table operation or Data Space remapping, as described in **Section 4.3 "Interfacing Program and Data Memory Spaces"**.

The user access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FV16KM204 family of devices are displayed in Figure 4-1.



FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES

REGISTER 8-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC
—	—	—	—	—	—	—	DC ⁽¹⁾
bit 15							bit 8

R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC
IPL2 ^(2,3)	IPL1 ^(2,3)	IPL0 ^(2,3)	RA ⁽¹⁾	N ⁽¹⁾	OV ⁽¹⁾	Z ⁽¹⁾	C ⁽¹⁾
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-9 Unimplemented: Read as '0'

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

Note 1: See Register 3-1 for the description of these bits, which are not dedicated to interrupt control functions.

- 2: The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the Interrupt Priority Level if IPL3 = 1.
- 3: The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

Note: Bit 8 and bits 4 through 0 are described in Section 3.0 "CPU".

REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	_	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0, HSC	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽²⁾	PSV ⁽¹⁾	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/C	learable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 Unimplemented: Read as '0'

bit 3 IPL3: CPU Interrupt Priority Level Status bit⁽²⁾ 1 = CPU Interrupt Priority Level is greater than 7 0 = CPU Interrupt Priority Level is 7 or less

bit 1-0 Unimplemented: Read as '0'

Note 1: See Register 3-2 for the description of this bit, which is not dedicated to interrupt control functions.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

Note: Bit 2 is described in Section 3.0 "CPU".

9.3 Control Registers

The operation of the oscillator is controlled by three Special Function Registers (SFRs):

- OSCCON
- CLKDIV
- OSCTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources.

The Clock Divider register (Register 9-2) controls the features associated with Doze mode, as well as the postscaler for the FRC Oscillator.

The FRC Oscillator Tune register (Register 9-3) allows the user to fine-tune the FRC Oscillator over a range of approximately $\pm 5.25\%$. Each bit increment or decrement changes the factory calibrated frequency of the FRC Oscillator by a fixed amount.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-0, HSC	R-0, HSC	R-0, HSC	U-0	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

R/SO-0, HSC	U-0	R-0, HSC ⁽²⁾	U-0	R/CO-0, HS	R/W-0 ⁽³⁾	R/W-0	R/W-0
CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
HS = Hardware Settable bit	CO = Clearable Only bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	COSC<2:0>: Current Oscillator Selection bits
	 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV) 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV) 101 = Low-Power RC Oscillator (LPRC) 100 = Secondary Oscillator (SOSC) 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL) 010 = Primary Oscillator (XT, HS, EC) 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL) 000 = 8 MHz FRC Oscillator (FRC)
bit 11	Unimplemented: Read as '0'
bit 10-8	NOSC<2:0>: New Oscillator Selection bits ⁽¹⁾
	111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
	110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
	000 = 8 MHz FRC Oscillator (FRC)
Note 1:	Reset values for these bits are determined by the FNOSCx Configuration bits.
2:	This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

3: When SOSC is selected to run from a digital clock input, rather than an external crystal (SOSCSRC = 0), this bit has no effect.

9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 25.0** "**Special Features**" for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

- 1. If desired, read the COSCx bits (OSCCON<14:12>) to determine the current oscillator source.
- 2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
- 3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
- 4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
- 5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically, as follows:

- 1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
- If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
- The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
- 4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
- 5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
- The old clock source is turned off at this time, with the exception of LPRC (if WDT, FSCM or RTCC with LPRC as a clock source is enabled) or SOSC (if SOSCEN remains enabled).

Note 1: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.





FIGURE 14-4: MSSPx BLOCK DIAGRAM (I²C[™] MASTER MODE)



REGISTER 14-2: SSPxSTAT: MSSPx STATUS REGISTER (I²C[™] MODE) (CONTINUED)

- BF: Buffer Full Status bit
- In Transmit mode:

bit 0

- 1 = Transmit is in progress, SSPxBUF is full
- 0 = Transmit is complete, SSPxBUF is empty
- In Receive mode:
- 1 = SSPxBUF is full (does not include the \overline{ACK} and Stop bits)
- 0 = SSPxBUF is empty (does not include the \overline{ACK} and Stop bits)
- **Note 1:** This bit is cleared on Reset and when SSPEN is cleared.
 - 2: This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not ACK bit.
 - 3: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSPx is in Active mode.

REGISTER 14-3: SSPxCON1: MSSPx CONTROL REGISTER 1 (SPI MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV ⁽¹⁾	SSPEN ⁽²⁾	CKP	SSPM3 ⁽³⁾	SSPM2 ⁽³⁾	SSPM1 ⁽³⁾	SSPM0 ⁽³⁾
bit 7							bit 0

Legend:				
R = Reada	able bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15-8	Unimple	mented: Read as '0'		
bit 7	WCOL: V	Vrite Collision Detect bit		
	1 = The S softw	SSPxBUF register is written v are)	while it is still transmitting the	previous word (must be cleared in
	0 = No co	ollision		
bit 6	SSPOV:	Master Synchronous Serial P	ort Receive Overflow Indicate	or bit ⁽¹⁾
	<u>SPI Slave</u> 1 = A new flow, SSP: 0 = No o	<u>e mode:</u> w byte is received while the St the data in SSPxSR is lost. (kBUF, even if only transmitting verflow	SPxBUF register is still holding Overflow can only occur in Sla g data, to avoid setting overflow	the previous data. In case of over- ave mode. The user must read the w (must be cleared in software).
bit 5	SSPEN:	Master Synchronous Serial P	ort Enable bit ⁽²⁾	
	1 = Enab 0 = Disab	les the serial port and configues the serial port and config	ares SCKx, SDOx, SDIx and $\overline{\$}$ ures these pins as I/O port pir	SSx as serial port pins
bit 4	CKP: Clo	ck Polarity Select bit		
	1 = Idle s 0 = Idle s	tate for clock is a high level tate for clock is a low level		
bit 3-0	SSPM<3	0>: Master Synchronous Ser	rial Port Mode Select bits ⁽³⁾	
	1010 = S 0101 = S 0010 = S 0011 = S 0010 = S 0001 = S 0000 = S	PI Master mode, Clock = Fos PI Slave mode, Clock = SCK PI Slave mode, Clock = SCK PI Master mode, Clock = TM PI Master mode, Clock = Fos PI Master mode, Clock = Fos	sc/(2 <u>* ([</u> SSPxADD] + 1)) x pin; <u>SSx</u> pin control is disabl (x pin; <u>SSx</u> pin control is enab R2 output/2 sc/32 sc/8 sc/2	ed, SSx can be used as an I/O pin led
Note 1:	In Master mo writing to the	de, the overflow bit is not set SSPxBUF register.	since each new reception (ar	nd transmission) is initiated by

- 2: When enabled, these pins must be properly configured as inputs or outputs.
- **3:** Bit combinations not specifically listed here are either reserved or implemented in I^2C^{TM} mode only.

NOTES:

REGISTER 16-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾ (CONTINUED)

- **Note 1:** The RCFGCAL register is only affected by a POR.
 - 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
 - 3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

REGISTER 17-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER (CONTINUED)

bit 3	G3D2T: Gate 3 Data Source 2 True Enable bit
	1 = The Data Source 2 inverted signal is enabled for Gate 3
	0 = The Data Source 2 inverted signal is disabled for Gate 3
bit 2	G3D2N: Gate 3 Data Source 2 Negated Enable bit
	1 = The Data Source 2 inverted signal is enabled for Gate 3
	0 = The Data Source 2 inverted signal is disabled for Gate 3
bit 1	G3D1T: Gate 3 Data Source 1 True Enable bit
	1 = The Data Source 1 inverted signal is enabled for Gate 3
	0 = The Data Source 1 inverted signal is disabled for Gate 3
bit 0	G3D1N: Gate 3 Data Source 1 Negated Enable bit
	1 = The Data Source 1 inverted signal is enabled for Gate 3
	0 = The Data Source 1 inverted signal is disabled for Gate 3

NOTES:

REGISTER 24-2: CTMUCON1H: CTMU CONTROL 1 HIGH REGISTER (CONTINUED)

- bit 6 EDG2POL: Edge 2 Polarity Select bit 1 = Edge 2 is programmed for a positive edge 0 = Edge 2 is programmed for a negative edge bit 5-2 EDG2SEL<3:0>: Edge 2 Source Select bits 1111 = Edge 2 source is the Comparator 3 output 1110 = Edge 2 source is the Comparator 2 output 1101 = Edge 2 source is the Comparator 1 output 1100 = Unimplemented; do not use 1011 = Edge 2 source is CLC1 1010 = Edge 2 source is the MCCP2 Compare Event (CCP2IF) 1001 = Unimplemented; do not use 1000 = Edge 2 source is CTED13 0111 = Edge 2 source is CTED12 0110 = Edge 2 source is CTED11⁽²⁾ 0101 = Edge 2 source is CTED10 0100 = Edge 2 source is CTED9⁽²⁾ 0011 = Edge 2 source is CTED1 0010 = Edge 2 source is CTED2 0001 = Edge 2 source is the MCCP1 Compare Event (CCP1IF) 0000 = Edge 2 source is Timer1
- bit 1-0 Unimplemented: Read as '0'
- Note 1: Edge sources, CTED7 and CTED8, are not available on 28-pin and 20-pin devices.
 - 2: Edge sources, CTED3, CTED9 and CTED11, are not available on 20-pin devices.

REGISTER 25-7: FICD: IN-CIRCUIT DEBUGGER CONFIGURATION REGISTER

R/P-1	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
DEBUG		—	_	_	_	FICD1	FICD0
bit 7							bit 0
Legend:							
R = Readab	le bit	P = Programn	nable bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 7	DEBUG: Back	ground Debugg	er Enable bit				
	1 = Backgroun 0 = Backgroun	d debugger is o d debugger fun	lisabled ctions are ena	bled			
bit 6-2	Unimplemente	ed: Read as '0'					
bit 1-0	FICD<1:0:>: IC	D Pin Select b	its				
	11 = PGEC1/P 10 = PGEC2/P 01 = PGEC3/P 00 = Reserved	GED1 are use GED2 are use GED3 are use ; do not use	d for programm d for programm d for programm	ning and debug ning and debug ning and debug	ging the device ging the device ging the device	9 9 9	







DC CHARACTERISTICS			Standard	l Operatin g tempera	g Conditio ture	ons: 1.8V 2.0V -40°0 -40°0	to 3.6V (PIC24F1 to 5.5V (PIC24F\ C ≤ TA ≤ +85°C fc C ≤ TA ≤ +125°C f	6KM204) /16KM204) or Industrial for Extended
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conc	litions
	Vol	Output Low Voltage						
DO10		All I/O Pins	_	—	0.4	V	IOL = 8.0 mA	VDD = 4.5V
			_	—	0.4	V	IOL = 4.0 mA	VDD = 3.6V
			_	—	0.4	V	IOL = 3.5 mA	VDD = 2.0V
DO16		OSC2/CLKO	_	—	0.4	V	IOL = 2.0 mA	VDD = 4.5V
			_	—	0.4	V	IOL = 1.2 mA	VDD = 3.6V
			_	—	0.4	V	IOL = 0.4 mA	VDD = 2.0V
	Vон	Output High Voltage						
DO20		All I/O Pins	3.8	—	—	V	Iон = -3.5 mA	VDD = 4.5V
			3	—	—	V	Iон = -3.0 mA	VDD = 3.6V
			1.6	_	—	V	Іон = -1.0 mA	VDD = 2.0V
DO26		OSC2/CLKO	3.8	—	—	V	Іон = -2.0 mA	VDD = 4.5V
			3	—	—	V	Іон = -1.0 mA	VDD = 3.6V
			1.6	_	_	V	Іон = -0.5 mA	VDD = 2.0V

TABLE 27-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 27-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating	Operatin tempera	g Conditi ture	ons: 1.8 2.0 -40 -40	V to 3.6V (PIC24F16KM204) V to 5.5V (PIC24FV16KM204) $^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $^{\circ}C \le TA \le +125^{\circ}C$ for Extended	
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units Conditions		
		Program Flash Memory						
D130	Ер	Cell Endurance	10,000 ⁽²⁾	_	—	E/W		
D131	Vpr	VDD for Read	VMIN	_	3.6	V	VMIN = Minimum operating voltage	
D133A	Tiw	Self-Timed Write Cycle Time	—	2	—	ms		
D134	Tretd	Characteristic Retention	40	_	—	Year	Provided no other specifications are violated	
D135	IDDP	Supply Current During Programming	—	10	—	mA		

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Self-write and block erase.

27.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FV16KM204 family AC characteristics and timing parameters.

TABLE 27-18: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions:	1.8V to 3.6V
	Operating temperature	-40°C \leq TA \leq +85°C for Industrial
AC CHARACTERISTICS		-40°C \leq TA \leq +125°C for Extended
	Operating voltage VDD range as des	scribed in Section 27.1 "DC Characteristics".

FIGURE 27-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 27-19: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO50	Cosc2	OSCO/CLKO Pin	_	—	15	pF	In XT and HS modes when External Clock is used to drive OSCI
DO56	Сю	All I/O Pins and OSCO	_	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	—		400	pF	In I ² C™ mode

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.



TABLE 27-38: A/D CONVERSION TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS Ope			Standar Operatir	Standard Operating Condition			pns: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended		
Param No.	Sym	Characteristic	Min.	Тур	Max.	Units	Conditions		
			Clock P	aramete	rs				
AD50	Tad	A/D Clock Period	600	—	—	ns	Tcy = 75 ns, AD1CON3 in default state		
AD51	TRC	A/D Internal RC Oscillator Period		1.67	—	μs			
			Conver	sion Rat	е				
AD55	Τςονν	Conversion Time	—	12 14		Tad Tad	10-bit results 12-bit results		
AD56	FCNV	Throughput Rate			100	ksps			
AD57	TSAMP	Sample Time		1	—	TAD			
AD58	TACQ	Acquisition Time	750	—	—	ns	(Note 2)		
AD59	Tswc	Switching Time from Convert to Sample	—	—	(Note 3)				
AD60	TDIS	Discharge Time	12	—	—	TAD			
			Clock P	aramete	rs				
AD61	TPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	_	3	TAD			

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

- 2: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to Vss or Vss to VDD).
- 3: On the following cycle of the device clock.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			
Dimension	MIN	NOM	MAX	
Number of Pins	N		28	
Pitch	е		0.65 BSC	
Overall Height	А	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	С	0.09	-	0.25
Foot Angle	¢	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

NOTES: