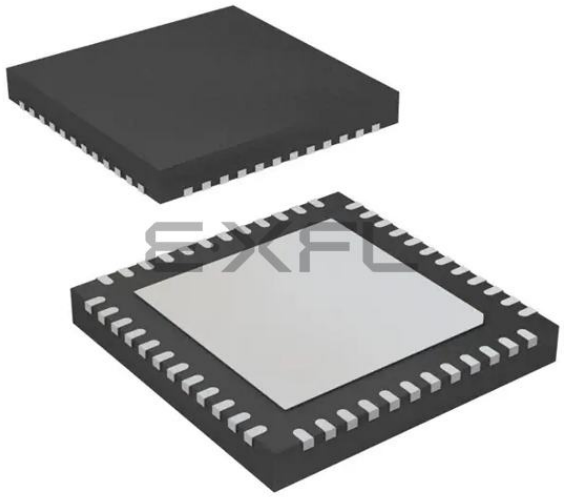

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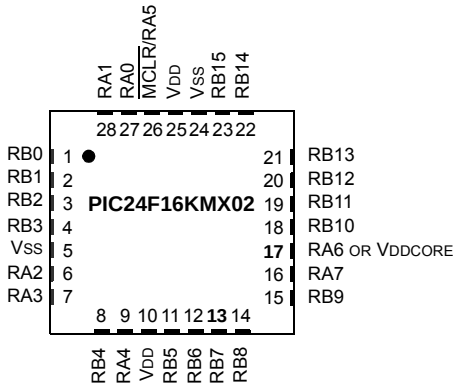
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 22x10b/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fv16km204t-i-mv

Pin Diagrams (Continued)

28-Pin QFN(1)



Pin	Pin Features	Pin Features
	PIC24FXXKMX02	PIC24FVXXKMX02
1	PGED1/AN2/CTCMP/ULPWU/C1IND/ / / /CN4/RB0	
2	PGEC1/ / /AN3/C1INC/ / /CTED12/CN5/RB1	
3	/ /AN4/C1INB/ / /U1RX/TCKIB/CTED13/CN6/RB2	
4	/AN5/C1INA/ / /CN7/RB3	
5	VSS	
6	OSCI/CLKI/AN13/CN30/RA2	
7	OSCO/CLKO/AN14/CN29/RA3	
8	SOSCI/AN15/ / /CN1/RB4	
9	SOSCO/SCLKI/AN16/PWRLCLK/ /CN0/RA4	
10	VDD	
11	PGED3/AN17/ASDA1/ / /OC1E/CLCINA/CN27/RB5	
12	PGEC3/AN18/ASCL1/ / /OC1F/CLCINB/CN24/RB6	
13	AN19/U1TX/INT0/CN23/RB7	AN19/U1TX/ /OC1A/INT0/CN23/RB7
14	AN20/SCL1/$\overline{\text{U1CTS}}$/C3OUT/OC1B/CTED10/CN22/RB8	
15	AN21/SDA1/T1CK/$\overline{\text{U1RTS}}$/U1BCLK/IC2/ /CLC1O/CTED4/CN21/RB9	
16	/IC1/ / /CTED3/CN9/RA7	
17	/OC1A/CTED1/INT2/CN8/RA6	VDDCORE/VCAP
18	PGED2/SDI1/ /OC1C/CTED11/CN16/RB10	
19	PGEC2/SCK1/OC2A/CTED9/CN15/RB11	
20	/AN12/HLVDIN/ / / /CTED2/CN14/RB12	/AN12/HLVDIN/$\overline{\text{SS2}}$/ / /CTED2/INT2/CN14/RB12
21	/ /AN11/SDO1/OCFB/OC3B/OC1D/CTPLS/CN13/RB13	
22	/CVREF/ / /AN10/ / /C1OUT/OCFA/CTED5/INT1/CN12/RB14	
23	/ /AN9/ /REFO/$\overline{\text{SS1}}$/TCKIA/CTED6/CN11/RB15	
24	VSS	
25	VDD	
26	$\overline{\text{MCLR}}$/VPP/RA5	
27	CVREF+/VREF+/ /AN0/ /CN2/RA0	CVREF+/VREF+/ /AN0/ /CTED1/CN2/RA0
28	CVREF-/VREF-/AN1/CN3/RA1	

Legend: Values in indicate pin function differences between PIC24F(V)XXKM202 and PIC24F(V)XXKM102 devices.

Note 1: Exposed pad on underside of device is connected to VSS.

TABLE 1-5: PIC24FV16KM204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Function	F					FV					I/O	Buffer	Description
	Pin Number					Pin Number							
	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin PDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN			
CTED1	11	20	17	7	7	11	2	27	19	21	I	ST	CTMU Trigger Edge Inputs
CTED2	15	23	20	10	11	15	23	20	10	11	I	ST	CTMU Trigger Edge Inputs
CTED3	—	19	16	6	6	—	19	16	6	6	I	ST	CTMU Trigger Edge Inputs
CTED4	13	18	15	1	1	13	18	15	1	1	I	ST	CTMU Trigger Edge Inputs
CTED5	17	25	22	14	15	17	25	22	14	15	I	ST	CTMU Trigger Edge Inputs
CTED6	18	26	23	15	16	18	26	23	15	16	I	ST	CTMU Trigger Edge Inputs
CTED7	—	—	—	5	5	—	—	—	5	5	I	ST	CTMU Trigger Edge Inputs
CTED8	—	—	—	13	14	—	—	—	13	14	I	ST	CTMU Trigger Edge Inputs
CTED9	—	22	19	9	10	—	22	19	9	10	I	ST	CTMU Trigger Edge Inputs
CTED10	12	17	14	44	48	12	17	14	44	48	I	ST	CTMU Trigger Edge Inputs
CTED11	—	21	18	8	9	—	21	18	8	9	I	ST	CTMU Trigger Edge Inputs
CTED12	5	5	2	22	24	5	5	2	22	24	I	ST	CTMU Trigger Edge Inputs
CTED13	6	6	3	23	25	6	6	3	23	25	I	ST	CTMU Trigger Edge Inputs
CTPLS	16	24	21	11	12	16	24	21	11	12	O	—	CTMU Pulse Output
CV_{REF}	17	25	22	14	15	17	25	22	14	15	O	ANA	Comparator Voltage Reference Output
CV_{REF+}	2	2	27	19	21	2	2	27	19	21	I	ANA	Comparator Voltage Reference Positive Input
CV_{REF-}	3	3	28	20	22	3	3	28	20	22	I	ANA	Comparator Voltage Reference Negative Input
DAC1OUT	—	23	20	10	11	—	23	20	10	11	O	ANA	DAC1 Output
DAC1REF+	—	2	27	19	21	—	2	27	19	21	I	ANA	DAC1 Positive Voltage Reference Input
DAC2OUT	—	25	22	14	15	—	25	22	14	15	O	ANA	DAC2 Output
DAC2REF+	—	26	23	15	16	—	26	23	15	16	I	ANA	DAC2 Positive Voltage Reference Input
HLVDIN	15	23	20	10	11	15	23	20	10	11	I	ANA	External High/Low-Voltage Detect Input
IC1	14	19	16	6	6	11	19	16	6	6	I	ST	MCCP1 Input Capture Input
IC2	13	18	15	1	1	13	18	15	1	1	I	ST	MCCP2 Input Capture Input
IC3	—	23	20	13	14	—	23	20	13	14	I	ST	MCCP3 Input Capture Input
IC4	—	14	11	5	5	—	14	11	5	5	I	ST	SCCP4 Input Capture Input
IC5	—	15	12	12	13	—	15	12	12	13	I	ST	SCCP5 Input Capture Input
INT0	11	16	13	43	47	11	16	13	43	47	I	ST	External Interrupt 0 Input
INT1	17	25	22	14	15	17	25	22	14	15	I	ST	External Interrupt 1 Input
INT2	14	20	17	7	7	15	23	20	10	11	I	ST	External Interrupt 2 Input

Legend: ANA = Analog level input/output, ST = Schmitt Trigger input buffer, I^2C™ = I^2C/SMBus input buffer

NOTES:

3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the *"PIC24F Family Reference Manual"*, **"CPU"** (DS39703).

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into program space at any 16K word boundary of either program memory or data EEPROM memory, defined by the 8-bit Program Space Visibility Page Address (PSVPAG) register. The program to Data Space mapping feature lets any instruction access program space as if it were Data Space.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs.

The core supports Inherent (no operand), Relative, Literal, Memory Direct and three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (i.e., A + B = C) to be executed in a single cycle.

A high-speed, 17-bit by 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit by 16-bit or 8-bit by 8-bit integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is illustrated in Figure 3-1.

3.1 Programmer's Model

Figure 3-2 displays the programmer's model for the PIC24F. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions.

Table 3-1 provides a description of each register. All registers associated with the programmer's model are memory mapped.

4.2 Data Address Space

The PIC24F core has a separate, 16-bit-wide data memory space, addressable as a single linear range. The Data Space is accessed using two Address Generation Units (AGUs), one each for read and write operations. The Data Space memory map is displayed in Figure 4-3.

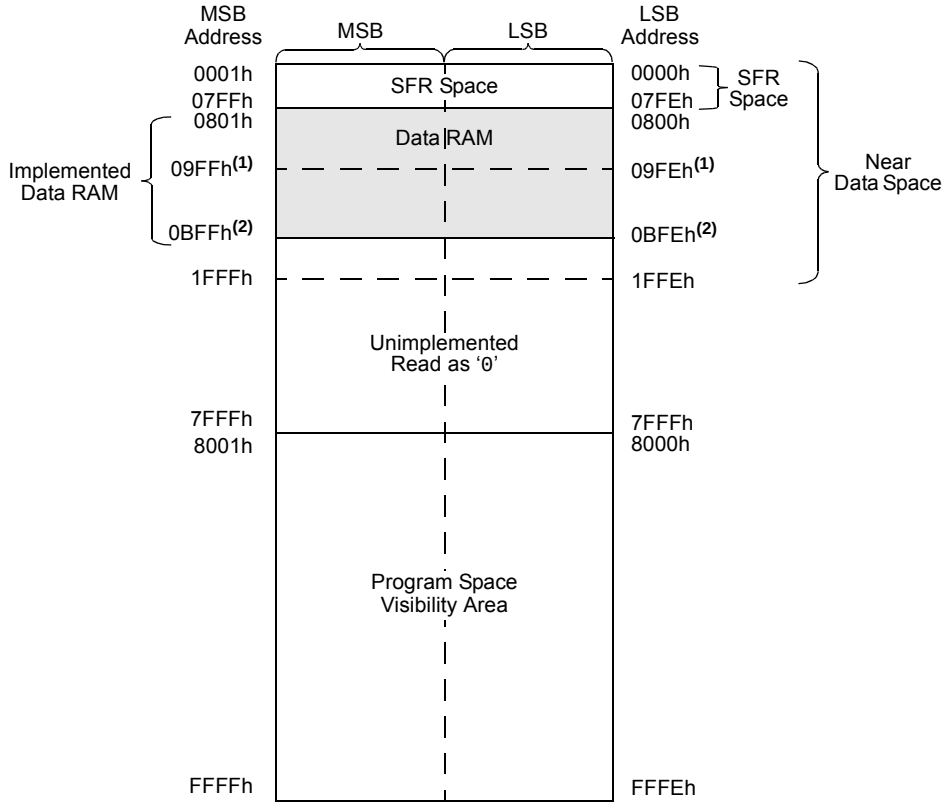
All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This gives a Data Space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility (PSV) area (see **Section 4.3.3 "Reading Data From Program Memory Using Program Space Visibility"**).

Depending on the particular device, PIC24FV16KM family devices implement either 512 or 1024 words of data memory. Should an EA point to a location outside of this area, an all zero word or byte will be returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all the Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

FIGURE 4-3: DATA SPACE MEMORY MAP FOR PIC24FXXXXX FAMILY DEVICES(3)



Note 1: Upper data memory boundary for PIC24FXXKM10X devices.
2: Upper data memory boundary for PIC24FXXKM20X devices.
3: Data memory areas are not shown to scale.

TABLE 4-31: CLOCK CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	740h	TRAPR	IOPUWR	SBOREN	RETEN	—	—	CM	PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	(Note 1)
OSCCON	742h	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	—	LOCK	—	CF	SOSCDRV	SOSCEN	OSWEN	(Note 2)
CLKDIV	744h	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	—	—	—	—	—	—	—	—	0100
OSCTUN	748h	—	—	—	—	—	—	—	—	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000
REFOCON	74Eh	ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
HLVDCON	756h	HLVDEN	—	HLSIDL	—	—	—	—	—	VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on Configuration fuses and by type of Reset.

TABLE 4-32: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	760h	WR	WREN	WRERR	PGMONLY	—	—	—	—	—	ERASE	NVMOP5	NVMOP4	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMKEY	766h	—	—	—	—	—	—	—	—	NVMKEY7	NVMKEY6	NVMKEY5	NVMKEY4	NVMKEY3	NVMKEY2	NVMKEY1	NVMKEY0	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-33: ULTRA LOW-POWER WAKE-UP REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ULPWCON	768h	ULPEN	—	ULPSIDL	—	—	—	—	ULPSINK	—	—	—	—	—	—	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.

TABLE 4-34: PMD REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	770h	—	—	—	—	T1MD	—	—	—	SSP1MD	U2MD(1)	U1MD	—	—	—	—	ADCMD	0000
PMD2	772h	—	—	—	—	—	—	—	—	—	—	—	CCP5MD(1)	CCP4MD(1)	CCP3MD(1)	CCP2MD	CCP1MD	0000
PMD3	774h	—	—	—	—	—	CMPMD	RTCCMD	—	—	DAC1MD(1)	—	—	—	—	SSP2MD(1)	—	0000
PMD4	776h	—	—	—	—	—	—	—	—	—	ULPWUMD	—	—	REFOMD	CTMUMD	HLVDMD	—	0000
PMD6	77Ah	—	—	—	—	—	—	—	—	—	—	AMP1MD(1)	DAC2MD(1)	AMP2MD(1)	—	—	—	0000
PMD8	77Eh	—	—	—	—	—	—	—	—	—	—	—	—	CLC2MD(1)	CLC1MD	—	—	0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, r = reserved.
Note 1: These bits are available only on PIC24F(V)16KM2XX devices.

REGISTER 8-13: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
U2TXIE	U2RXIE	INT2IE	CCT4IE	CCT3IE	—	—	—
bit 15							bit 8

U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CCP5IE	—	INT1IE	CNIE	CMIE	BCL1IE	SSP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **CCT4IE:** Capture/Compare 4 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **CCT3IE:** Capture/Compare 3 Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10-7 **Unimplemented:** Read as '0'

bit 6 **CCP5IE:** Capture/Compare 5 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **BCL1IE:** MSSP1 I^2C™ Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SSP1IE:** MSSP1 SPI/I^2C Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

NOTES:

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19.1 A/D Control Registers

The 12-bit A/D Converter module uses up to 43 registers for its operation. All registers are mapped in the data memory space.

19.1.1 CONTROL REGISTERS

Depending on the specific device, the module has up to eleven control and status registers:

- AD1CON1: A/D Control Register 1
- AD1CON2: A/D Control Register 2
- AD1CON3: A/D Control Register 3
- AD1CON5: A/D Control Register 5
- AD1CHS: A/D Sample Select Register
- AD1CHITH and AD1CHITL: A/D Scan Compare Hit Registers
- AD1CSSH and AD1CSSL: A/D Input Scan Select Registers
- AD1CTMENH and AD1CTMENL: CTMU Enable Registers

The AD1CON1, AD1CON2 and AD1CON3 registers (Register 19-1, Register 19-2 and Register 19-3) control the overall operation of the A/D module. This includes enabling the module, configuring the conversion clock and voltage reference sources, selecting the sampling and conversion Triggers, and manually controlling the sample/convert sequences. The AD1CON5 register (Register 19-4) specifically controls features of the Threshold Detect operation, including its function in power-saving modes.

The AD1CHS register (Register 19-5) selects the input channels to be connected to the S/H amplifier. It also allows the choice of input multiplexers and the selection of a reference source for differential sampling.

The AD1CHITH and AD1CHITL registers (Register 19-6 and Register 19-7) are semaphore registers used with Threshold Detect operations. The status of individual bits, or bit pairs in some cases, indicates if a match condition has occurred. AD1CHITL is always implemented, whereas AD1CHITH may not be implemented in devices with 16 or fewer channels.

The AD1CSSH/L registers (Register 19-8 and Register 19-9) select the channels to be included for sequential scanning.

The AD1CTMENH/L registers (Register 19-10 and Register 19-11) select the channel(s) to be used by the CTMU during conversions. Selecting a particular channel allows the A/D Converter to control the CTMU (particularly, its current source) and read its data through that channel. AD1CTMENL is always implemented, whereas AD1CTMENH may not be implemented in devices with 16 or fewer channels.

19.1.2 A/D RESULT BUFFERS

The module incorporates a multi-word, dual port buffer, called ADC1BUFx. Each of the locations is mapped into the data memory space and is separately addressable. The buffer locations are referred to as ADC1BUF0 through ADC1BUFx (x = up to 17).

The A/D result buffers are both readable and writable. When the module is active (AD1CON<15> = 1), the buffers are read-only and store the results of A/D conversions. When the module is inactive (AD1CON<15> = 0), the buffers are both readable and writable. In this state, writing to a buffer location programs a conversion threshold for Threshold Detect operations.

Buffer contents are not cleared when the module is deactivated with the ADON bit (AD1CON1<15>). Conversion results and any programmed threshold values are maintained when ADON is set or cleared.

REGISTER 19-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS(1)	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM(1)	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG<1:0>:** A/D Converter Positive Voltage Reference Configuration bits
11 = 4 * Internal V_{BG}(2)
10 = 2 * Internal V_{BG}(3)
01 = External V_{REF+}
00 = AV_{DD}

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bits
1 = External V_{REF-}
0 = AV_{SS}

bit 12 **Unimplemented:** Read as '0'

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into a buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ S/H Input for MUX A Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** A/D Buffer Fill Status bit(1)
1 = A/D is filling the upper half of the buffer; user should access data in the lower half
0 = A/D is filling the lower half of the buffer; user should access data in the upper half

bit 6-2 **SMPI<4:0>:** Interrupt Sample Rate Select bits
11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
•
•
•
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

bit 1 **BUFM:** A/D Buffer Fill Mode Select bit(1)
1 = Starts filling the buffer at address, ADC1BUF0, on the first interrupt and ADC1BUF(x/2) on the next interrupt (Split Buffer mode)
0 = Starts filling the buffer at address, ADC1BUF0, and each sequential address on successive interrupts (FIFO mode)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
0 = Always uses channel input selects for Sample A

Note 1: This is only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.
2: PIC24FV16KMXXX devices only. Reference setting will not be within specification for V_{DD} below 4.5V.
3: Reference setting will not be within specification for V_{DD} below 2.3V.

REGISTER 21-1: AMPxCON: OP AMP x CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
AMPEN	—	AMPSIDL	AMPSLP	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	—	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AMPEN:** Op Amp x Control Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **AMPSIDL:** Op Amp x Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **AMPSLP:** Op Amp x Peripheral Enabled in Sleep Mode bit
1 = Continues module operation when device enters Sleep mode
0 = Discontinues module operation in Sleep mode

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **SPDSEL:** Op Amp x Power/Speed Select bit
1 = Higher power and bandwidth (faster response time)
0 = Lower power and bandwidth (slower response time)

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **NINSEL<2:0>:** Negative Op Amp Input Select bits
111 = Reserved; do not use
110 = Reserved; do not use
101 = Op amp negative input is connected to the op amp output (voltage follower)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp negative input is connected to the OAxIND pin
001 = Op amp negative input is connected to the OAxINB pin
000 = Op amp negative input is connected to AVSS

bit 2-0 **PINSEL<2:0>:** Positive Op Amp Input Select bits
111 = Op amp positive input is connected to the output of the A/D input multiplexer
110 = Reserved; do not use
101 = Op amp positive input is connected to the DAC1 output for OA1 (DAC2 output for OA2)
100 = Reserved; do not use
011 = Reserved; do not use
010 = Op amp positive input is connected to the OAxINC pin
001 = Op amp positive input is connected to the OAxINA pin
000 = Op amp positive input is connected to AVSS

Note 1: This register is available only on PIC24F(V)16KM2XX devices.

REGISTER 24-3: CTMUCON2L: CTMU CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DISCHS2	DISCHS1	DISCHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **IRSTEN:** CTMU Current Source Reset Enable bit
1 = Signal selected by the DISCHS<2:0> bits or the IDISSEN control bit will reset the CTMU edge detect logic
0 = CTMU edge detect logic will not occur

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DISCHS<2:0>:** Discharge Source Select bits
111 = CLC2 output
110 = CLC1 output
101 = Reserved; do not use.
100 = A/D end of conversion signal
011 = SCCP5 auxiliary output
110 = MCCP2 auxiliary output
001 = MCCP1 auxiliary output
000 = No discharge source selected, use the IDISSEN bit

REGISTER 25-4: FOSC: OSCILLATOR CONFIGURATION REGISTER

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCKSM1	FCKSM0	SOSCSEL	POSCFREQ1	POSCFREQ0	OSCIOFNC	POSCMD1	POSCMD0
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **SOSCSEL:** Secondary Oscillator Power Selection Configuration bit
1 = Secondary Oscillator is configured for high-power operation
0 = Secondary Oscillator is configured for low-power operation

bit 4-3 **POSCFREQ<1:0>:** Primary Oscillator Frequency Range Configuration bits
11 = Primary Oscillator/External Clock input frequency is greater than 8 MHz
10 = Primary Oscillator/External Clock input frequency is between 100 kHz and 8 MHz
01 = Primary Oscillator/External Clock input frequency is less than 100 kHz
00 = Reserved; do not use

bit 2 **OSCIOFNC:** CLKO Enable Configuration bit
1 = CLKO output signal is active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock (EC) mode for the CLKO to be active (POSCMD<1:0> = 11 or 00)
0 = CLKO output is disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator mode is disabled
10 = HS Oscillator mode is selected
01 = XT Oscillator mode is selected
00 = External Clock mode is selected

FIGURE 27-9: BROWN-OUT RESET CHARACTERISTICS

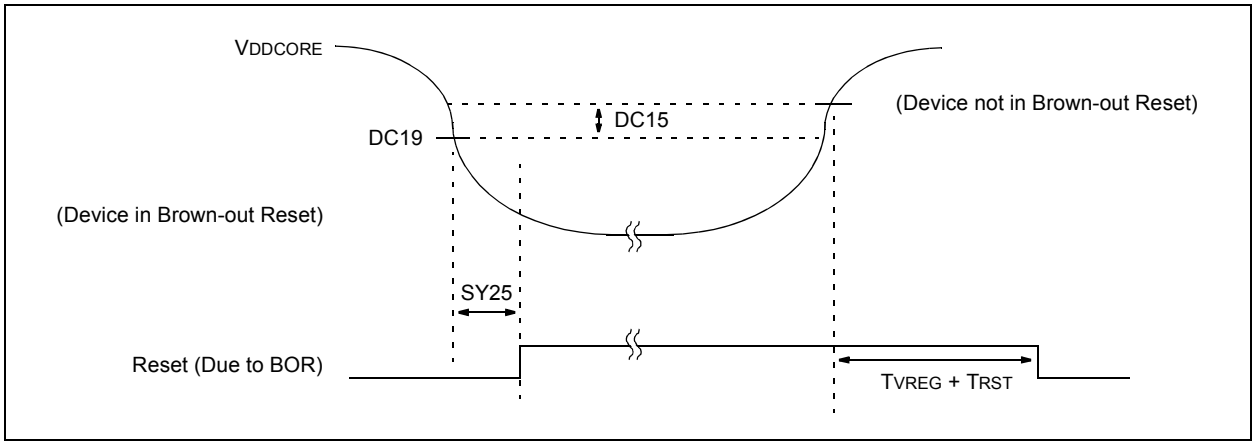


TABLE 27-25: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
SY10	TmcL	MCLR Pulse Width (low)	2	—	—	µs	
SY11	TPWRT	Power-up Timer Period	50	64	90	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	µs	
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1.32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	µs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	2.0	2.3	µs	
SY45	TRST	Internal State Reset Time	—	5	—	µs	
SY50	TVREG	On-Chip Voltage Regulator Output Delay	—	10	—	µs	**(Note 2)**
SY55	TLOCK	PLL Start-up Time	—	100	—	µs	
SY65	TOST	Oscillator Start-up Time	—	1024	—	TOSC	
SY71	TPM	Program Memory Wake-up Time	—	1	—	µs	Sleep wake-up with PMSLP = 0
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	250	—	µs	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: This applies to PIC24FV16KMXXX devices only.

TABLE 27-26: COMPARATOR TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
300	TRESP	Response Time*(1)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	μs	

* Parameters are characterized but not tested.

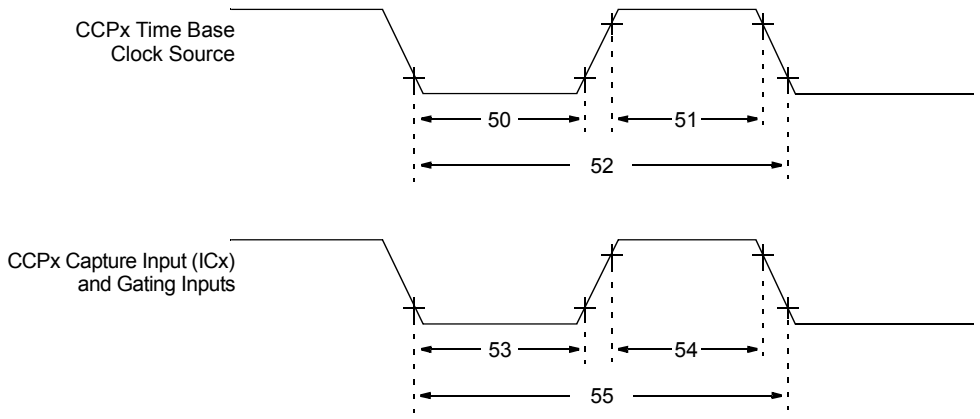
Note 1: Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 27-27: COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Comments
VR310	TSET	Settling Time(1)	—	—	10	μs	

Note 1: Settling time is measured while CVRSS = 1 and the CVR<3:0> bits transition from '0000' to '1111'.

FIGURE 27-10: CAPTURE/COMPARE/PWM TIMINGS (MCCPx, SCCPx MODULES)



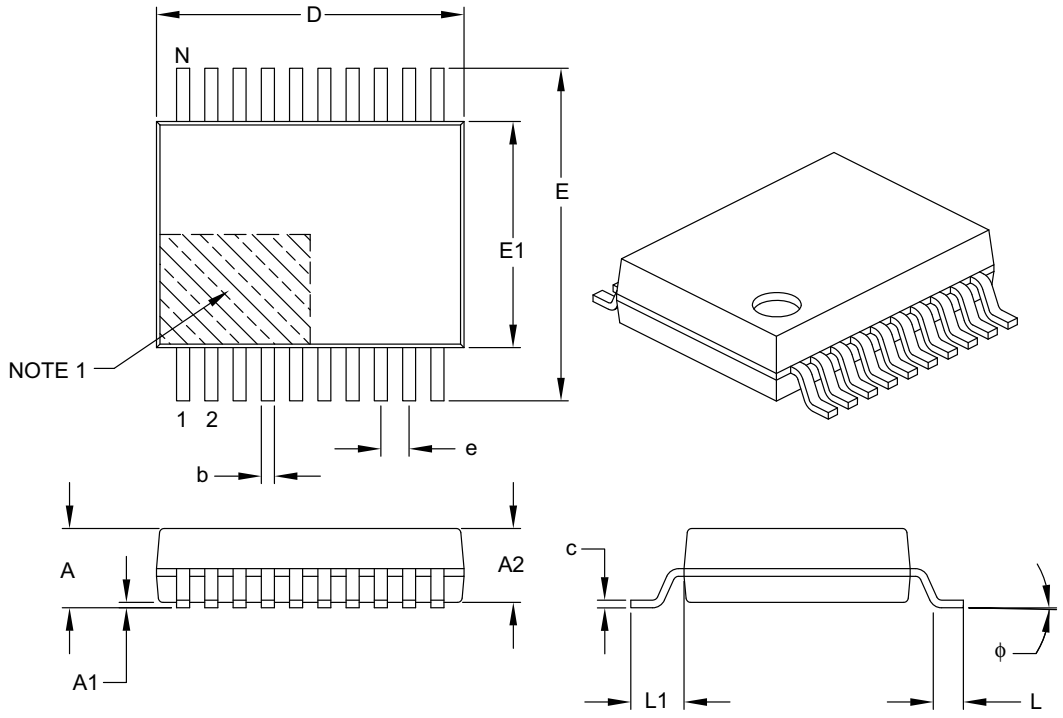
Note: Refer to Figure 27-5 for load conditions.

TABLE 27-28: CAPTURE/COMPARE/PWM REQUIREMENTS (MCCPx, SCCPx MODULES)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
50	TCLKL	CCPx Time Base Clock Source Low Time	TCY/2	—	ns	
51	TCLKH	CCPx Time Base Clock Source High Time	TCY/2	—	ns	
52	TCLK	CCPx Time Base Clock Source Period	TCY	—	ns	
53	TCCL	CCPx Capture or Gating Input Low Time	TCLK	—	ns	
54	TCCH	CCPx Capture or Gating Input High Time	TCLK	—	ns	
55	TCCP	CCPx Capture or Gating Input Period	2 * TCLK/N	—	ns	N = Prescale Value (1, 4 or 16)

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

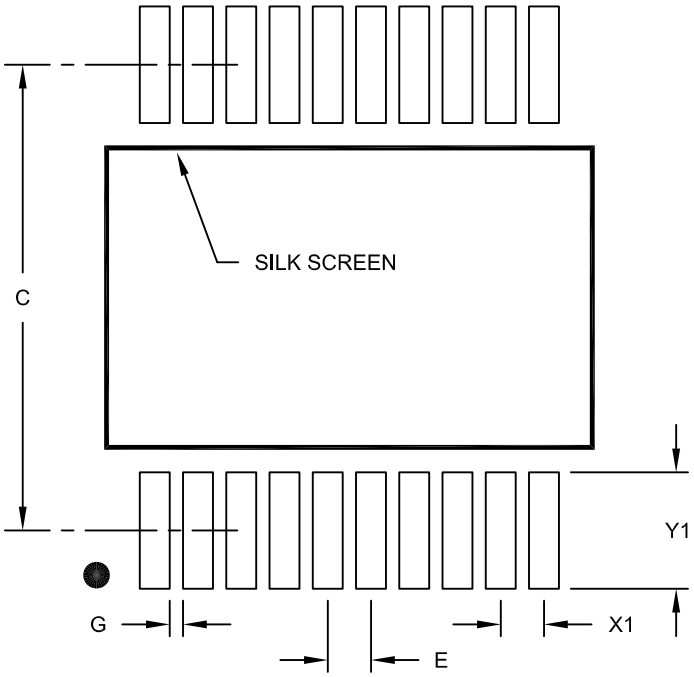
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

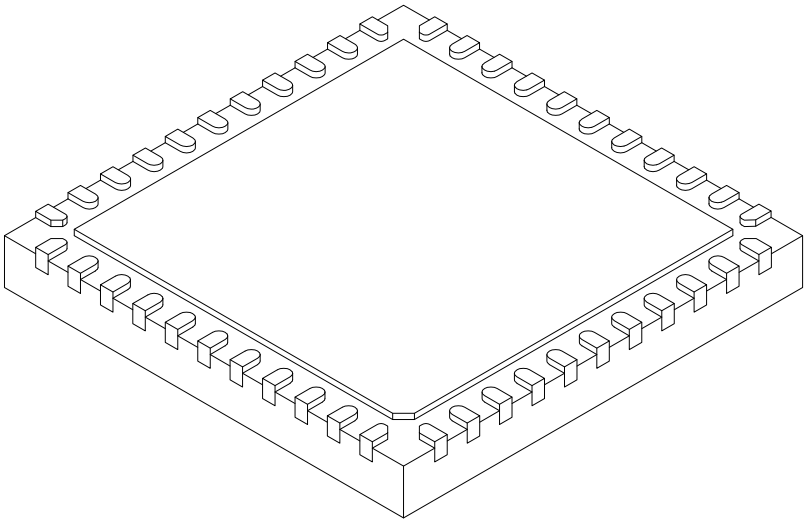
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

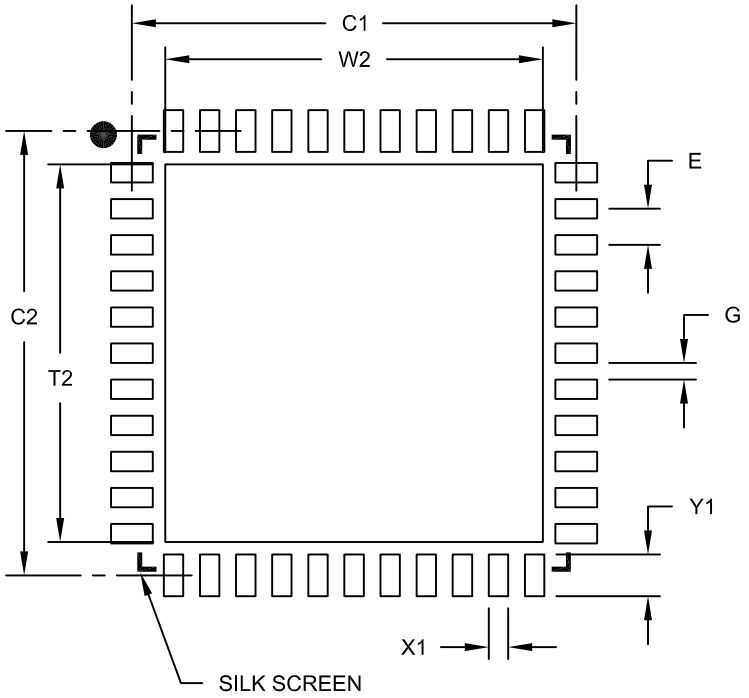
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B