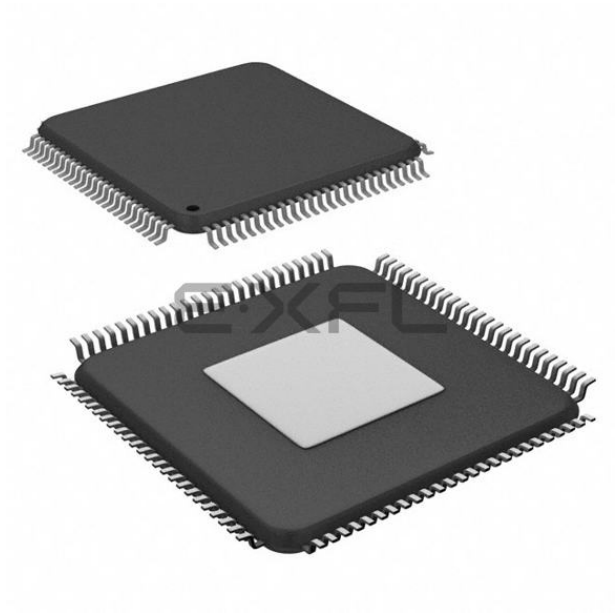
Infineon Technologies - XC2766X96F66LACKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	51K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-3
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2766x96f66lackxuma1

2 General Device Information

The XC2766X derivatives are high-performance members of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

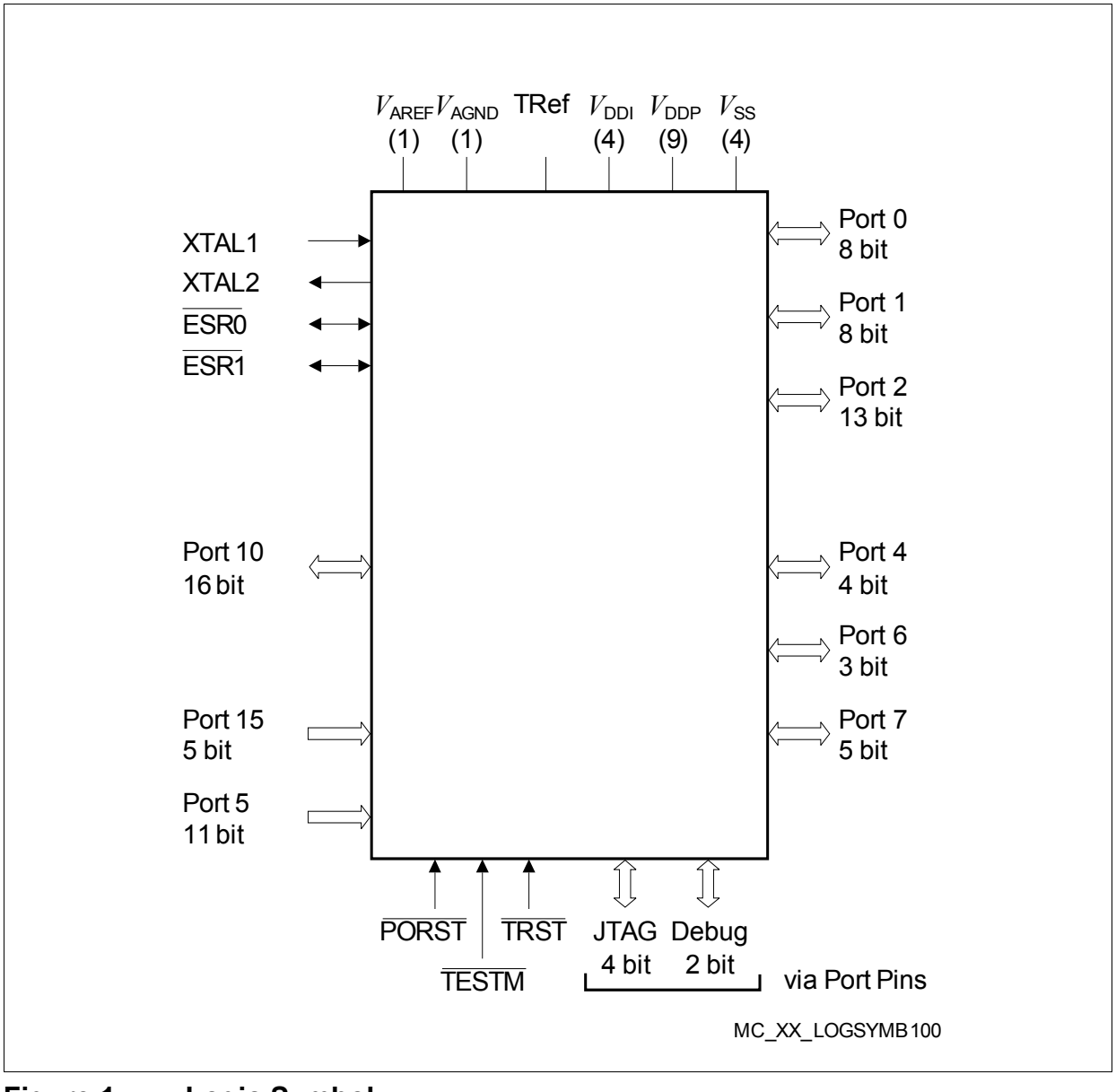

Figure 1 Logic Symbol

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P0.2	O0 / I	St/B	**Bit 2 of Port 0, General Purpose Input/Output**
	U1C0_ SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC62	O3 / I	St/B	**CCU61 Channel 2 Input/Output**
	A2	OH	St/B	**External Bus Interface Address Line 2**
	U1C0_DX1B	I	St/B	**USIC1 Channel 0 Shift Clock Input**
59	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ CC60	O2 / I	St/B	**CCU60 Channel 0 Input/Output**
	AD0	OH / I	St/B	**External Bus Interface Address/Data Line 0**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
60	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_ CC61	O2 / I	St/B	**CCU60 Channel 1 Input/Output**
	AD1	OH / I	St/B	**External Bus Interface Address/Data Line 1**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
93	P1.6	O0 / I	St/B	**Bit 6 of Port 1, General Purpose Input/Output**
	CCU62_ CC61	O1 / I	St/B	**CCU62 Channel 1 Input/Output**
	U1C1_ SELO2	O2	St/B	**USIC1 Channel 1 Select/Control 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	A14	OH	St/B	**External Bus Interface Address Line 14**
	U2C0_DX0D	I	St/B	**USIC2 Channel 0 Shift Data Input**
94	P1.7	O0 / I	St/B	**Bit 7 of Port 1, General Purpose Input/Output**
	CCU62_ CC60	O1 / I	St/B	**CCU62 Channel 0 Input/Output**
	U1C1_ MCLKOUT	O2	St/B	**USIC1 Channel 1 Master Clock Output**
	U2C0_ SCLKOUT	O3	St/B	**USIC2 Channel 0 Shift Clock Output**
	A15	OH	St/B	**External Bus Interface Address Line 15**
	U2C0_DX1C	I	St/B	**USIC2 Channel 0 Shift Clock Input**
95	XTAL2	O	Sp/1	**Crystal Oscillator Amplifier Output**
96	XTAL1	I	Sp/1	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC2766X completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1 Kbyte of on-chip Stand-By SRAM (SBRAM) provides storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

Table 6 XC2766X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'0094$_H$	25$_H$ / 37$_D$
CAPCOM Timer 7	CC2_T7IC	xx'0098$_H$	26$_H$ / 38$_D$
CAPCOM Timer 8	CC2_T8IC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Converter Request 0	ADC_0IC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Converter Request 1	ADC_1IC	xx'00A4$_H$	29$_H$ / 41$_D$
A/D Converter Request 2	ADC_2IC	xx'00A8$_H$	2A$_H$ / 42$_D$
A/D Converter Request 3	ADC_3IC	xx'00AC$_H$	2B$_H$ / 43$_D$
A/D Converter Request 4	ADC_4IC	xx'00B0$_H$	2C$_H$ / 44$_D$
A/D Converter Request 5	ADC_5IC	xx'00B4$_H$	2D$_H$ / 45$_D$
A/D Converter Request 6	ADC_6IC	xx'00B8$_H$	2E$_H$ / 46$_D$
A/D Converter Request 7	ADC_7IC	xx'00BC$_H$	2F$_H$ / 47$_D$
CCU60 Request 0	CCU60_0IC	xx'00C0$_H$	30$_H$ / 48$_D$
CCU60 Request 1	CCU60_1IC	xx'00C4$_H$	31$_H$ / 49$_D$
CCU60 Request 2	CCU60_2IC	xx'00C8$_H$	32$_H$ / 50$_D$
CCU60 Request 3	CCU60_3IC	xx'00CC$_H$	33$_H$ / 51$_D$
CCU61 Request 0	CCU61_0IC	xx'00D0$_H$	34$_H$ / 52$_D$
CCU61 Request 1	CCU61_1IC	xx'00D4$_H$	35$_H$ / 53$_D$
CCU61 Request 2	CCU61_2IC	xx'00D8$_H$	36$_H$ / 54$_D$
CCU61 Request 3	CCU61_3IC	xx'00DC$_H$	37$_H$ / 55$_D$
CCU62 Request 0	CCU62_0IC	xx'00E0$_H$	38$_H$ / 56$_D$
CCU62 Request 1	CCU62_1IC	xx'00E4$_H$	39$_H$ / 57$_D$
CCU62 Request 2	CCU62_2IC	xx'00E8$_H$	3A$_H$ / 58$_D$
CCU62 Request 3	CCU62_3IC	xx'00EC$_H$	3B$_H$ / 59$_D$
CCU63 Request 0	CCU63_0IC	xx'00F0$_H$	3C$_H$ / 60$_D$
CCU63 Request 1	CCU63_1IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CCU63 Request 2	CCU63_2IC	xx'00F8$_H$	3E$_H$ / 62$_D$
CCU63 Request 3	CCU63_3IC	xx'00FC$_H$	3F$_H$ / 63$_D$
CAN Request 0	CAN_0IC	xx'0100$_H$	40$_H$ / 64$_D$
CAN Request 1	CAN_1IC	xx'0104$_H$	41$_H$ / 65$_D$
CAN Request 2	CAN_2IC	xx'0108$_H$	42$_H$ / 66$_D$

Table 6 XC2766X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
Unassigned node	–	xx'0184$_H$	61$_H$ / 97$_D$
Unassigned node	–	xx'0188$_H$	62$_H$ / 98$_D$
Unassigned node	–	xx'018C$_H$	63$_H$ / 99$_D$
Unassigned node	–	xx'0190$_H$	64$_H$ / 100$_D$
Unassigned node	–	xx'0194$_H$	65$_H$ / 101$_D$
Unassigned node	–	xx'0198$_H$	66$_H$ / 102$_D$
Unassigned node	–	xx'019C$_H$	67$_H$ / 103$_D$
Unassigned node	–	xx'01A0$_H$	68$_H$ / 104$_D$
Unassigned node	–	xx'01A4$_H$	69$_H$ / 105$_D$
Unassigned node	–	xx'01A8$_H$	6A$_H$ / 106$_D$
SCU Request 1	SCU_1IC	xx'01AC$_H$	6B$_H$ / 107$_D$
SCU Request 0	SCU_0IC	xx'01B0$_H$	6C$_H$ / 108$_D$
Program Flash Modules	PFM_IC	xx'01B4$_H$	6D$_H$ / 109$_D$
RTC	RTC_IC	xx'01B8$_H$	6E$_H$ / 110$_D$
End of PEC Subchannel	EOPIC	xx'01BC$_H$	6F$_H$ / 111$_D$

1) Register VECSEG defines the segment where the vector table is located.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting with a distance of 4 (two words) between two vectors.

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XC2766X provides a broad range of debug and emulation features. User software running on the XC2766X can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This consists of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the debug interface, or via the external bus interface for increased performance.

The JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

3.7 Capture/Compare Units CCU6x

The XC2766X features four CCU6 units (CCU60, CCU61, CCU62, CCU63).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

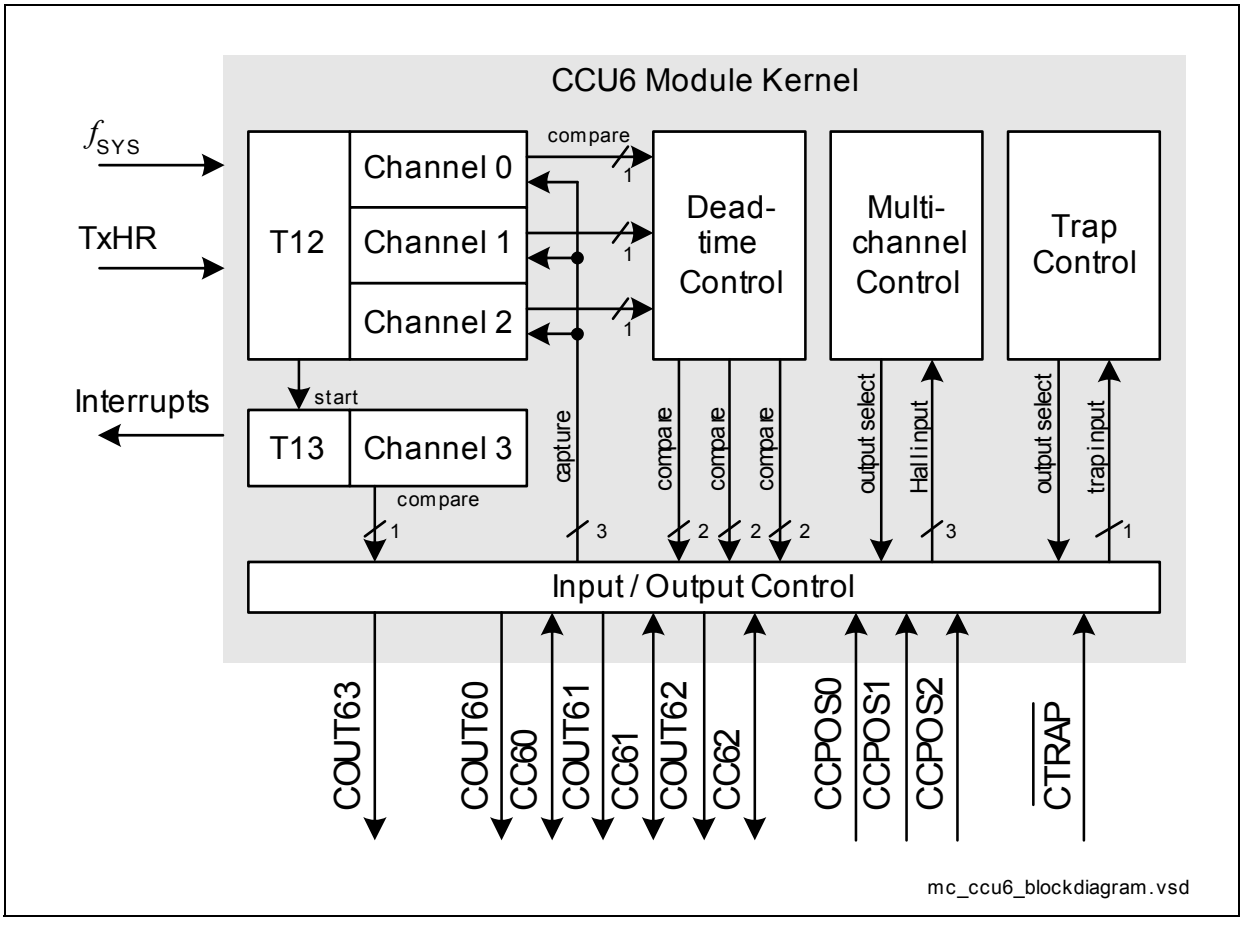

Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

4.2.1 DC Parameters for Upper Voltage Area

These parameters apply to the upper IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Table 14 DC Characteristics for Upper Voltage Range (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input Hysteresis[2)]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DDP} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \ge I_{OHmax}$[3)]
Output high voltage[5)]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5, Port 15)[6)]	I_{OZ1} CC	–	±10	±200	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±5	µA	$T_J \le$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Input leakage current (all other)[6)7)]	I_{OZ2} CC	–	±0.2	±15	µA	$T_J \le$ 150°C, 0.45 V < V_{IN} < V_{DDP}
Pull level keep current	I_{PLK}	–	–	±30	µA	$V_{PIN} \ge V_{IH}$ (up)[8)] $V_{PIN} \le V_{IL}$ (dn)
Pull level force current	I_{PLF}	±250	–	–	µA	$V_{PIN} \le V_{IL}$ (up)[8)] $V_{PIN} \ge V_{IH}$ (dn)
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 13, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.
4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
6) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
   The leakage current value is not tested in the lower voltage range but only in the upper voltage range. This parameter is ensured by correlation.
7) The given values are worst-case values. In production test, this leakage current is only tested at 125°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
   Leakage derating depending on temperature (T_J = junction temperature [°C]):
   I_{OZ} = 0.03 × $e^{(1.35 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 130°C the resulting leakage current is 4.41 µA.
   Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
   I_{OZ} = $I_{OZtempmax}$ - (1.3 × DV) [µA]
   This voltage derating formula is an approximation which applies for maximum temperature.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal leakage.
8) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
   Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
   These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
9) Not subject to production test - verified by design/characterization.
   Because pin P2.8 is connected to two pads (standard pad and high-speed clock pad), it has twice the normal capacitance.

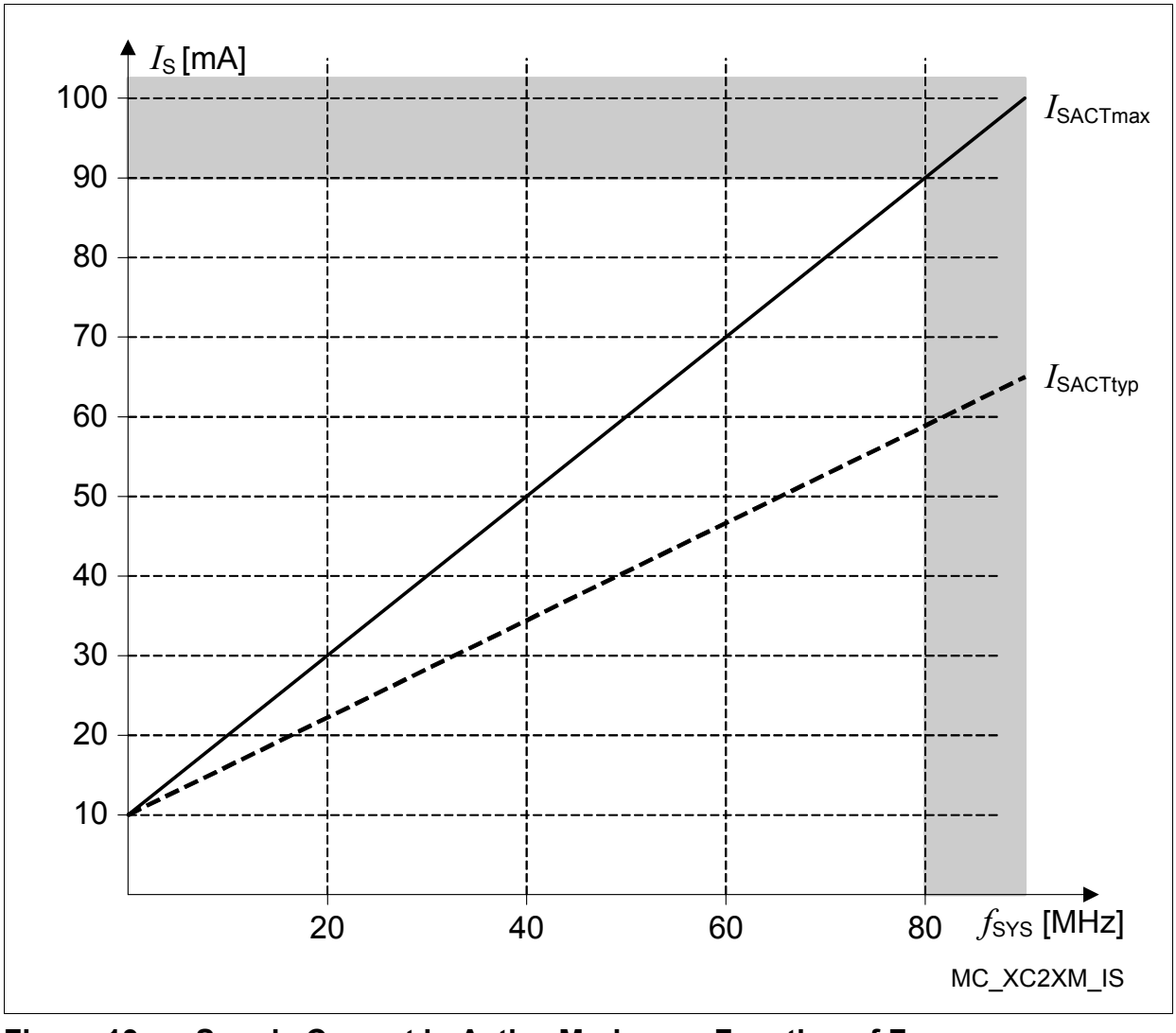

Figure 13 Supply Current in Active Mode as a Function of Frequency

Table 17 Leakage Power Consumption XC2766X (Operating Conditions apply)

Parameter	Sym-bol	Values			Unit	Note / Test Condition[1]
		Min.	Typ.	Max.		
Leakage supply current[2] Formula[3]: 600,000 × $e^{-\alpha}$; α = 5000 / (273 + B×T_J); Typ.: B = 1.0, Max.: B = 1.3	I_{LK1}	–	0.03	0.05	mA	T_J = 25°C
		–	0.5	1.3	mA	T_J = 85°C
		–	2.1	6.2	mA	T_J = 125°C
		–	4.4	13.7	mA	T_J = 150°C

1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

2) The supply current caused by leakage depends mainly on the junction temperature (see **Figure 14**) and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

3) This formula is valid for temperatures above 0°C. For temperatures below 0°C a value of below 10 µA can be assumed.

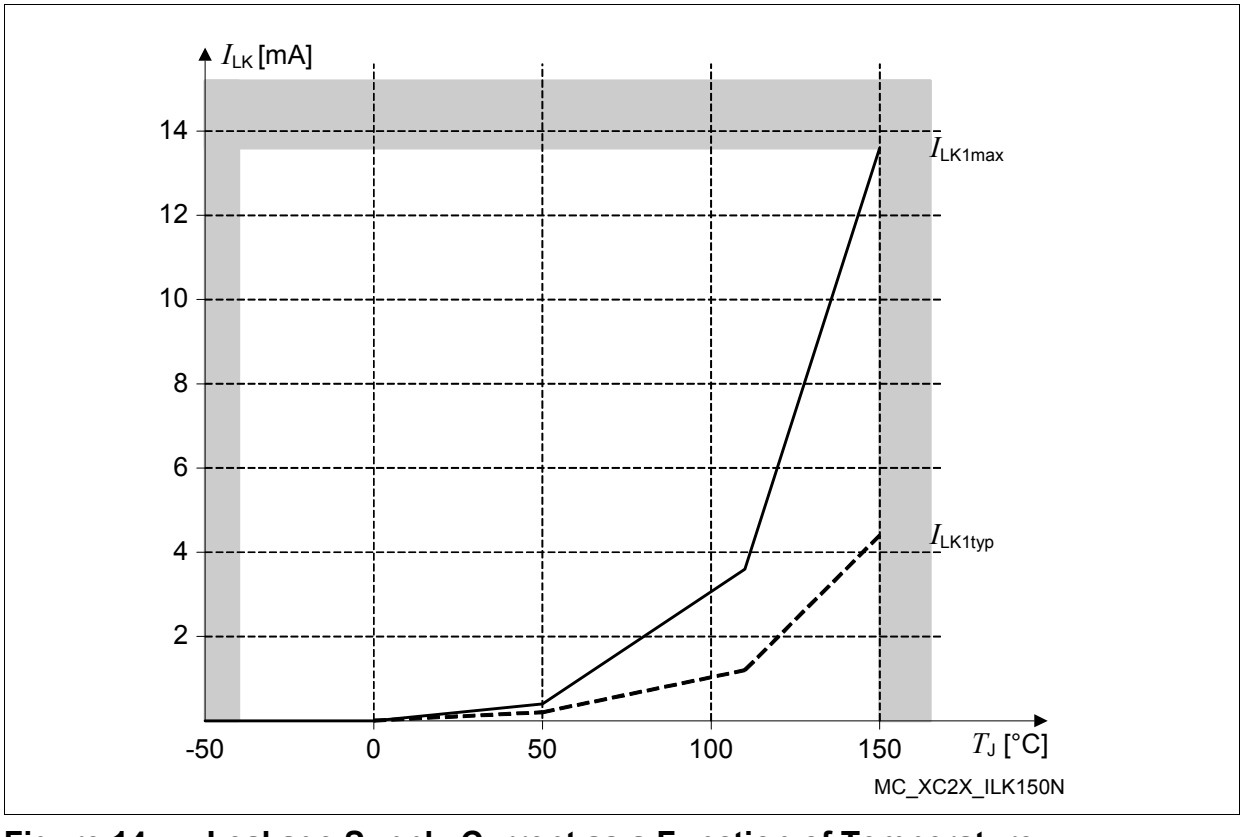

Figure 14 Leakage Supply Current as a Function of Temperature

4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Table 18 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	V_{AGND} + 1.0	V_{DDPA} + 0.05	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{AREF} - 1.0	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Analog clock frequency	f_{ADCI}		0.5	20	MHz	3)
Conversion time for 10-bit result[4)]	t_{C10}	CC	(13 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Conversion time for 8-bit result[4)]	t_{C8}	CC	(11 + STC) × t_{ADCI} + 2 × t_{SYS}		–	–
Wakeup time from analog powerdown, fast mode	t_{WAF}	CC	–	1	µs	–
Wakeup time from analog powerdown, slow mode	t_{WAS}	CC	–	10	µs	–
Total unadjusted error[5)]	TUE	CC	–	±2	LSB	V_{AREF} = 5.0 V[1)]
DNL error	EA_{DNL}	CC	–	±1	LSB	
INL error	EA_{INL}	CC	–	±1.2	LSB	
Gain error	EA_{GAIN}	CC	–	±0.8	LSB	
Offset error	EA_{OFF}	CC	–	±0.8	LSB	
Total capacitance of an analog input	C_{AINT}	CC	–	10	pF	6)7)
Switched capacitance of an analog input	C_{AINS}	CC	–	4	pF	6)7)
Resistance of the analog input path	R_{AIN}	CC	–	1.5	kΩ	6)7)
Total capacitance of the reference input	C_{AREFT}	CC	–	15	pF	6)7)

Table 18 A/D Converter Characteristics (cont'd)
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Switched capacitance of the reference input	C_{AREFS} CC	–	7	pF	6)7)
Resistance of the reference input path	R_{AREF} CC	–	2	kΩ	6)7)

1) TUE is tested at $V_{AREFx} = V_{DDPA}$, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.

4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and are found in **Table 19**.

5) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.

6) Not subject to production test - verified by design/characterization.

7) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

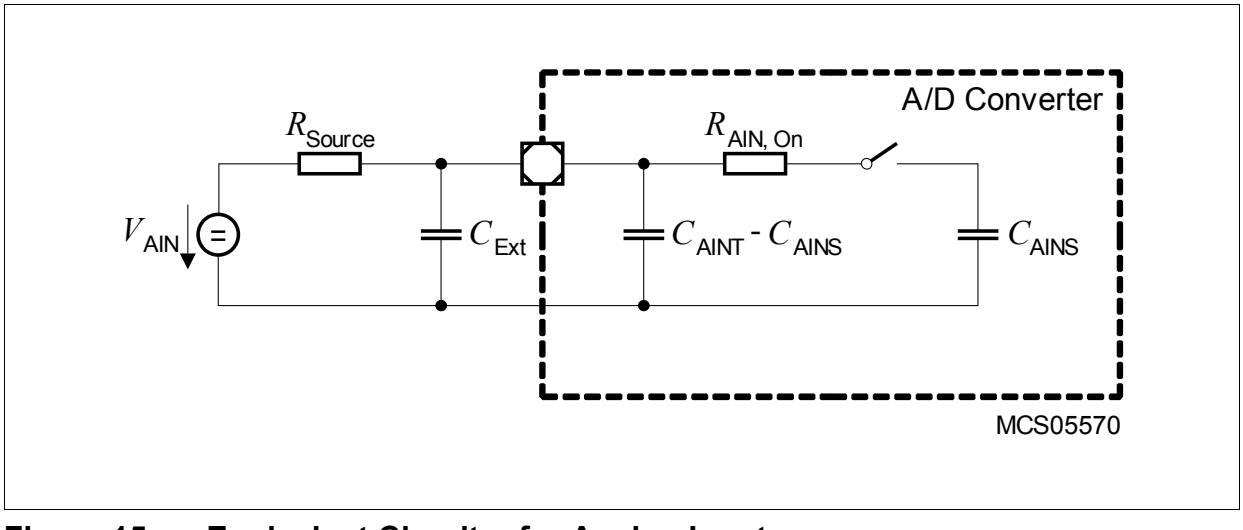

Figure 15 Equivalent Circuitry for Analog Inputs

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC2766X. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. In connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Table 26 External Clock Input Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDI}	–	1.7	V	1)
Input voltage (amplitude) on XTAL1	V_{AX1} SR	0.3 × V_{DDI}	–	–	V	Peak-to-peak voltage2)
XTAL1 input current	I_{IL} CC	–	–	±20	µA	0 V < V_{IN} < V_{DDI}
Oscillator frequency	f_{OSC} CC	4	–	40	MHz	Clock signal
		4	–	16	MHz	Crystal or Resonator
High time	t_1 SR	6	–	–	ns	
Low time	t_2 SR	6	–	–	ns	
Rise time	t_3 SR	–	8	8	ns	
Fall time	t_4 SR	–	8	8	ns	

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

Table 29 External Bus Cycle Timing for Upper Voltage Range (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: RD, WR(L/H)	t_{10} CC	–		13	ns	
Output valid delay for: BHE, ALE	t_{11} CC	–		13	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	t_{12} CC	–		14	ns	
Output valid delay for: A15 … A0 (on P2/P10)	t_{13} CC	–		14	ns	
Output valid delay for: CS	t_{14} CC	–		13	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	t_{15} CC	–		14	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	t_{16} CC	–		14	ns	
Output hold time for: RD, WR(L/H)	t_{20} CC	0		8	ns	
Output hold time for: BHE, ALE	t_{21} CC	0		8	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	t_{23} CC	0		8	ns	
Output hold time for: CS	t_{24} CC	0		8	ns	
Output hold time for: D15 … D0 (write data)	t_{25} CC	0		8	ns	
Input setup time for: READY, D15 … D0 (read data)	t_{30} SR	18		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1)]	t_{31} SR	-4		–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

4.6.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 31 SSC Master/Slave Mode Timing for Upper Voltage Range (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode Timing						
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	0	–	1)	ns	2)
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0.5 × t_{BIT}	–	3)	ns	
Transmit data output valid time	t_3 CC	-6	–	13	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-7	–	–	ns	
Slave Mode Timing						
Select input DX2 setup to first clock input DX1 transmit edge	t_{10} SR	7	–	–	ns	4)
Select input DX2 hold after last clock input DX1 receive edge	t_{11} SR	5	–	–	ns	4)
Data input DX0 setup time to clock input DX1 receive edge	t_{12} SR	7	–	–	ns	4)
Data input DX0 hold time from clock input DX1 receive edge	t_{13} SR	5	–	–	ns	4)
Data output DOUT valid time	t_{14} CC	8	–	29	ns	4)

1) The maximum value further depends on the settings for the slave select output leading delay.

2) $t_{SYS} = 1/f_{SYS}$ (= 12.5 ns @ 80 MHz)

3) The maximum value depends on the settings for the slave select output trailing delay and for the shift clock output delay.

4) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

5 Package and Reliability

In addition to the electrical parameters, the following specifcations ensure proper integration of the XC2766X into the target system.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 34 Package Parameters (PG-LQFP-100-3)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	6.2 × 6.2	mm	–
Power Dissipation	P_{DISS}	–	1.0	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	49	K/W	No thermal via[1)]
			37	K/W	4-layer, no pad[2)]
			22	K/W	4-layer, pad[3)]

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) or a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.