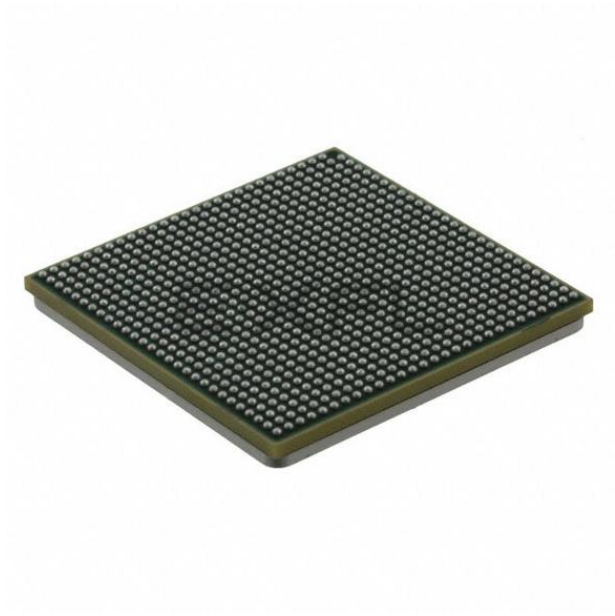

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144esvt1000b

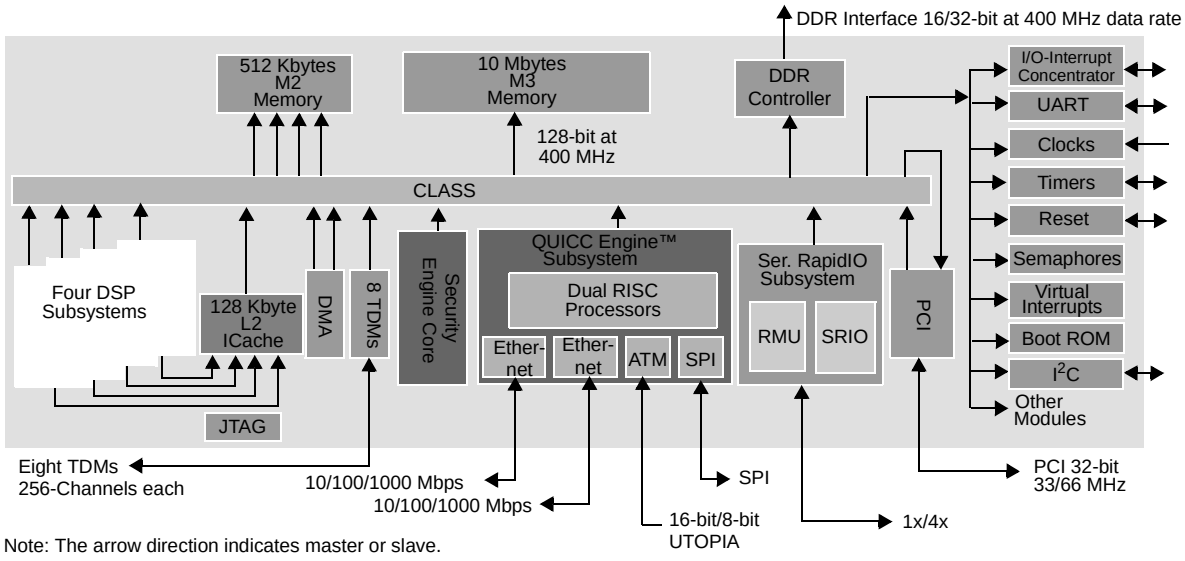


Figure 1. MSC8144E Block Diagram

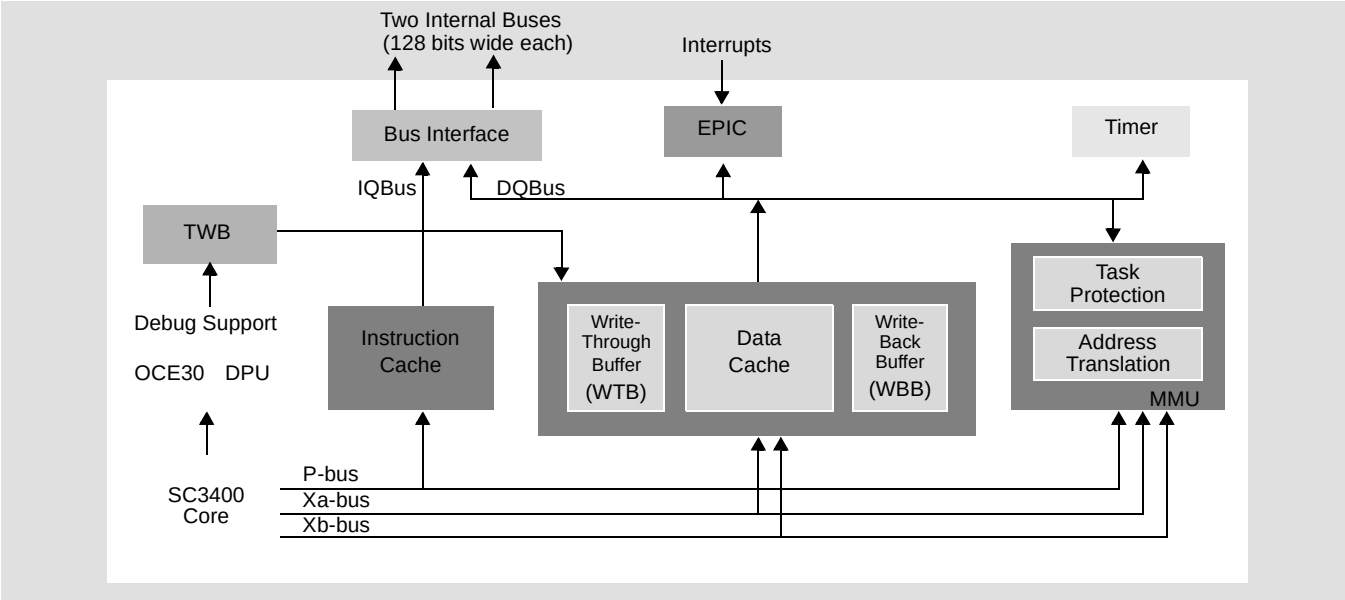


Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/ GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/ GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AB19	V_{DDM3}										V_{DDM3}
AB20	GND										GND
AB21	GND										GND
AB22	V_{DDDDR}										V_{DDDDR}
AB23	MECC7										V_{DDDDR}
AB24	MECC1										V_{DDDDR}
AB25	MECC4										V_{DDDDR}
AB26	MECC5										V_{DDDDR}
AB27	MECC2										V_{DDDDR}
AB28	ECC_MDQS										V_{DDDDR}
AC1	Reserved[1]										—
AC2	UTP_RD9/RC13	RC13	UTOPIA								V_{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA								V_{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM			PCI		TDM			V_{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/ $\overline{IRQ12}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AC6	V_{DDIO}										V_{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM								V_{DDIO}
AC8	PCI_AD23/GPIO7/$\overline{IRQ13}$/ TDM6TDAT[3, 6]/UTP_RMOD		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ		UTOPIA	V_{DDIO}
AC9	TDM7TSYN/ PCI_AD4		TDM		PCI			reserved			V_{DDIO}
AC10	V_{DDM3IO}										V_{DDM3IO}
AC11	GND										GND
AC12	V_{DDM3}										V_{DDM3}
AC13	GND										GND
AC14	V_{DDM3}										V_{DDM3}
AC15	GND										GND
AC16	V_{DDM3}										V_{DDM3}
AC17	GND										GND
AC18	V_{DDM3}										V_{DDM3}
AC19	GND										GND
AC20	V_{DDM3IO}										V_{DDM3IO}
AC21	Reserved[1]										—
AC22	MECC6										V_{DDDDR}
AC23	MECC3										V_{DDDDR}
AC24	ECC_MDM										V_{DDDDR}
AC25	V_{DDDDR}										V_{DDDDR}
AC26	MECC0										V_{DDDDR}
AC27	V_{DDDDR}										V_{DDDDR}
AC28	$\overline{ECC\_MDQS}$										V_{DDDDR}
AD1	Reserved[1]										—
AD2	GPIO1[3, 6]		GPIO								V_{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO								V_{DDIO}

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	–0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	–0.3 to V_{DDM3IO} + 0.3	V
Rapid I/O C voltage	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O P voltage	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	–0.3 to 1.21	V
Operating temperature	T_J	–40 to 105	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144E (see Figure 43)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DD}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
PLL supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
M3 memory Internal voltage	V_{DDM3}	1.213	1.25	1.313	V
DDR memory supply voltage • DDR mode • DDR2 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 2.375 1.71 0.49 × V_{DDDDR} (nom)	 2.5 1.8 0.5 × V_{DDDDR} (nom)	 2.625 1.89 0.51 × V_{DDDDR} (nom)	 V V V
Ethernet 1 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE1}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
Ethernet 2 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE2}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.97	1.0	1.05	V
Rapid I/O P voltage • Short run (haul) mode • Long run (haul) mode	V_{DDSXP}	 0.97 1.14	 1.0 1.2	 1.05 1.26	 V V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.97	1.0	1.05	V
Operating temperature range: • Standard (VT) • Intermediate (SVT) • Extended (TVT)	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C °C

Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144E (see Figure 43).

2.5.2.2 Spread Spectrum Clock

SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$ is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.5.3 PCI DC Electrical Characteristics

Table 9. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	$0.5 \times V_{DDPCI}$	3.465	V
Input low voltage	V_{IL}	–0.5	$0.3 \times V_{DDPCI}$	V
Input Pull-up voltage[2]	V_{IPU}	$0.7 \times V_{DDPCI}$		
Input leakage current, $0<V_{IN}<V_{DDPCI}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, $0<V_{IN}<V_{DDPCI}$	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –0.5 mA, except open drain pins	V_{OH}	$0.9 \times V_{DDPCI}$	—	V
Output low voltage, I_{OL}= 1.5 mA	V_{OL}	—	$0.1 \times V_{DDPCI}$	V
Input Pin Capacitance[2]	C_{IN}		10	pF

Notes: **1.** Not tested. Guaranteed by design.

2.5.4 TDM DC Electrical Characteristics

Table 10. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current $0<V_{IN}<V_{DDTDM}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current	I_{OZ}	–30	30	µA
Output high voltage, I_{OH} = –1.6 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 0.4mA	V_{OL}	—	0.4	V

2.5.5 Ethernet DC Electrical Characteristics

2.5.5.1 MII, SMII and RMII DC Electrical Characteristics

Table 11. MII, SMII and RMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDGE1} V_{DDGE2}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4mA	V_{OL}	—	0.4	V
Input Pin Capacitance[1]	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

2.5.5.2 RGMII DC Electrical Characteristics

Table 12. RGMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 2.5 V	V_{DDGE1} V_{DDGE2}	2.375	2.625	V
Input high voltage	V_{IH}	1.7	2.625	V
Input low voltage	V_{IL}	–0.3	0.7	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Output high voltage, I_{OH} = –1 mA	V_{OH}	2.0	2.625	V
Output low voltage, I_{OL}= 1 mA	V_{OL}	—	0.4	V
Input Pin Capacitance[1]	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

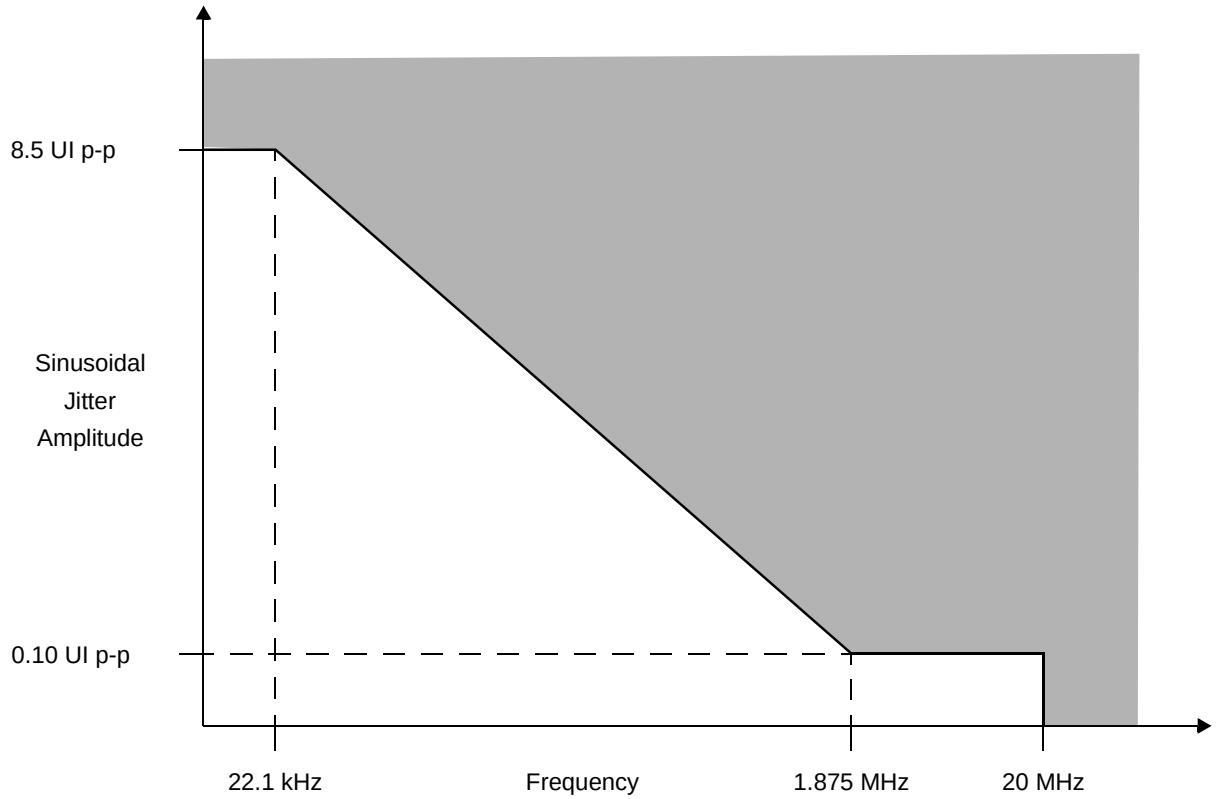


Figure 13. Single Frequency Sinusoidal Jitter Limits

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 14 and Table 35. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. Table 36 provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

Table 36. PCI AC Timing Specifications (continued)

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	

Notes:
1. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
2. All PCI signals are measured from $0.5 \times V_{DDIO}$ of the rising edge of PCI_CLK_IN to $0.4 \times V_{DDIO}$ of the signal in question for 3.3-V PCI signaling levels.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is in Table 19 and Figure 7

Figure 15 provides the AC test load for the PCI.

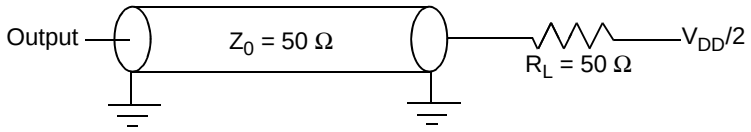


Figure 15. PCI AC Test Load

Figure 16 shows the PCI input AC timing conditions.

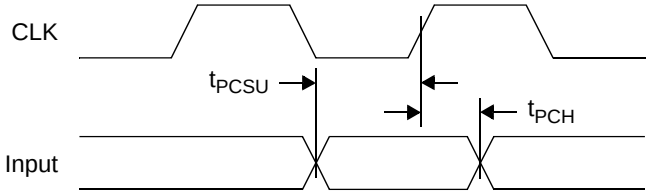


Figure 16. PCI Input AC Timing Measurement Conditions

Figure 17 shows the PCI output AC timing conditions.

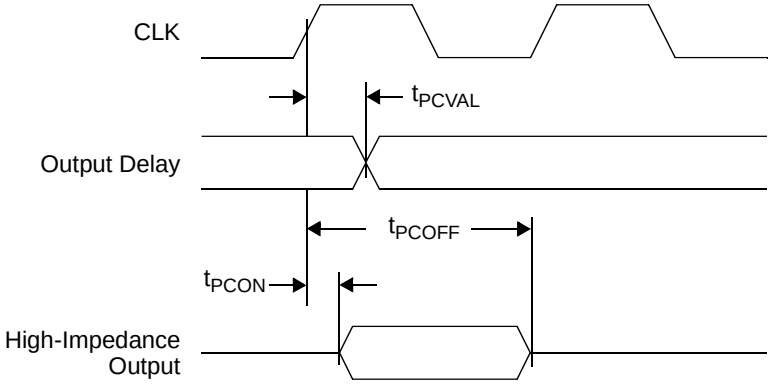


Figure 17. PCI Output AC Timing Measurement Condition

2.6.7 TDM Timing

Table 37. TDM Timing

Characteristic	Symbol	Expression	Min	Max	Units
TDMxRCLK/TDMxTCLK	t_{TDMC}	TC[1]	16	—	ns
TDMxRCLK/TDMxTCLK high pulse width	t_{TDMCH}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDMxRCLK/TDMxTCLK low pulse width	t_{TDMCL}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDM receive all input setup time related to TDMxRCLK TDMxTSYN input setup time related to TDMxTCLK in TSO=0 mode	t_{TDMVKH}		3.6	—	ns
TDM receive all input hold time related to TDMxRCLK TDMxTSYN input hold time related to TDMxTCLK in TSO=0 mode	t_{TDMXKH}		1.9	—	ns
TDMxTCLK high to TDMxTDAT output active[2]	$t_{TDMDHOX}$		2.5	—	ns
TDMxTCLK high to TDMxTDAT output valid[2]	$t_{TDMDHOV}$		—	9.8	ns
All output hold time (except TDMxTSYN) [3]	t_{TDMHOX}		2.5	—	ns
TDMxTCLK high to TDMxTDAT output high impedance[2]	$t_{TDMDHOZ}$		—	9.8	ns
TDMxTCLK high to TDMxTSYN output valid[2]	$t_{TDMSHOV}$		—	9.25	ns
TDMxTSYN output hold time[3]	$t_{TDMSHOX}$		2.0	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. Values are based on 10 pF capacitive load.
4. The expression is for common calculations only.

Figure 18 shows the TDM input AC timing.

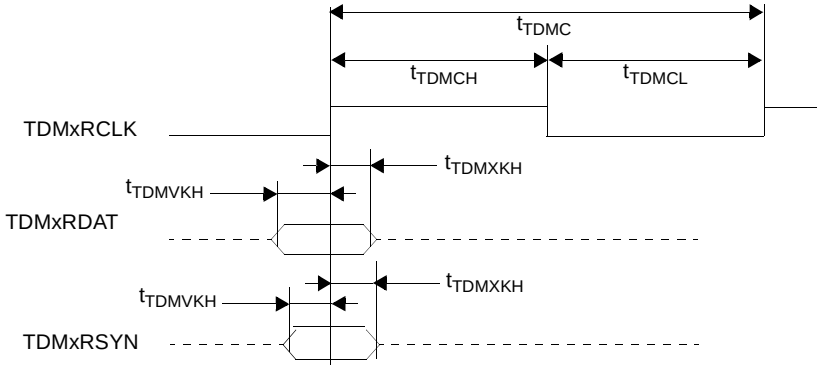


Figure 18. TDM Inputs Signals

Note: For some TDM modes, receive data and receive sync are input on other pins. This timing is also valid for them. See the *MSC8144E Reference Manual*.

Figure 19 shows TDMxTSYN AC timing in TSO=0 mode.

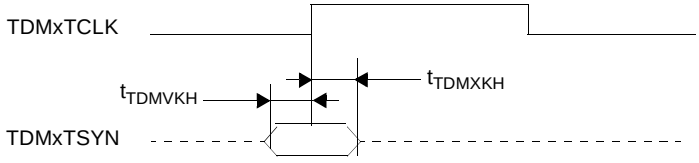


Figure 19. TDMxTSYN in TSO=0 mode

Figure 20 shows the TDM Output AC timing

Figure 28 shows the RMII transmit and receive AC timing diagram.

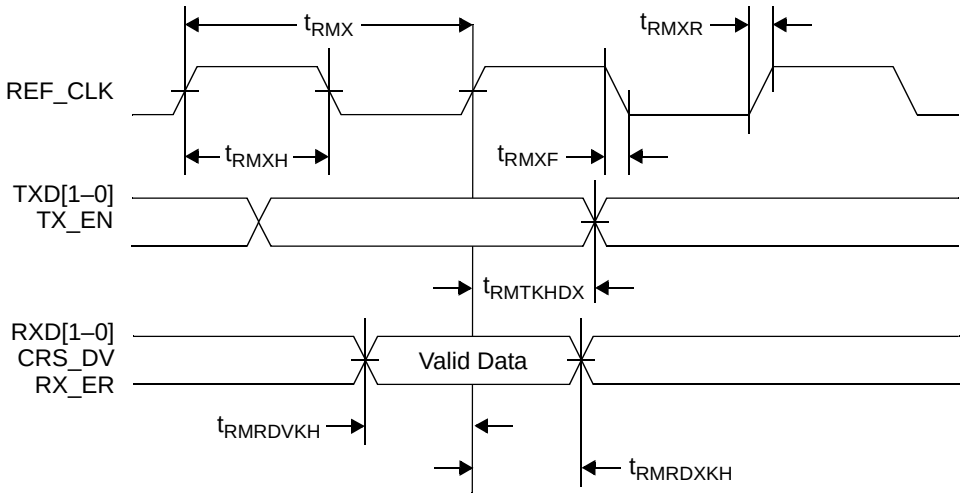


Figure 28. RMII Transmit and Receive AC Timing

Figure 29 provides the AC test load.

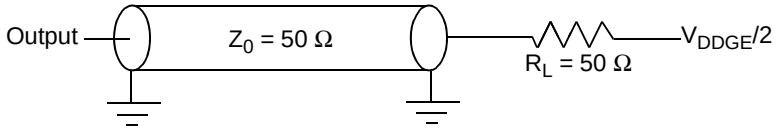


Figure 29. AC Test Load

2.6.10.5 SMII AC Timing Specification

Table 44. SMII Mode Signal Timing

Characteristics	Symbol	Min	Max	Unit
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.0	ns

Notes:
1. Typical REF_CLK clock period is 8ns
2. Measured using a 5 pF load.
3. Measured using a 15 pF load
4. Program GCR4 as 0x00002008

Figure 30 shows the SMII Mode signal timing.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

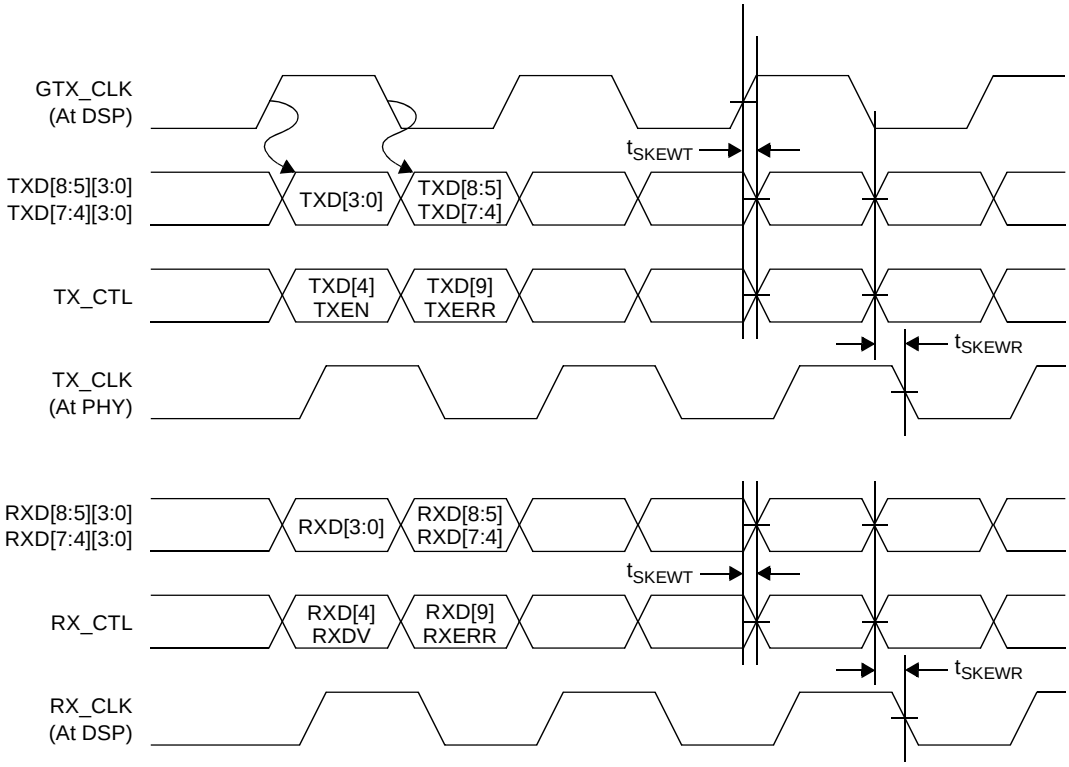


Figure 31. RGMII AC Timing and Multiplexing

2.6.12 SPI Timing

Table 48 lists the SPI input and output AC timing specifications.

Table 48. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 34 provides the AC test load for the SPI.

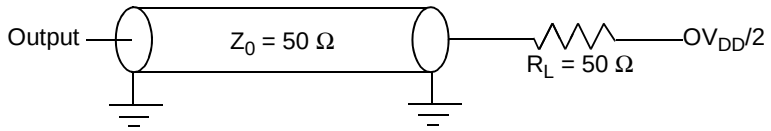
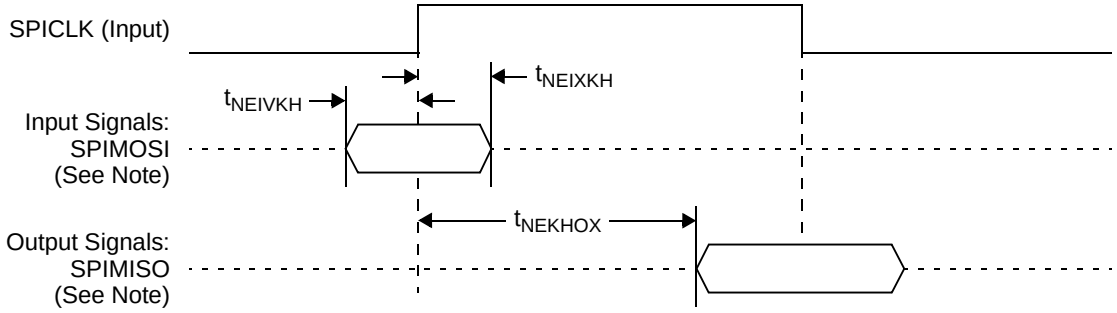


Figure 34. SPI AC Test Load

Figure 35 and Figure 36 represent the AC timings from Table 48. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 35 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Slave Mode (External Clock)

Figure 36 shows the SPI timings in master mode (internal clock).

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	15.0	—	ns
TCK rise and fall times	t_{TCKR}	—	3.0	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 38 Shows the Test Clock Input Timing Diagram

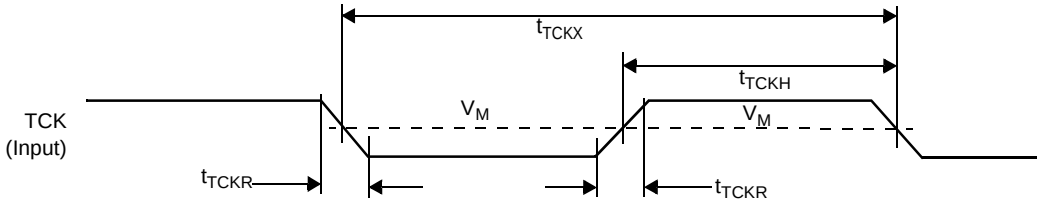


Figure 38. Test Clock Input Timing

Figure 39 Shows the boundary scan (JTAG) timing diagram.

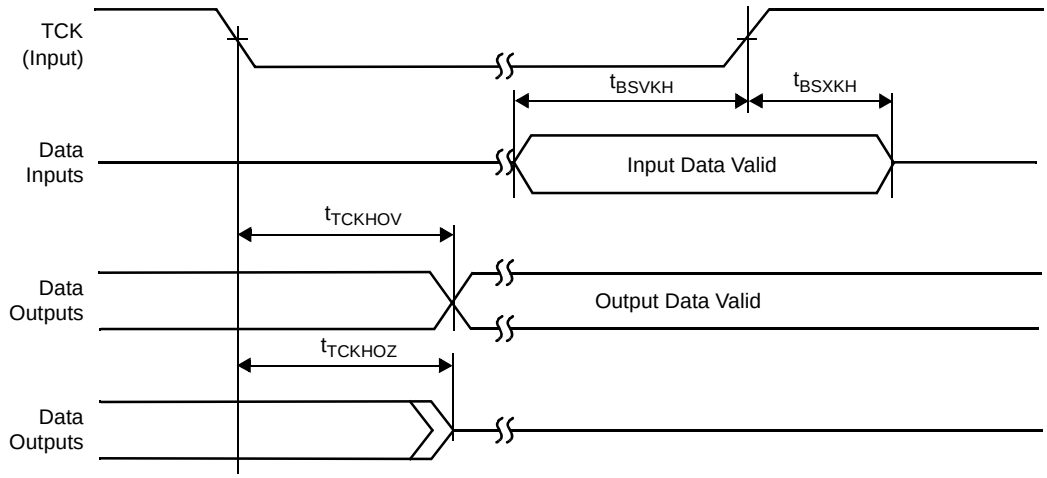


Figure 39. Boundary Scan (JTAG) Timing

Figure 40 Shows the test access port timing diagram

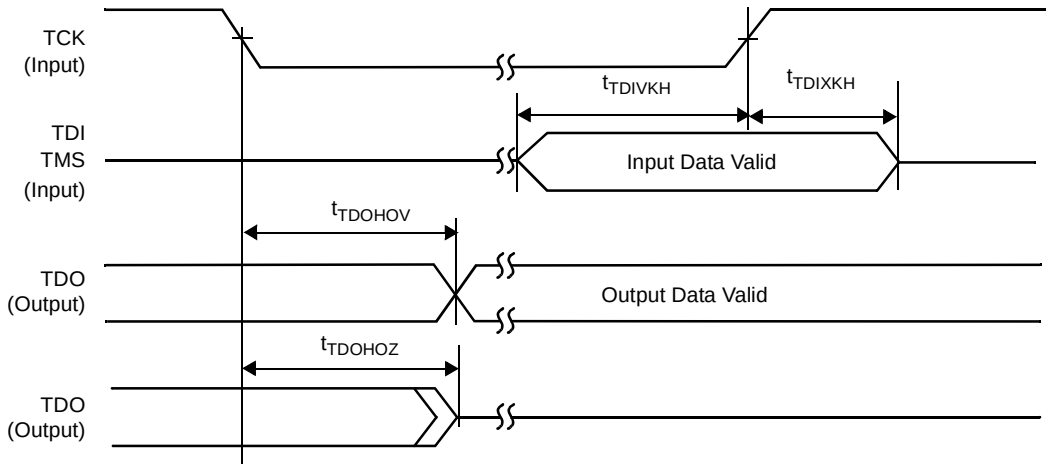


Figure 40. Test Access Port Timing

Figure 41 Shows the $\overline{\text{TRST}}$ timing diagram.

Figure 41. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8144E device is designed into a system.

3.1 Start-up Sequencing Recommendations

3.1.1 Power-on Sequence

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSXC}, V_{DDSXP}, $V_{DDRIOPLL}$ and other MSC8144E supplies.
- V_{DDPLL} should be coupled with the V_{DD} power rail with extremely low impedance path.

External voltage applied to any input line must not exceed the related to this port I/O supply by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8144E device in the system during start-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4V/ns.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

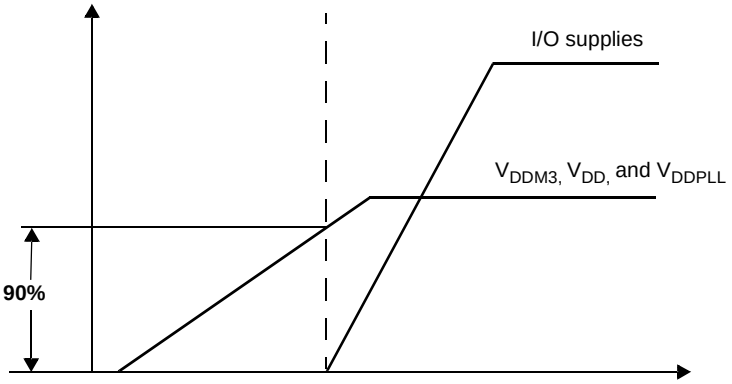


Figure 42. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

3.2 Power Supply Design Considerations

Each PLL supply must have an external RC filter for the V_{DDPLL} input. The filter is a 10 Ω resistor in series with two 2.2 µF, low ESL (<0.5 nH) and low ESR capacitors. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately (see Figure 43). For optimal noise filtering, place the circuit as close as possible to its V_{DDPLL} inputs. These traces should be short and direct.

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

3.4.2.2 Serial RapidIO Specific Lane Is Not Used

Table 55. Connectivity of Serial RapidIO Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	in use
SRIO_IMP_CAL_TX	in use
$\overline{\text{SRIO\_REF\_CLK}}$	in use
SRIO_REF_CLK	in use
SRIO_RXD***x***	GND_{SXC}
$\overline{\text{SRIO\_RXD}\boldsymbol{x}}$	GND_{SXC}
$\overline{\text{SRIO\_TXD}\boldsymbol{x}}$	NC
SRIO_TXD***x***	NC
$V_{DDRIOPLL}$	in use
GND_{RIOPLL}	in use
GND_{SXP}	GND_{SXP}
GND_{SXC}	GND_{SXC}
V_{DDSXP}	1.0 V
V_{DDSXC}	1.0 V
Note: The ***x*** indicates the lane number {0,1,2,3} for all unused lanes.	

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Revision	Date	Description
0	June. 2007	• Initial public release.
1	Sep 2007	• Updated M3 voltage range in Table 3. • Changed note in Table 7 for PLL power supplies. • DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, **Section 2.7.4.1**, **Section 2.7.4.2**, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. • Deleted text before Table 13 and added note 2 to input pin capacitance. • Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. • Deleted **Section 2.6.5** on page 32 and renumbered subsequent subsections. • Deleted text before new **Section 2.6.5.1**. • Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. • Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. • Changed output high and low voltage levels in Table 17 and Table 18. • Deleted text before Table 19. • Added clock skew ranges in percent in Table 21. • Changed V_{REF} to MV_{REF} in Table 26. • Changed V_{DD} to V_{DDIO} in Table 36 Updated note 2. • Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. • Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. • Changed the value of the data to clock out skew in Table 51. • Changed EE pin timing in Table 55. • Changed the head for the JTAG timing section, now **Section 2.7.14**. • Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 55. • Added new **Section 3.3** with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
2	Sep 2007	• Changed leakage current values in Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, and Table 19 from –10 and 10 µa to –30 and 30 µa. • Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. • Updated note 1 in Table 45.
3	Oct 2007	• Corrected column numbering in Figure 3 and Figure 4. • Updated SPI signal names in Table 1.
4	Oct 2007	• Updated SPI signal names in Table 1.
5	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
6	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
7	Mar 2008	• Changed description of Table 16 in **Section 2.7.2**.
8	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are “not” required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.