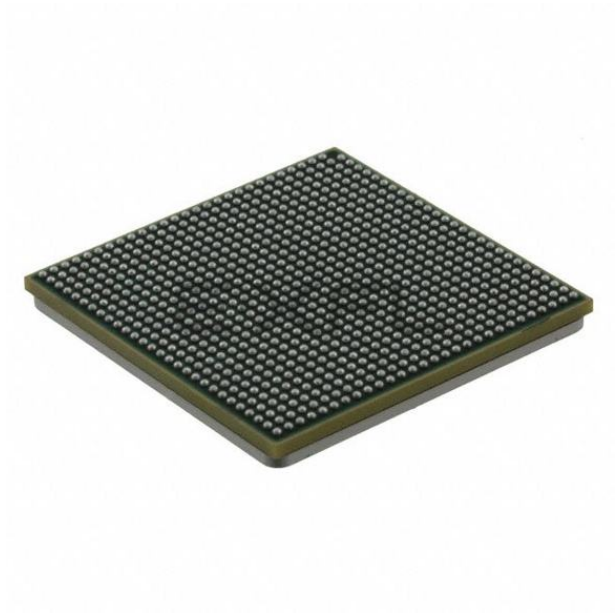

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144esvt800b

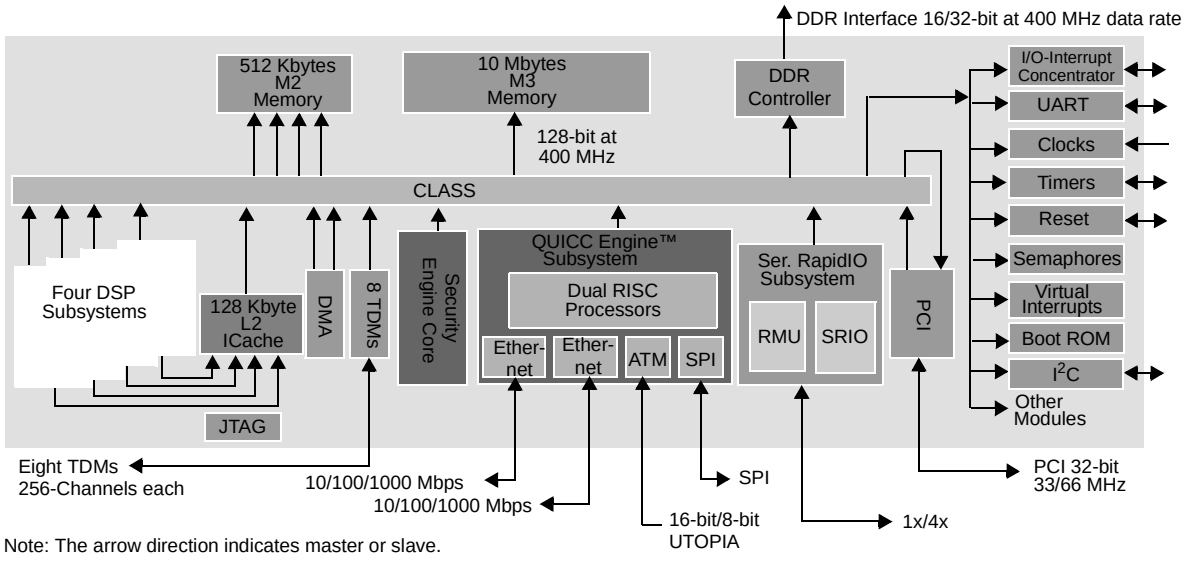


Figure 1. MSC8144E Block Diagram

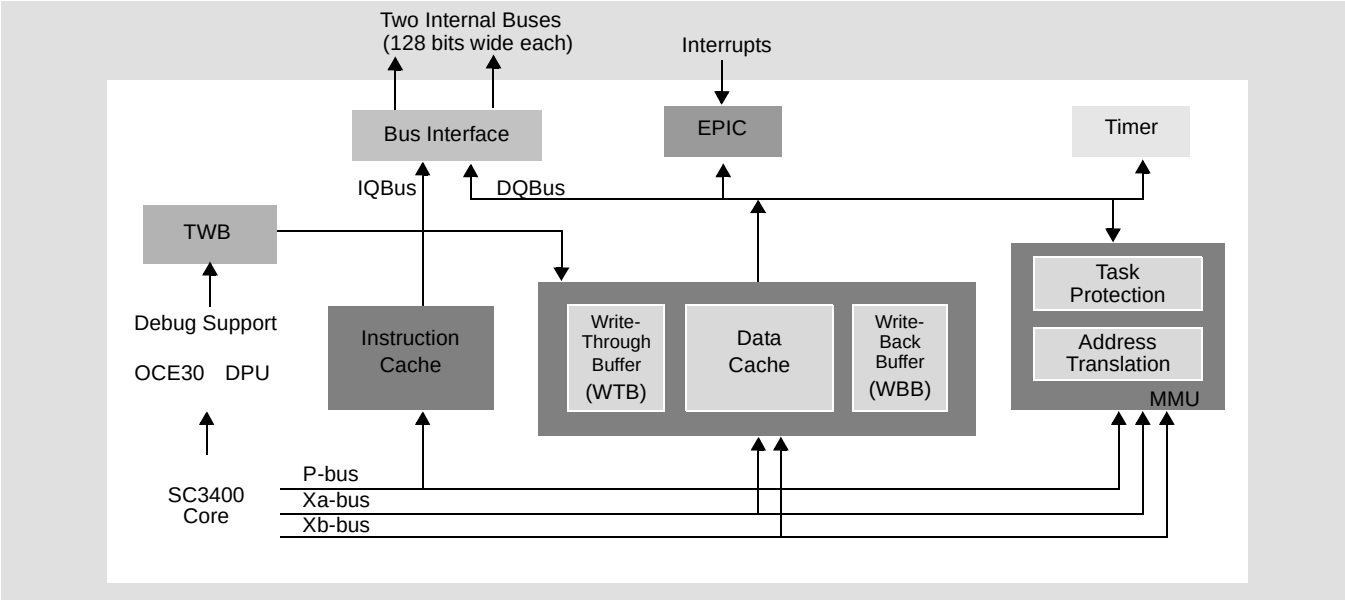


Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	GE1_RD0/UTP_RD2/ PCI_CBE2		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	MDQS2										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/ GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/ GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V_{DDIO}										V_{DDIO}
M9	V_{DD}										V_{DD}
M10	GND										GND
M11	V_{DD}										V_{DD}
M12	GND										GND
M13	V_{DD}										V_{DD}
M14	GND										GND
M15	V_{DD}										V_{DD}
M16	GND										GND
M17	V_{DD}										V_{DD}
M18	GND										GND
M19	V_{DD}										V_{DD}
M20	GND										GND
M21	V_{DD}										V_{DD}
M22	V_{DDDDR}										V_{DDDDR}
M23	$\overline{MCS1}$										V_{DDDDR}
M24	MA13										V_{DDDDR}
M25	MA2										V_{DDDDR}
M26	MA0										V_{DDDDR}
M27	GND										GND
M28	MCK1										V_{DDDDR}
N1	Reserved[1]										—
N2	V_{DDIO}										V_{DDIO}
N3	TMS										V_{DDIO}
N4	UTP_RD10/PCI_AD14[5]		UTOPIA		PCI	UTOPIA					V_{DDIO}
N5	V_{DDIO}		Power								V_{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V_{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V_{DDIO}
N8	TMR3/$\overline{PCI\_IRDY}$/GPIO19[3,6]/ UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
N9	GND										GND
N10	V_{DDM3}										V_{DDM3}
N11	V_{DD}										V_{DD}
N12	V_{DDM3}										V_{DDM3}
N13	V_{DD}										V_{DD}
N14	V_{DDM3}										V_{DDM3}
N15	V_{DD}										V_{DD}
N16	V_{DDM3}										V_{DDM3}
N17	V_{DD}										V_{DD}
N18	V_{DDM3}										V_{DDM3}
N19	V_{DD}										V_{DD}
N20	V_{DDM3}										V_{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144E Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144E Reference Manual* for configuration details.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8144E Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8144E.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{dd}	–0.3 to 1.1	V
PLL supply voltage[3]	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1	V
M3 memory Internal voltage	V_{DDM3}	–0.3 to 1.32	V
DDR memory supply voltage • DDR mode • DDR2 mode	V_{DDDDR}	 –0.3 to 2.75 –0.3 to 1.98	 V V
DDR reference voltage	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage	V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
Ethernet 1 I/O voltage	V_{DDGE1}	–0.3 to 3.465	V
Input Ethernet 1 I/O voltage	V_{INGE1}	–0.3 to V_{DDGE1} + 0.3	V
Ethernet 2 I/O voltage	V_{DDGE2}	–0.3 to 3.465	V
Input Ethernet 2I/O voltage	V_{INGE2}	–0.3 to V_{DDGE2} + 0.3	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	–0.3 to 3.465	V
Input I/O voltage	V_{INIO}	–0.3 to V_{DDIO} + 0.3	V

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144E for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144E

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4 mA	V_{OL}	—	0.5	V

Notes: **1.** Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}		30	µA
Output high voltage, I_{OH} = –4.0 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 4.0 mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, JTAG Ports DC Electrical Characteristics

Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, and JTAG Port[1] DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–30	30	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes: **1.** This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

Table 19. Timing for a Reset Configuration Write (continued)

No.	Characteristics	Expression	Max	Min	Unit
2	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for external pins and hard coded RCW				
	• 33 MHz <= CLKIN < 66 MHz	15369/CLKIN	615	233	µs
	• 66 MHz <= CLKIN <= 133 MHz	34825/CLKIN	528	262	µs
	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for loading RCW the I^2C interface				
	• 33 MHz <= CLKIN < 44 MHz	92545/CLKIN	3702	2103	µs
	• 44 MHz <= CLKIN < 66 MHz	107435/CLKIN	2441	1627	µs
	• 66 MHz <= CLKIN < 100 MHz	124208/CLKIN	1882	1242	µs
	• 100 MHz <= CLKIN < 133 MHz	157880/CLKIN	1579	1187	µs
3	Delay from $\overline{\text{HRESET}}$ deassertion to $\overline{\text{SRESET}}$ deassertion				
	• REFCLK = 33 MHz to 133 MHz	16/CLKIN	640	120	ns
Note:	Timings are not tested, but are guaranteed by design.				

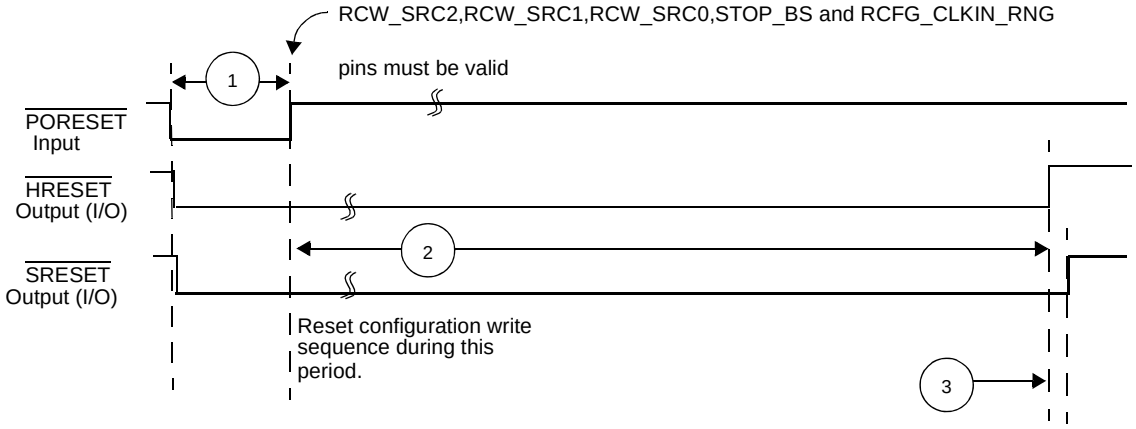


Figure 7. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

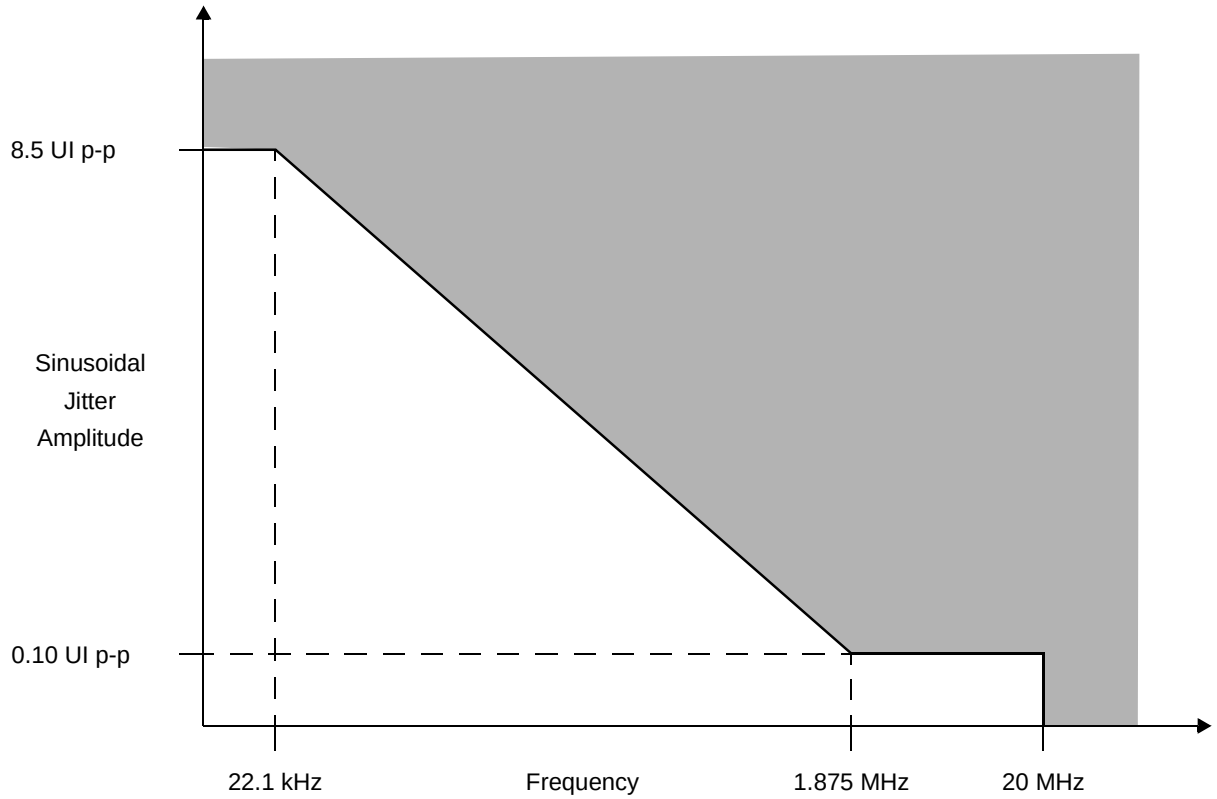


Figure 13. Single Frequency Sinusoidal Jitter Limits

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 14 and Table 35. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. Table 36 provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

2.6.7 TDM Timing

Table 37. TDM Timing

Characteristic	Symbol	Expression	Min	Max	Units
TDMxRCLK/TDMxTCLK	t_{TDMC}	TC[1]	16	—	ns
TDMxRCLK/TDMxTCLK high pulse width	t_{TDMCH}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDMxRCLK/TDMxTCLK low pulse width	t_{TDMCL}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDM receive all input setup time related to TDMxRCLK TDMxTSYN input setup time related to TDMxTCLK in TSO=0 mode	t_{TDMVKH}		3.6	—	ns
TDM receive all input hold time related to TDMxRCLK TDMxTSYN input hold time related to TDMxTCLK in TSO=0 mode	t_{TDMXKH}		1.9	—	ns
TDMxTCLK high to TDMxTDAT output active[2]	$t_{TDMDHOX}$		2.5	—	ns
TDMxTCLK high to TDMxTDAT output valid[2]	$t_{TDMDHOV}$		—	9.8	ns
All output hold time (except TDMxTSYN) [3]	t_{TDMHOX}		2.5	—	ns
TDMxTCLK high to TDMxTDAT output high impedance[2]	$t_{TDMDHOZ}$		—	9.8	ns
TDMxTCLK high to TDMxTSYN output valid[2]	$t_{TDMSHOV}$		—	9.25	ns
TDMxTSYN output hold time[3]	$t_{TDMSHOX}$		2.0	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. Values are based on 10 pF capacitive load.
4. The expression is for common calculations only.

Figure 18 shows the TDM input AC timing.

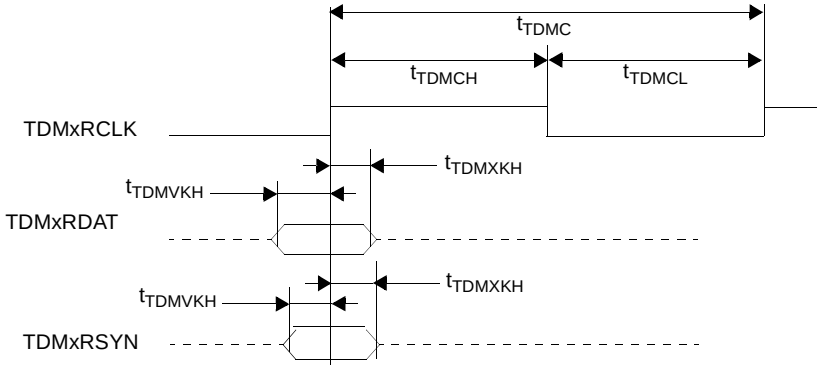


Figure 18. TDM Inputs Signals

Note: For some TDM modes, receive data and receive sync are input on other pins. This timing is also valid for them. See the *MSC8144E Reference Manual*.

Figure 19 shows TDMxTSYN AC timing in TSO=0 mode.

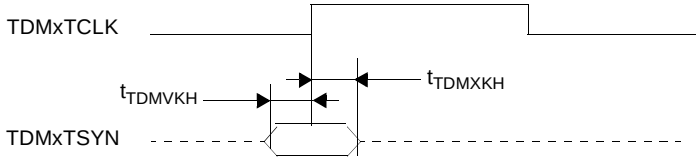


Figure 19. TDMxTSYN in TSO=0 mode

Figure 20 shows the TDM Output AC timing

Figure 26 provides the AC test load.

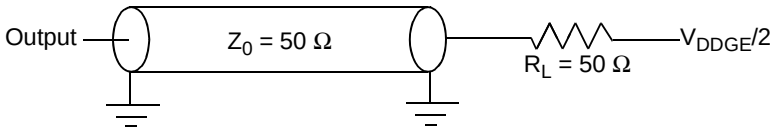


Figure 26. AC Test Load

Figure 27 shows the MII receive AC timing diagram.

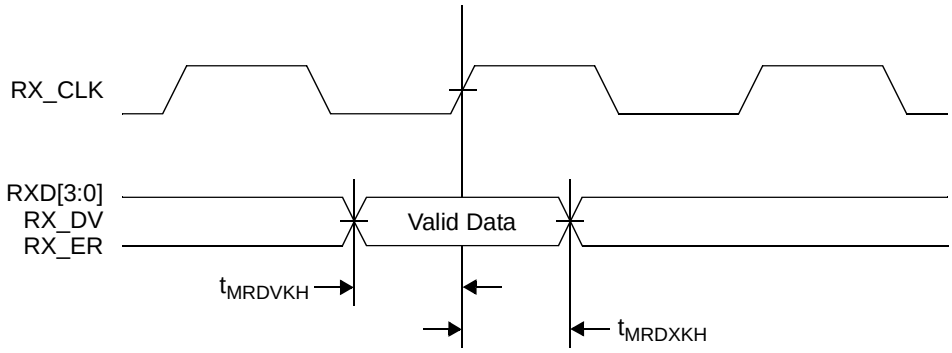


Figure 27. MII Receive AC Timing

2.6.10.4 RMII Transmit and Receive AC Timing Specifications

Table 43 provides the RMII transmit and receive AC timing specifications.

Table 43. RMII Transmit and Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	65	%
REF_CLK to RMII data TXD[1–0], TX_EN delay	$t_{RMTKHDX}$	2	10	ns
RXD[1–0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	ns
RXD[1–0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	ns
REF_CLK data clock rise	t_{RMXR}	1.0	4.0	ns
REF_CLK data clock fall	t_{RMXF}	1.0	4.0	ns
Typical REF_CLK clock period (t_{RMX}) is 20 ns				
Notes: **1.** Typical REF_CLK clock period (t_{RMX}) is 20 ns **2.** Program GCR4 as 0x00001405				

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

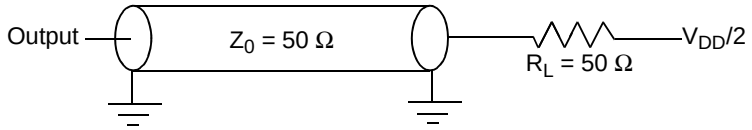


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

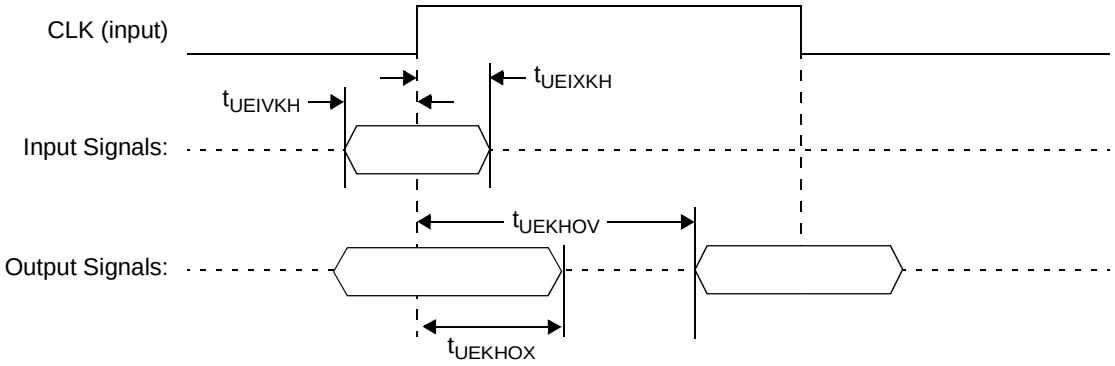


Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

2.6.12 SPI Timing

Table 48 lists the SPI input and output AC timing specifications.

Table 48. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 34 provides the AC test load for the SPI.

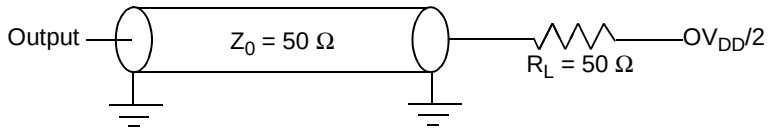
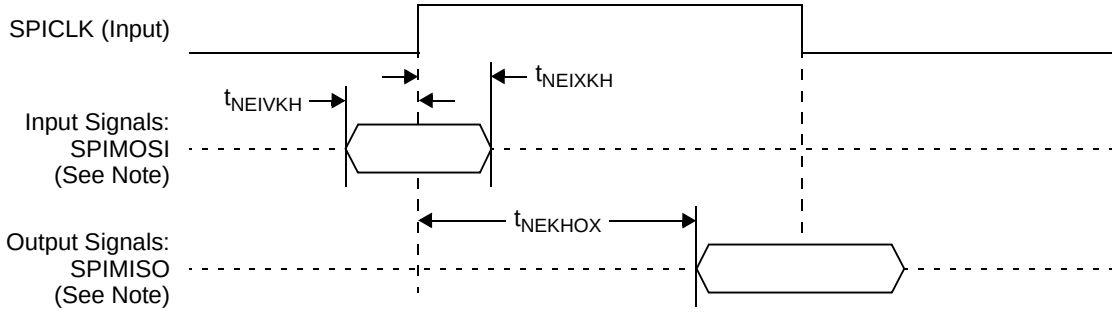


Figure 34. SPI AC Test Load

Figure 35 and Figure 36 represent the AC timings from Table 48. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 35 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Slave Mode (External Clock)

Figure 36 shows the SPI timings in master mode (internal clock).

3.4.7 PCI Related Pins

Table 64 lists the board connections of the pins when PCI is not used. Table 64 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 64. Connectivity of PCI Related Pins When PCI Is Not Used

Signal Name	Pin Connection
PCI_AD[0–31]	GND
$\overline{\text{PCI\_CBE[0–3]}}$	GND
PCI_CLK_IN	GND
$\overline{\text{PCI\_DEVSEL}}$	V_{DDIO}
$\overline{\text{PCI\_FRAME}}$	V_{DDIO}
$\overline{\text{PCI\_GNT}}$	V_{DDIO}
PCI_IDS	GND
$\overline{\text{PCI\_IRDY}}$	V_{DDIO}
PCI_PAR	GND
$\overline{\text{PCI\_PERR}}$	V_{DDIO}
$\overline{\text{PCI\_REQ}}$	NC
$\overline{\text{PCI\_SERR}}$	V_{DDIO}
$\overline{\text{PCI\_STOP}}$	V_{DDIO}
$\overline{\text{PCI\_TRDY}}$	V_{DDIO}
V_{DDIO}	3.3 V

3.4.8 Miscellaneous Pins

Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ[0–15]}}$	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND

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