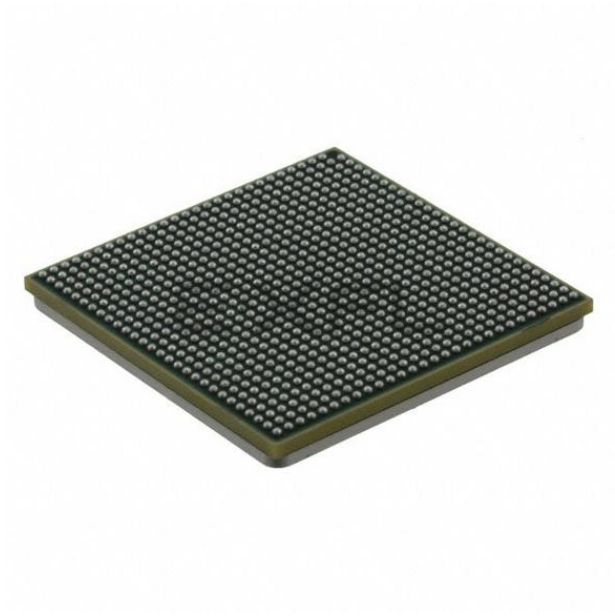

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144evt1000b

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1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
N22	GND										GND
N23	MODT1										V_{DDDDR}
N24	MCKE0										V_{DDDDR}
N25	V_{DDDDR}										V_{DDDDR}
N26	MA5										V_{DDDDR}
N27	MA6										V_{DDDDR}
N28	MA11										V_{DDDDR}
P1	Reserved[1]										—
P2	TDI[5]										V_{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA					V_{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA					V_{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA					V_{DDIO}
P7	$\overline{\text{PCI\_GNT}}$/GPIO29/$\overline{\text{IRQ7}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P8	$\overline{\text{PCI\_STOP}}$/GPIO30/$\overline{\text{IRQ2}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P9	GND										GND
P10	GND										GND
P11	V_{DDM3}										V_{DDM3}
P12	GND										GND
P13	V_{DDM3}										V_{DDM3}
P14	GND										GND
P15	V_{DDM3}										V_{DDM3}
P16	GND										GND
P17	V_{DDM3}										V_{DDM3}
P18	GND										GND
P19	V_{DDM3}										V_{DDM3}
P20	GND										GND
P21	GND										GND
P22	V_{DDDDR}										V_{DDDDR}
P23	$\overline{\text{MCS0}}$										V_{DDDDR}
P24	$\overline{\text{MRAS}}$										V_{DDDDR}
P25	GND										GND
P26	V_{DDDDR}										V_{DDDDR}
P27	GND										GND
P28	$\overline{\text{MCK2}}$										V_{DDDDR}
R1	Reserved[1]										—
R2	TCK										V_{DDIO}
R3	TDO										V_{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA					V_{DDIO}
R5	UTP_RCLAV_PDRPA/ PCI_AD12		UTOPIA		PCI	UTOPIA					V_{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI		TDM			V_{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI		TDM			V_{DDIO}
AA9	V_{DDIO}										V_{DDIO}
AA10	V_{DDM3}										V_{DDM3}
AA11	GND										GND
AA12	V_{DDM3}										V_{DDM3}
AA13	GND										GND
AA14	V_{DDM3}										V_{DDM3}
AA15	GND										GND
AA16	V_{DDM3}										V_{DDM3}
AA17	GND										GND
AA18	V_{DDM3}										V_{DDM3}
AA19	GND										GND
AA20	V_{DDM3}										V_{DDM3}
AA21	GND										GND
AA22	GND										GND
AA23	MDQ15										V_{DDDDR}
AA24	MDQ14										V_{DDDDR}
AA25	MDM1										V_{DDDDR}
AA26	MDQ12										V_{DDDDR}
AA27	$\overline{\text{MDQS1}}$										V_{DDDDR}
AA28	MDQS1										V_{DDDDR}
AB1	Reserved[1]										-
AB2	UTP_TSOC/RC15	RC15	UTOPIA								V_{DDIO}
AB3	V_{DDIO}										V_{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/$\overline{\text{IRQ11}}$[3, 6]		TDM/GPIO/ IRQ			PCI		TDM/GPIO/ IRQ			V_{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/ $\overline{\text{IRQ14}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/$\overline{\text{IRQ10}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI		TDM			V_{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI		TDM			V_{DDIO}
AB10	GND										GND
AB11	V_{DDM3}										V_{DDM3}
AB12	GND										GND
AB13	V_{DDM3}										V_{DDM3}
AB14	GND										GND
AB15	V_{DDM3}										V_{DDM3}
AB16	GND										GND
AB17	V_{DDM3}										V_{DDM3}
AB18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AD4	GPIO2[3, 6]		GPIO								V_{DDIO}
AD5	GND										GND
AD6	TDM1TCLK		TDM								V_{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM								V_{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM								V_{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM								V_{DDIO}
AD10	GND										GND
AD11	V_{25M3}										V_{25M3}
AD12	GND										GND
AD13	V_{DDM3}										V_{DDM3}
AD14	GND										GND
AD15	V_{25M3}										V_{25M3}
AD16	GND										GND
AD17	V_{DDM3}										V_{DDM3}
AD18	GND										GND
AD19	V_{25M3}										V_{25M3}
AD20	GND										GND
AD21	Reserved[1]										—
AD22	V_{DDDDR}										V_{DDDDR}
AD23	GND										GND
AD24	V_{DDDDR}										V_{DDDDR}
AD25	GND										GND
AD26	V_{DDDDR}										V_{DDDDR}
AD27	GND										GND
AD28	V_{DDDDR}										V_{DDDDR}
AE1	Reserved[1]										—
AE2	GPIO0[3, 6]		GPIO								V_{DDIO}
AE3	GPIO3[3, 6]		GPIO								V_{DDIO}
AE4	TDM1RCLK		TDM								V_{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM								V_{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM								V_{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM								V_{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM								V_{DDIO}
AE9	TDM3TCLK		TDM								V_{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM								V_{DDIO}
AE11	GPIO21/$\overline{IRQ1}$[3, 6]/SPICLK		GPIO/IRQ/SPI								V_{DDIO}
AE12	GND										GND
AE13	Reserved[1]										—
AE14	GND										GND
AE15	Reserved[1]										—
AE16	Reserved[1]										—
AE17	Reserved[1]										—
AE18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V_{DDM3IO}										V_{DDM3IO}
AE21	Reserved[1]										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V_{DDDDR}										V_{DDDDR}
AE26	GND										GND
AE27	V_{DDDDR}										V_{DDDDR}
AE28	GND										GND
AF1	Reserved[1]										—
AF2	V_{DDIO}										V_{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V_{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V_{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V_{DDIO}
AF7	V_{DDIO}										V_{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V_{DDIO}
AF10	TDM2TCLK		TDM								V_{DDIO}
AF11	GPIO22/$\overline{IRQ4}$[3, 6]/SPIMOSI		GPIO/IRQ/SPI								V_{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V_{DDM3IO}										V_{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved[1]										—
AF18	V_{DDM3IO}										V_{DDM3IO}
AF19	GND										GND
AF20	Reserved[1]										—
AF21	Reserved[1]										—
AF22	$\overline{M3\_RESET}$										V_{DDM3IO}
AF23	GND										GND
AF24	V_{DDDDR}										V_{DDDDR}
AF25	GND										GND
AF26	V_{DDDDR}										V_{DDDDR}
AF27	GND										GND
AF28	V_{DDDDR}										V_{DDDDR}
AG1	Reserved[1]										—
AG2	GPIO16/$\overline{IRQ0}$[3, 6]		GPIO/IRQ								V_{DDIO}
AG3	TDM0TCLK		TDM								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM								V_{DDIO}
AG5	TDM0RCLK		TDM								V_{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM								V_{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM								V_{DDIO}
AG8	TDM2RCLK		TDM								V_{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM								V_{DDIO}
AG10	GPIO24/$\overline{\text{IRQ6}}$[3, 6]/$\overline{\text{SPISEL}}$		GPIO/IRQ/SPI								V_{DDIO}
AG11	GPIO23/$\overline{\text{IRQ5}}$[3, 6]/SPIMISO		GPIO/IRQ/SPI								V_{DDIO}
AG12	Reserved[1]										—
AG13	GND										GND
AG14	GND										GND
AG15	GND										GND
AG16	GND										GND
AG17	Reserved[1]										—
AG18	Reserved[1]										—
AG19	GND										GND
AG20	GND										GND
AG21	V_{DDM3IO}										V_{DDM3IO}
AG22	GND										GND
AG23	GND										GND
AG24	GND										GND
AG25	V_{DDDDR}										V_{DDDDR}
AG26	GND										GND
AG27	V_{DDDDR}										V_{DDDDR}
AG28	GND										GND
AH1	Reserved[1]										—
AH2	Reserved[1]										—
AH3	Reserved[1]										—
AH4	Reserved[1]										—
AH5	Reserved[1]										—
AH6	Reserved[1]										—
AH7	Reserved[1]										—
AH8	Reserved[1]										—
AH9	Reserved[1]										—
AH10	Reserved[1]										—
AH11	Reserved[1]										—
AH12	Reserved[1]										—
AH13	Reserved[1]										—
AH14	Reserved[1]										—
AH15	Reserved[1]										—
AH16	Reserved[1]										—

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144E for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144E

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

2.5.1.2 DDR (2.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM component(s) of the MSC8144E when V_{DDDDR}(typ) = 2.5 V.

Table 7. DDR SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	2.3	2.7	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.15$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

Table 8 lists the current draw characteristics for MV_{REF}.

Table 8. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REF}	I_{MVREF}	—	500	µA

Note: The voltage regulator for MV_{REF} must be able to supply up to 500 µA current.

2.5.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.5.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$ are AC-coupled differential inputs. Each differential clock input has an internal 50 Ω termination to GND_{SXC}. The reference clock must be able to drive this termination. The recommended minimum operating voltage is –0.4 V; the recommended maximum operating voltage is 1.32 V; and the maximum absolute voltage is 1.72 V.

The maximum average current allowed in each input is 8 mA. This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 Ω = 8 mA) while the minimum common mode input level is GND_{SXC}. For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from 0 mA to 16 mA (0–0.8 V). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below 90 MHz.

If the device driving the $\overline{\text{SRIO\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC}, or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is 0.4 V (0.2 V peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is 1.6 V peak-to-peak (see Figure 5. The termination to GND_{SXC} allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a 400 mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive 100 mV around common mode voltage. The differential reference clock (SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

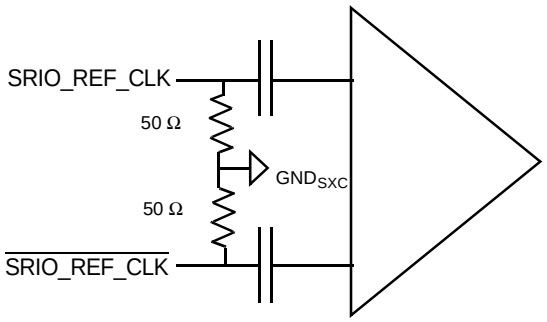


Figure 5. SerDes Reference Clocks Input Stage

Table 19. Timing for a Reset Configuration Write (continued)

No.	Characteristics	Expression	Max	Min	Unit
2	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for external pins and hard coded RCW				
	• 33 MHz <= CLKIN < 66 MHz	15369/CLKIN	615	233	µs
	• 66 MHz <= CLKIN <= 133 MHz	34825/CLKIN	528	262	µs
	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for loading RCW the I^2C interface				
	• 33 MHz <= CLKIN < 44 MHz	92545/CLKIN	3702	2103	µs
	• 44 MHz <= CLKIN < 66 MHz	107435/CLKIN	2441	1627	µs
	• 66 MHz <= CLKIN < 100 MHz	124208/CLKIN	1882	1242	µs
	• 100 MHz <= CLKIN < 133 MHz	157880/CLKIN	1579	1187	µs
3	Delay from $\overline{\text{HRESET}}$ deassertion to $\overline{\text{SRESET}}$ deassertion				
	• REFCLK = 33 MHz to 133 MHz	16/CLKIN	640	120	ns
Note:	Timings are not tested, but are guaranteed by design.				

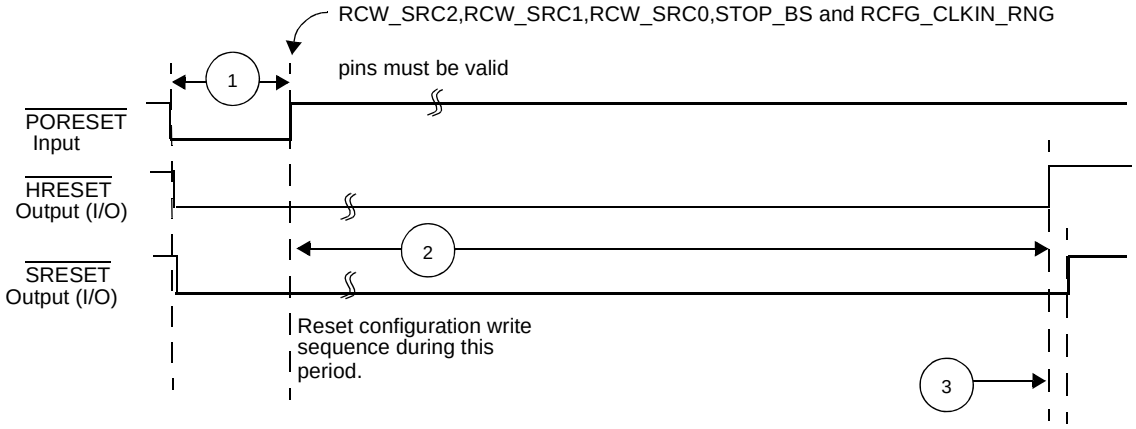


Figure 7. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

Table 29. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 30. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 12 with the parameters specified in Table 31 when measured at the output pins of the device and the device is driving a 100 Ω ±5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

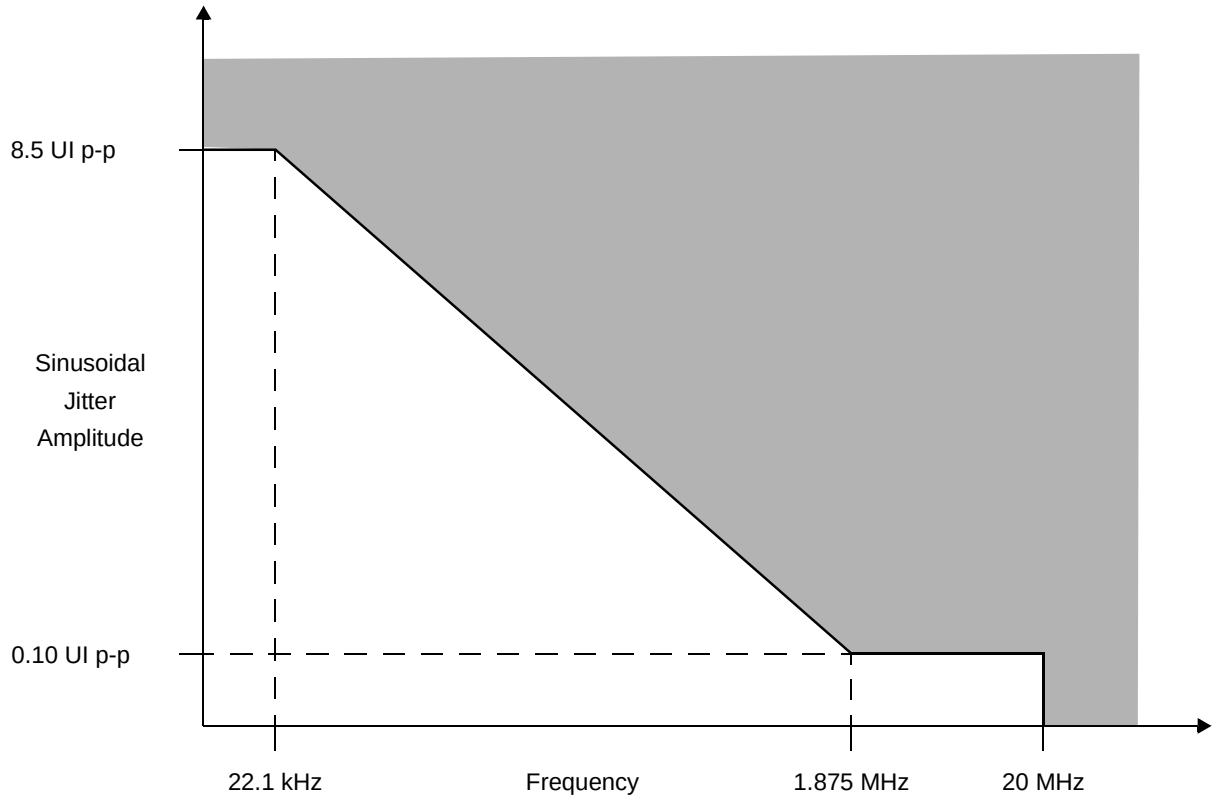
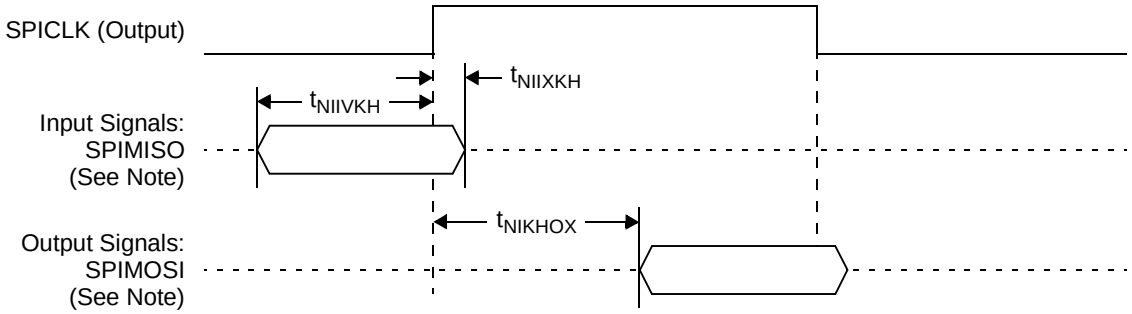


Figure 13. Single Frequency Sinusoidal Jitter Limits



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Master Mode (Internal Clock)

2.6.13 Asynchronous Signal Timing

Table 49. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle[1]
Output	t_{OUT}	Asynchronous	Application dependent
Note: 1. Relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- [illegible] . Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a GPI, the input should be driven until it is acknowledged by the device; the GPIO input status is read from a register.

- [illegible] Signals EE0, EE1, EE2_0, EE2_1, EE2_2, and EE2_3.
- [illegible] . Signal STOP_BS.
- I^2C [illegible] . Signals I2C_SCL and I2C_SDA.
- [illegible] . Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- [illegible] . Signals $\overline{\text{INT\_OUT}}$ and $\overline{\text{NMI\_OUT}}$ (pulse width is 10 ns).

Figure 37 shows the behavior of the asynchronous signals.

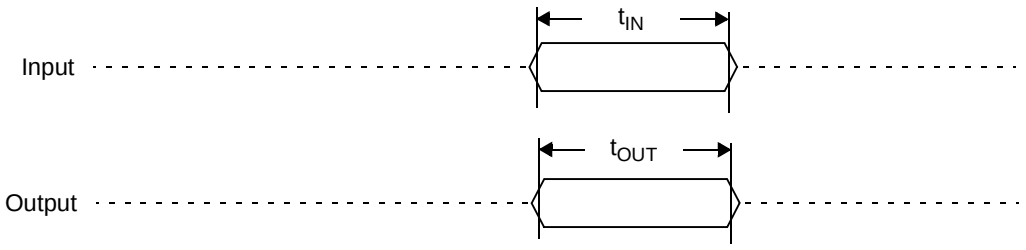


Figure 37. Asynchronous Signal Timing

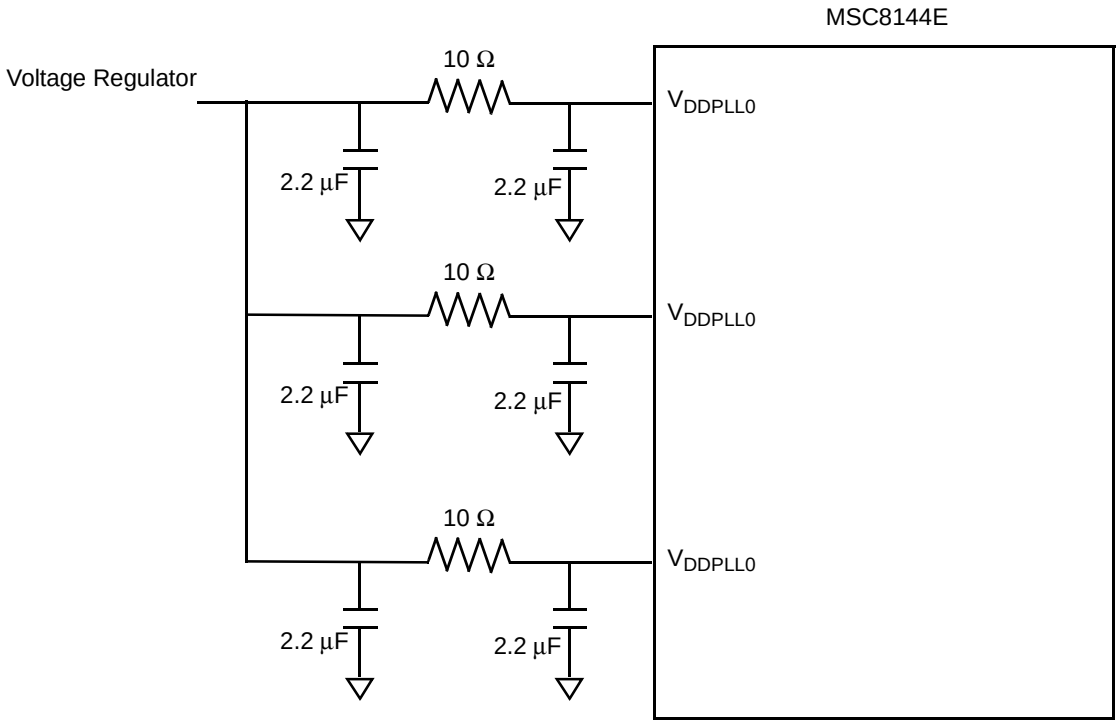


Figure 43. PLL Supplies

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

Note: See (AN3440) for an example layout.

3.4 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor it is clearly indicated as “pull-up/pull-down”.

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

3.4.2.2 Serial RapidIO Specific Lane Is Not Used

Table 55. Connectivity of Serial RapidIO Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	in use
SRIO_IMP_CAL_TX	in use
$\overline{\text{SRIO\_REF\_CLK}}$	in use
SRIO_REF_CLK	in use
SRIO_RXD***x***	GND_{SXC}
$\overline{\text{SRIO\_RXD}\boldsymbol{x}}$	GND_{SXC}
$\overline{\text{SRIO\_TXD}\boldsymbol{x}}$	NC
SRIO_TXD***x***	NC
$V_{DDRIOPLL}$	in use
GND_{RIOPLL}	in use
GND_{SXP}	GND_{SXP}
GND_{SXC}	GND_{SXC}
V_{DDSXP}	1.0 V
V_{DDSXC}	1.0 V
Note: The ***x*** indicates the lane number {0,1,2,3} for all unused lanes.	

3.4.3 M3 Memory Related Pins

Table 56. Connectivity of M3 Related Pins When M3 Memory Is Not Used

Signal Name	Pin Connection
$\overline{\text{M3\_RESET}}$	NC
V_{25M3}	GND
V_{DDM3}	GND
V_{DDM3IO}	GND

3.4.4 Ethernet Related Pins

3.4.4.1 Ethernet Controller 1 (GE1) Related Pins

Note: Table 57 and Table 58 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.1.1 GE1 Interface Is Not Used

Table 57 assumes that the GE1 signals are not used for any purpose (including any multiplexed functions) and that V_{DDGE1} is tied to GND.

Table 57. Connectivity of GE1 Related Pins When the GE1 Interface Is Not Used

Signal Name	Pin Connection
GE1_COL	NC
GE1_CRS	NC
GE1_RD[0–4]	NC
GE1_RX_ER	NC
GE1_RX_CLK	NC
GE1_RX_DV	NC
GE1_SGMII_RX	GND_{SXC}
$\overline{\text{GE1\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE1\_SGMII\_TX}}$	NC
GE1_SGMII_TX	NC
GE1_TD[0–4]	NC
GE1_TX_CLK	NC
GE1_TX_EN	NC
GE1_TX_ER	NC