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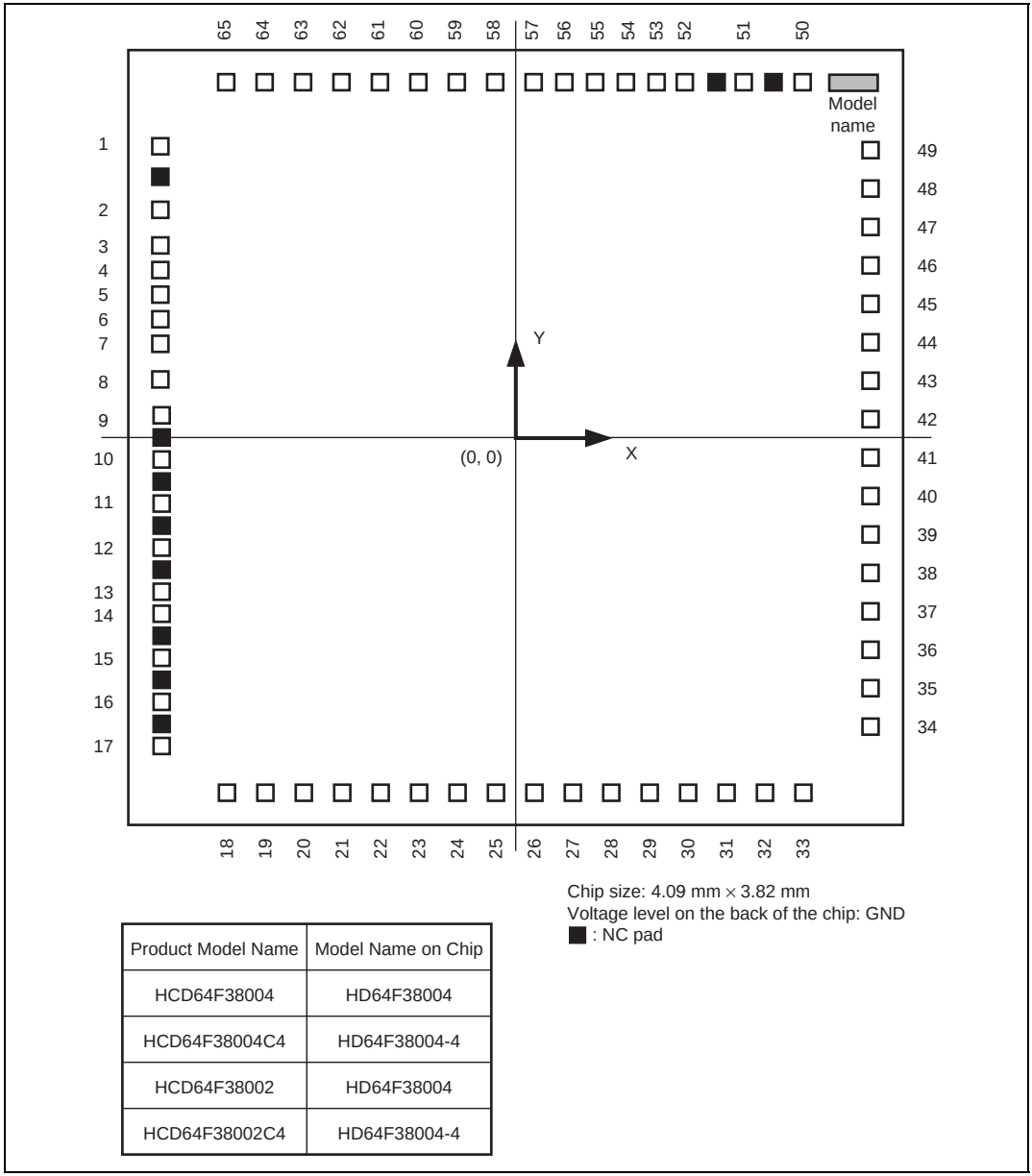
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b SAR
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38002fp4v



Product Model Name	Model Name on Chip
HCD64F38004	HD64F38004
HCD64F38004C4	HD64F38004-4
HCD64F38002	HD64F38004
HCD64F38002C4	HD64F38004-4

Figure 1.9 Pad Arrangement of HCD64F38004 and HCD64F38002 (Top View)

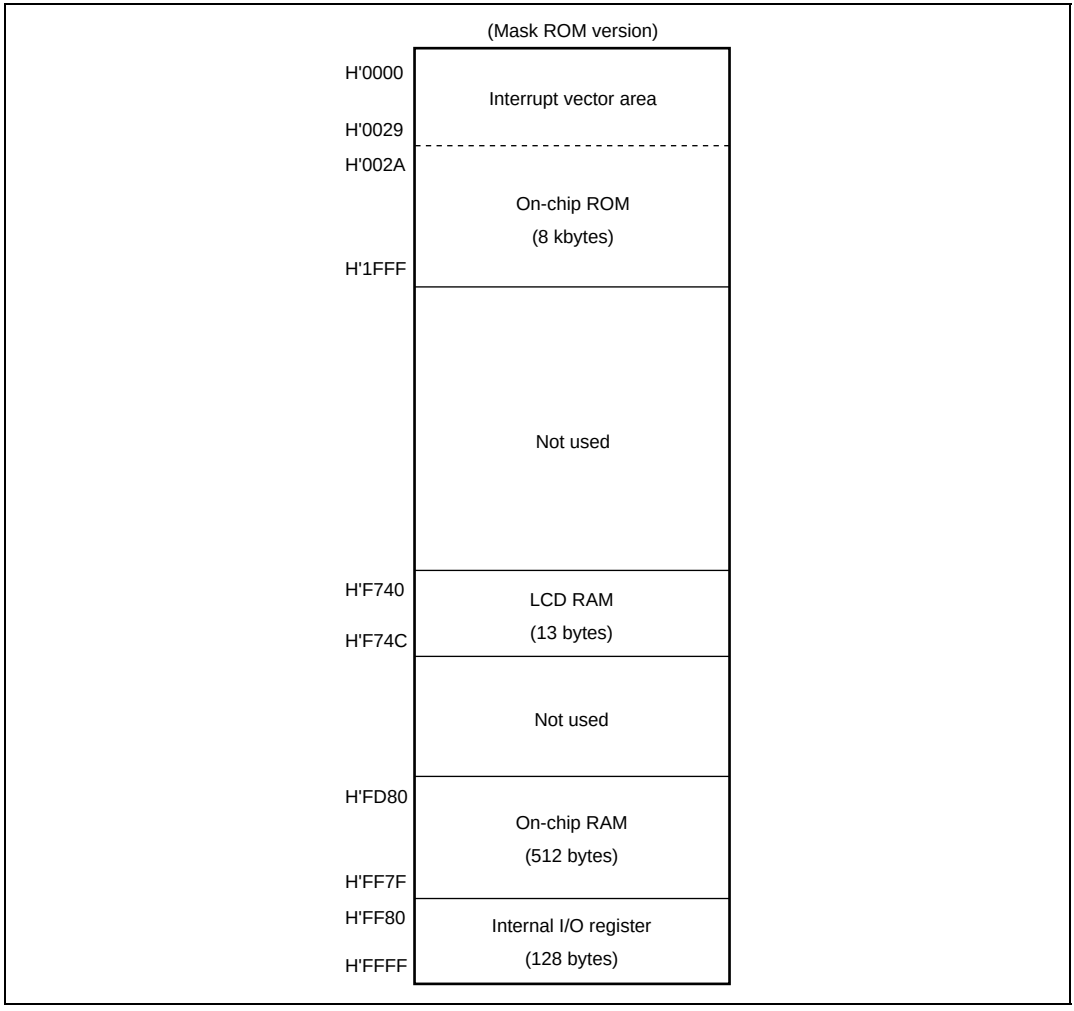


Figure 2.1(9) H8/38000, H8/38000S, H8/38100 Memory Map

2.5.1 Data Transfer Instructions

Table 2.3 describes the data transfer instructions.

Table 2.3 Data Transfer Instructions

Instruction	Size*	Function
MOV	B/W	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register. The Rn, @Rn, @(d:16, Rn), @aa:16, #xx:16, @–Rn, and @Rn+ addressing modes are available for word data. The @aa:8 addressing mode is available for byte data only. The @–R7 and @R7+ modes require word operands. Do not specify byte size for these two modes.
POP	W	@SP+ → Rn Pops a general register from the stack. Equivalent to MOV.W@SP+, Rn.
PUSH	W	Rn → @–SP Pushes a general register onto the stack. Equivalent to MOV.W Rn, @–SP.

Note: * Refers to the operand size.
B: Byte
W: Word

For details on data access, see section 2.9.1, Notes on Data Access to Empty Areas and section 2.9.2, Access to Internal I/O Registers.

Figure 2.6 shows the instruction formats of data transfer instructions.

Register Indirect—@Rn

The register field of the instruction specifies a 16-bit general register containing the address of the operand in memory.

Register Indirect with Displacement—@(d:16, Rn)

The instruction has a second word (bytes 3 and 4) containing a displacement which is added to the contents of the specified general register (16 bits) to obtain the operand address in memory.

This mode is used only in MOV instructions. For the MOV.W instruction, the resulting address must be even.

Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @-Rn

- Register indirect with post-increment—@Rn+

  The @Rn+ mode is used with MOV instructions that load registers from memory.

  The register field of the instruction specifies a 16-bit general register containing the address of the operand. After the operand is accessed, the register is incremented by 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.
- Register indirect with pre-decrement—@–Rn

  The @–Rn mode is used with MOV instructions that store register contents to memory.

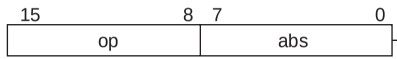
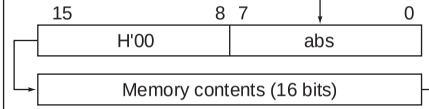
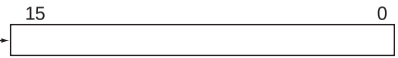
  The register field of the instruction specifies a 16-bit general register which is decremented by 1 or 2 to obtain the address of the operand in memory. The register retains the decremented value. The size of the decrement is 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the register must be even.

Absolute Address—@aa:8/@aa:16

The instruction specifies the absolute address of the operand in memory.

The absolute address may be 8 bits long (@aa:8) or 16 bits long (@aa:16). The MOV.B and bit manipulation instructions can use 8-bit absolute addresses. The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

For an 8-bit absolute address, the upper 8 bits are assumed to be 1 (H'FF). The address range is H'FF00 to H'FFFF (65280 to 65535).

No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
8	Memory indirect@@aa:8 		

Legend:

rm, rn: Register field
op: Operation field
disp: Displacement
IMM: Immediate data
abs: Absolute address

5.1.3 Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2)

CKSTPR1 and CKSTPR2 allow the on-chip peripheral modules to enter a standby state in module units.

- CKSTPR1

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved
5	S32CKSTP	1	R/W	SCI Module Standby SCI3 enters standby mode when this bit is cleared to 0.*1
4	ADCKSTP	1	R/W	A/D Converter Module Standby A/D converter enters standby mode when this bit is cleared to 0.
3	—	1	—	Reserved
2	TFCKSTP	1	R/W	Timer F Module Standby Timer F enters standby mode when this bit is cleared to 0.
1	—	1	—	Reserved
0	TACKSTP	1	R/W	Timer A Module Standby*2 Timer A enters standby mode when this bit is cleared to 0.

8. The maximum number of repetitions of the program/program-verify sequence of the same bit is 1,000.

8.1.6 Pin Functions

The port 3 pin functions are shown below.

- P37/AEVL pin

The pin function depends on the combination of bit AEVL in PMR3 and bit PCR37 in PCR3.

AEVL	0		1
PCR37	0	1	*
Pin Function	P37 input pin	P37 output pin	AEVL input pin

Legend: *: Don't care.

- P36/AEVH pin

The pin function depends on the combination of bit AEVH in PMR3 and bit PCR36 in PCR3.

AEVH	0		1
PCR36	0	1	*
Pin Function	P36 input pin	P36 output pin	AEVH input pin

Legend: *: Don't care.

- P35 to P33 pins

The pin function depends on the corresponding bit in PCR3.

(n = 5 to 3)

PCR3n	0	1
Pin Function	P3n input pin	P3n output pin

- P32/TMOFH pin

The pin function depends on the combination of bit TMOFH in PMR3 and bit PCR32 in PCR3.

TMOFH	0		1
PCR32	0	1	*
Pin Function	P32 input pin	P32 output pin	TMOFH output pin

Legend: *: Don't care.

Bit	Bit Name	Initial Value	R/W	Description
0	WRST	0	R/(W)*1	Watchdog Timer Reset [Setting condition] When TCW overflows and an internal reset signal is generated [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit while writing 0 to the B0WI bit when the TCSRWE bit = 1

Notes: 1. These bits can be written only when the writing conditions are satisfied.
2. Initial value 0 on H8/38004, H8/38002S Group and 1 on H8/38104 Group.
3. On reset, cleared to 0 on H8/38004, H8/38002S Group and set to 1 on H8/38104 Group.

Timer Counter W (TCW): TCW is an 8-bit readable/writable up-counter. When TCW overflows from H'FF to H'00, the internal reset signal is generated and the WRST bit in TCSRW is set to 1. TCW is initialized to H'00.

Timer Mode Register W (TMW): TMW selects the input clock. Clock source selection using this register is enabled when WDCKS in port mode register 2 (PMR2) is cleared to 0. If WDCKS is set to 1, $\phi w/32$ is selected as the clock source, regardless of the setting of TMW.

Note: TMW is implemented on H8/38104 Group only.

Section 10 Serial Communication Interface 3 (SCI3)

Serial Communication Interface 3 (SCI3) can handle both asynchronous and clocked synchronous serial communication. In the asynchronous method, serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA).

Figure 10.1 shows a block diagram of the SCI3.

10.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- External clock or on-chip baud rate generator can be selected as a transfer clock source.
- Six interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, overrun error, framing error, and parity error.

Note: On the H8/38104 Group, the system clock generator must be used when carrying out this function.

Asynchronous mode

- Data length: 7, 8, or 5 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RXD32 pin level directly in the case of a framing error

Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors detected

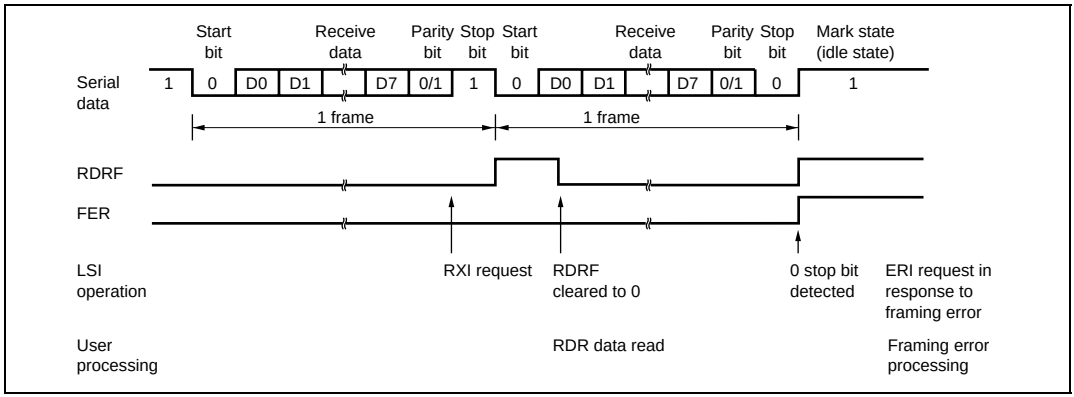


Figure 10.7 Example SCI3 Operation in Reception in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

Table 10.10 shows the states of the SSR status flags and receive data handling when a receive error is detected. If a receive error is detected, the RDRF flag retains its state before receiving data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the OER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 10.8 shows a sample flowchart for serial data reception.

Table 10.10 SSR Status Flags and Receive Data Handling

SSR Status Flag					
RDRF*	**OER**	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	1	0	0	Lost	Overrun error
0	0	1	0	Transferred to RDR	Framing error
0	0	0	1	Transferred to RDR	Parity error
1	1	1	0	Lost	Overrun error + framing error
1	1	0	1	Lost	Overrun error + parity error
0	0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	1	Lost	Overrun error + framing error + parity error

Note: * The RDRF flag retains the state it had before data reception. However, note that if RDR is read after an overrun error has occurred in a frame because reading of the receive data in the previous frame was delayed, the RDRF flag will be cleared to 0.

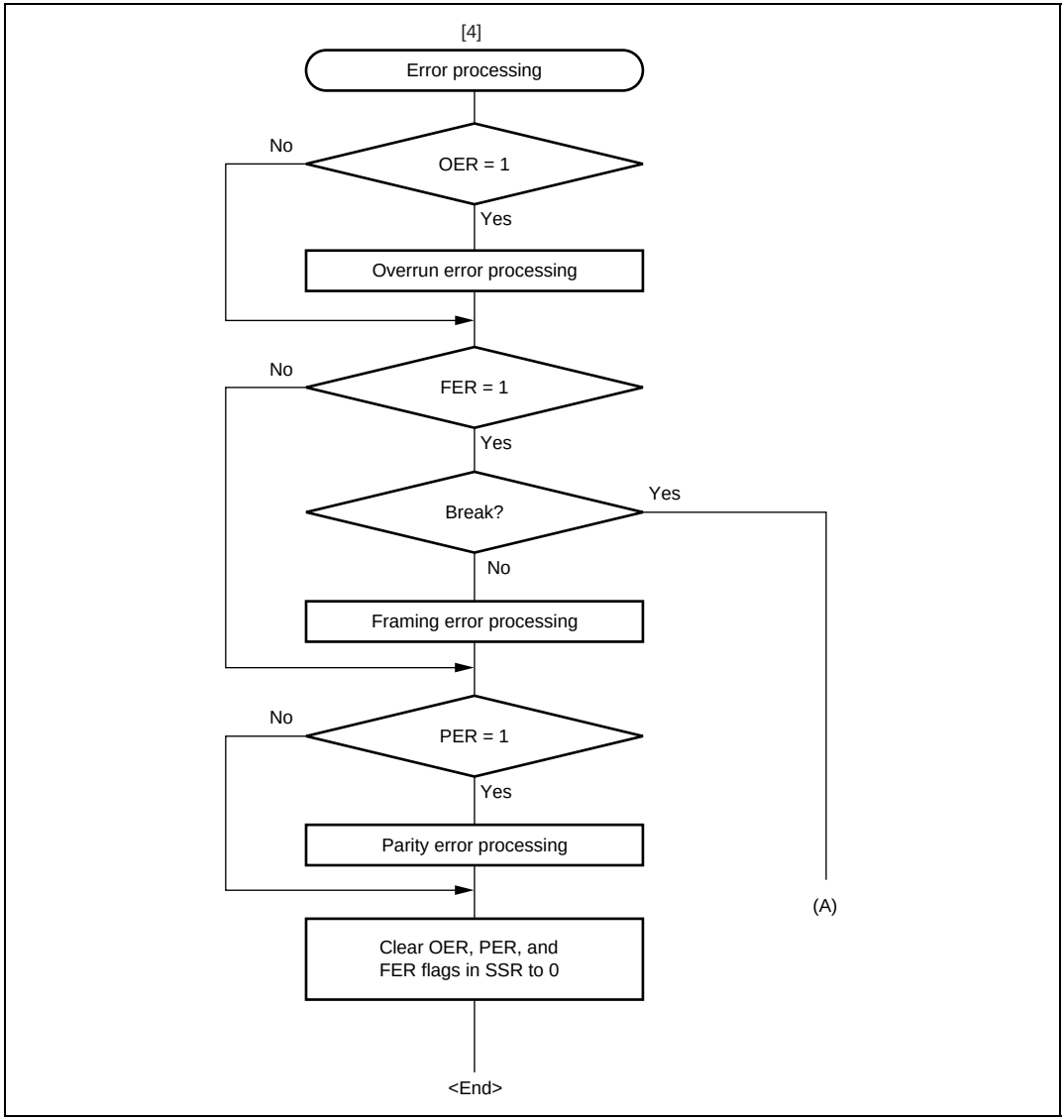


Figure 10.8 Sample Serial Data Reception Flowchart (Asynchronous Mode) (2)

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
Transmit data register	TDR	8	H'FFAB	SCI3	8	3
Serial status register	SSR	8	H'FFAC	SCI3	8	3
Receive data register	RDR	8	H'FFAD	SCI3	8	3
Timer mode register A	TMA	8	H'FFB0	Timer A	8	2
Timer counter A	TCA	8	H'FFB1	Timer A	8	2
Timer control/status register W	TCSRW	8	H'FFB2	WDT*2	8	2
Timer counter W	TCW	8	H'FFB3	WDT*2	8	2
Timer control register F	TCRF	8	H'FFB6	Timer F	8	2
Timer control status register F	TCSRF	8	H'FFB7	Timer F	8	2
8-bit timer counter FH	TCFH	8	H'FFB8	Timer F	8	2
8-bit timer counter FL	TCFL	8	H'FFB9	Timer F	8	2
Output compare register FH	OCRFH	8	H'FFBA	Timer F	8	2
Output compare register FL	OCRFL	8	H'FFBB	Timer F	8	2
LCD port control register	LPCR	8	H'FFC0	LCD*3	8	2
LCD control register	LCR	8	H'FFC1	LCD*3	8	2
LCD control register 2	LCR2	8	H'FFC2	LCD*3	8	2
Low-voltage detection counter*4	LVDCNT	8	H'FFC3	LVD	8	2
A/D result register H	ADRRH	8	H'FFC4	A/D converter	8	2
A/D result register L	ADRRL	8	H'FFC5	A/D converter	8	2
A/D mode register	AMR	8	H'FFC6	A/D converter	8	2
A/D start register	ADSR	8	H'FFC7	A/D converter	8	2
Port mode register 2	PMR2	8	H'FFC9	I/O port	8	2
Port mode register 3	PMR3	8	H'FFCA	I/O port	8	2
Port mode register 5	PMR5	8	H'FFCC	I/O port	8	2
PWM2 control register	PWCR2	8	H'FFCD	10-bit PWM	8	2
PWM2 data register U	PWDRU2	8	H'FFCE	10-bit PWM	8	2
PWM2 data register L	PWDRL2	8	H'FFCF	10-bit PWM	8	2
PWM1 control register	PWCR1	8	H'FFD0	10-bit PWM	8	2
PWM1 data register U	PWDRU1	8	H'FFD1	10-bit PWM	8	2
PWM1 data register L	PWDRL1	8	H'FFD2	10-bit PWM	8	2
Port data register 3	PDR3	8	H'FFD6	I/O port	8	2
Port data register 4	PDR4	8	H'FFD7	I/O port	8	2

Section 17 Electrical Characteristics

17.1 Absolute Maximum Ratings of H8/3802 Group (ZTAT Version, Mask ROM Version)

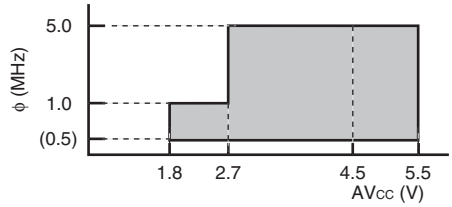
Table 17.1 lists the absolute maximum ratings.

Table 17.1 Absolute Maximum Ratings

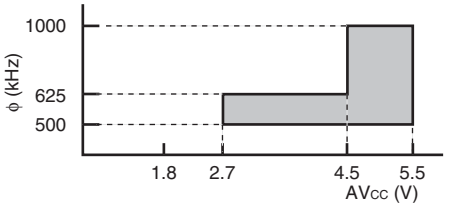
Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +7.0	V	*
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V	
Programming voltage		V_{PP}	–0.3 to +13.0	V	
Input voltage	Other than port B and IRQAEC	V_{in}	–0.3 to V_{CC} +0.3	V	
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	
	IRQAEC	HV_{in}	–0.3 to +7.3	V	
Port 9 pin voltage		V_{P9}	–0.3 to +7.3	V	
Operating temperature		T_{opr}	Regular specifications: –20 to +75	°C	
			Wide-range temperature specifications: –40 to +85		
Storage temperature		T_{stg}	–55 to +125	°C	

Note: * Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

Analog Power Supply Voltage and A/D Converter Operating Range



• Active (high-speed) mode
• Sleep (high-speed) mode



• Active (medium-speed) mode
• Sleep (medium-speed) mode

Note: When AVcc = 1.8 V to 2.7 V, the operating range is limited to φ = 1.0 MHz when using a resonator and is φ = 0.5 MHz to 1.0 MHz when using an external clock.

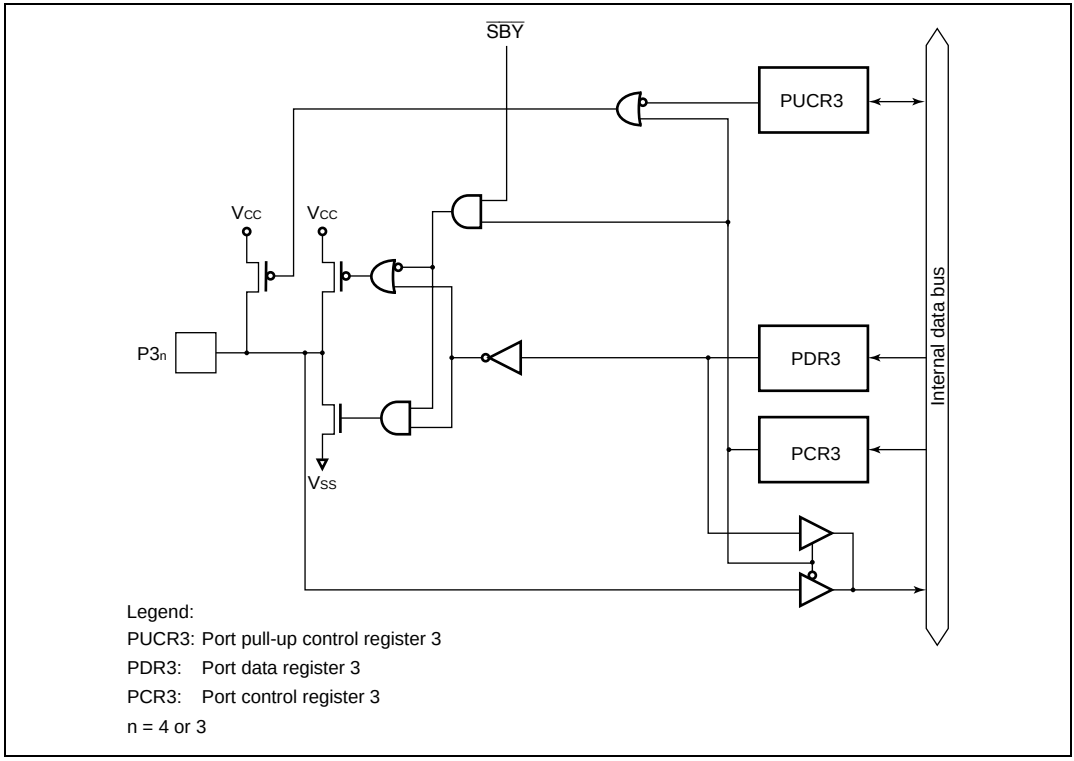


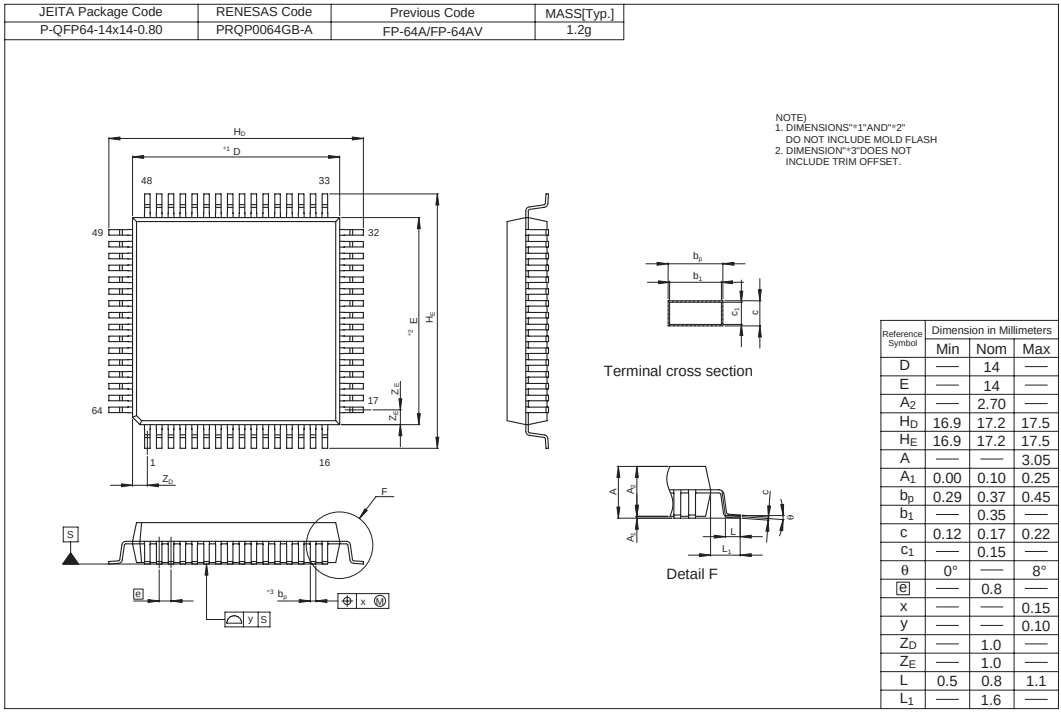
Figure B.1(c) Port 3 Block Diagram (Pins P34 and P33)

Appendix E Package Dimensions

The package dimensions are shown in figure E.1 (FP-64A), figure E.2 (FP-64E), figure E.3 (FP-64K), figure E.4 (DP-64S), and figure E.5 (TNP-64B).

The package dimension that is shown in the Renesas Semiconductor Package Data Book has Priority.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP64-14x14-0.80	PRQP0064GB-A	FP-64A/FP-64AV	1.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	2.70	—
H_D	16.9	17.2	17.5
H_E	16.9	17.2	17.5
A	—	—	3.05
A_1	0.00	0.10	0.25
b_p	0.29	0.37	0.45
b_1	—	0.35	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.15
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.5	0.8	1.1
L_1	—	1.6	—

Figure E.1 Package Dimensions (FP-64A)

H8/3802, H8/38004, H8/38002S, H8/38104 Group Hardware Manual

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REJ09B0024-0700