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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38004fp10v

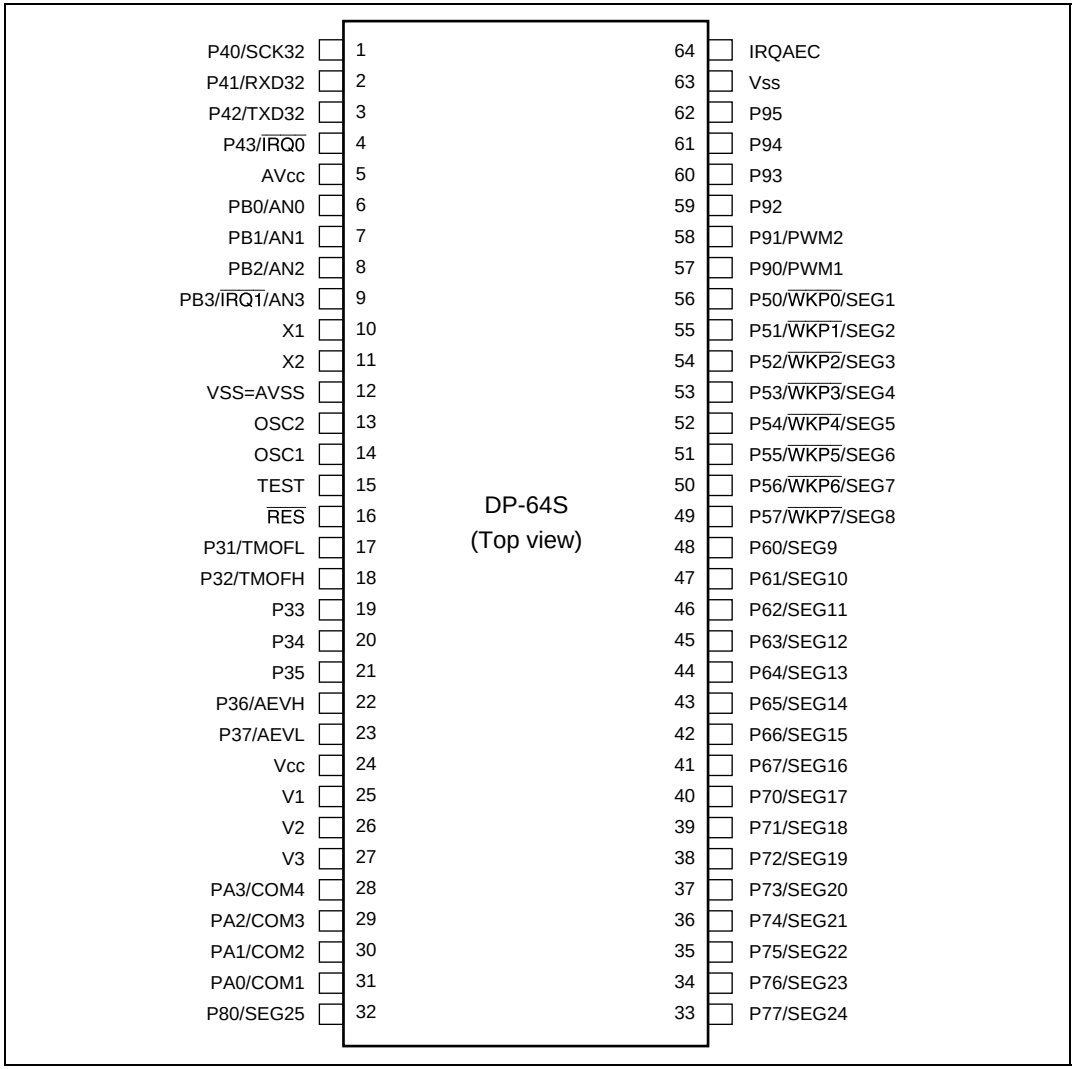


Figure 1.5 Pin Arrangement of H8/3802 Group (DP-64S)

Table 1.1 Pad Coordinate of HCD6433802, HCD6433801, and HCD6433800

Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)	Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)
1	PB3/$\overline{\text{IRQ1}}$/AN3	-1677	1495	32	P71/SEG18	1400	-1742
2	X1	-1677	1084	33	P70/SEG17	1578	-1742
3	X2	-1677	943	34	P67/SEG16	1677	-1401
4	AVss	-1677	765	35	P66/SEG15	1677	-1190
5	Vss	-1677	619	36	P65/SEG14	1677	-950
6	OSC2	-1677	488	37	P64/SEG13	1677	-801
7	OSC1	-1677	356	38	P63/SEG12	1677	-608
8	TEST	-1677	225	39	P62/SEG11	1677	-459
9	$\overline{\text{RES}}$	-1677	94	40	P61/SEG10	1677	-310
10	P31/TMOFL	-1677	-40	41	P60/SEG9	1677	-160
11	P32/TMOFH	-1677	-176	42	P57/$\overline{\text{WKP7}}$/SEG8	1677	-11
12	P33	-1677	-313	43	P56/$\overline{\text{WKP6}}$/SEG7	1677	121
13	P34	-1677	-450	44	P55/$\overline{\text{WKP5}}$/SEG6	1677	252
14	P35	-1677	-587	45	P54/$\overline{\text{WKP4}}$/SEG5	1677	383
15	P36/AEVH	-1677	-943	46	P53/$\overline{\text{WKP3}}$/SEG4	1677	801
16	P37/AEVL	-1677	-1083	47	P52/$\overline{\text{WKP2}}$/SEG3	1677	950
17	Vcc	-1677	-1404	48	P51/$\overline{\text{WKP1}}$/SEG2	1677	1190
18	V1	-1578	-1742	49	P50/$\overline{\text{WKP0}}$/SEG1	1677	1402
19	V2	-1339	-1742	50	P90/PWM1	1578	1742
20	V3	-1193	-1742	51	P91/PWM2	1411	1742
21	PA3/COM4	-1049	-1742	52	P92	1193	1742
22	PA2/COM3	-850	-1742	53	P93	1051	1742
23	PA1/COM2	-400	-1742	54	P94	850	1742
24	PA0/COM1	-200	-1742	55	P95	650	1742
25	P80/SEG25	0	-1742	56	Vss	400	1742
26	P77/SEG24	320	-1742	57	IRQAEC	200	1742
27	P76/SEG23	451	-1742	58	P40/SCK32	-298	1742
28	P75/SEG22	583	-1742	59	P41/RXD32	-435	1742
29	P74/SEG21	850	-1742	60	P42/TXD32	-572	1742
30	P73/SEG20	1051	-1742	61	P43/$\overline{\text{IRQ0}}$	-752	1742
31	P72/SEG19	1193	-1742	62	AVcc	-1036	1742

Type	Symbol	Pin No. FP-64A, FP-64E, FP-64K, TNP-64B	Pin No. DP-64S	Pad No.*1*3	Pad No.*2	I/O	Functions
Clock pins	X1	2	10	2	2	Input	These pins connect to a 32.768- or 38.4-kHz*5 crystal resonator for subclocks. See section 4, Clock Pulse Generators, for a typical connection.
	X2	3	11	3	3	Output	
System control	$\overline{\text{RES}}$	8	16	9	8	Input	Reset pin. When this driven low, the chip is reset.
	TEST	7	15	8	7	Input	Test pin. Connect this pin to V_{ss}. Users cannot use this pin.
Interrupt pins	$\overline{\text{IRQ0}}$	60	4	61	60	Input	External interrupt request input pins. Can select the rising or falling edge.
	$\overline{\text{IRQ1}}$	1	9	1	1		
	IRQAEC	56	64	57	56	Input	Asynchronous event counter interrupt input pin. Enables asynchronous event input. On the H8/38104 Group, this must be fixed at V_{cc} or GND because the oscillator is selected by the input level during resets. Refer to section 4, Clock Pulse Generators, for information on the selection method.
	$\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$	41 to 48	49 to 56	42 to 49	41 to 48	Input	Wakeup interrupt request input pins. Can select the rising or falling edge.
Timer	AEVL AEVH	15 14	23 22	16 15	15 14	Input	This is an event input pin for input to the asynchronous event counter.
	TMOFL	9	17	10	9	Output	This is an output pin for waveforms generated by the timer FL output compare function.

2.5.3 Logic Operations Instructions

Table 2.5 describes the logic operations instructions.

Table 2.5 Logic Operations Instructions

Instruction	Size*	Function
AND	B	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	¬ (Rd) → (Rd) Obtains the one's complement (logical complement) of general register contents.

Note: * Refers to the operand size.
B: Byte

2.5.4 Shift Instructions

Table 2.6 describes the shift instructions.

Table 2.6 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B	Rd (rotate) → Rd Rotates general register contents through the carry flag.

Note: * Refers to the operand size.
B: Byte

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	—
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	1	1

BCLR instruction executed

```
BCLR   #1,    @RAM0
```

The BCLR instructions executed for the PCR3 work area (RAM0).

After executing BCLR

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR3
```

The work area (RAM0) value is written to PCR3.

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	High level	—
PCR3	0	0	1	1	1	1	0	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	0	1

In the above example, an IRQ0 interrupt occurs while the AND.B instruction is executed. Since not only the original target IRRI1, but also IRRI0 is cleared to 0, the IRQ0 interrupt becomes invalid.

3.5.4 Notes on Rewriting Port Mode Registers

When a port mode register is rewritten to switch the functions of external interrupt pins, IRQAEC, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$, the interrupt request flag may be set to 1.

When switching a pin function, mask the interrupt before setting the bit in the port mode register. After accessing the port mode register, execute at least one instruction (e.g., NOP), then clear the interrupt request flag from 1 to 0.

Table 3.3 lists the interrupt request flags which are set to 1 and the conditions.

Table 3.3 Conditions under which Interrupt Request Flag Is Set to 1

Interrupt Request Flags Set to 1		Conditions
IRR1	IRREC2	When the edge designated by AIEGS1 and AIEGS0 in AEGSR is input while IENEC2 in IENRI is set to 1.
	IRRI1	When IRQ1 bit in PMRB is changed from 0 to 1 while pin $\overline{\text{IRQ1}}$ is low and IEG1 bit in IEGR = 0.
		When IRQ1 bit in PMRB is changed from 1 to 0 while pin $\overline{\text{IRQ1}}$ is low and IEG1 bit in IEGR = 1.
	IRRI0	When IRQ0 bit in PMR2 is changed from 0 to 1 while pin $\overline{\text{IRQ0}}$ is low and IEG0 bit in IEGR = 0.
		When IRQ0 bit in PMR2 is changed from 1 to 0 while pin $\overline{\text{IRQ0}}$ is low and IEG0 bit in IEGR = 1.

5.1.2 System Control Register 2 (SYSCR2)

SYSCR2 controls the power-down modes, as well as SYSCR1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select Selects the frequency at which the watch clock signal (ϕ_w) generated by the subclock pulse generator is sampled, in relation to the oscillator clock (ϕ_{osc}) generated by the system clock pulse generator. When ϕ_{osc} = 2 to 16 MHz, clear this bit to 0. 0: Sampling rate is ϕ_{osc}/16. 1: Sampling rate is ϕ_{osc}/4.
3	DTON	0	R/W	Direct Transfer on Flag Selects the mode to which the transition is made after the SLEEP instruction is executed with bits SSBY and LSON in SYSCR1, bit MSON in SYSCR2, and bit TMA3 in TMA. For details, see table 5.2.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode. 0: Operation in active (high-speed) mode 1: Operation in active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

Legend: X: Don't care.

5.3 Direct Transition

The CPU can execute programs in two modes: active and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition also enables operating frequency modification in active or subactive mode. After the mode transition, direct transition interrupt exception handling starts.

If the direct transition interrupt is disabled in interrupt permission register 2, a transition is made instead to sleep or watch mode. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or watch mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

- Direct transfer from active (high-speed) mode to active (medium-speed) mode

  When a SLEEP instruction is executed in active (high-speed) mode while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is set to 1, and the DTON bit in SYSCR2 is set to 1, a transition is made to active (medium-speed) mode via sleep mode.
- Direct transfer from active (medium-speed) mode to active (high-speed) mode

  When a SLEEP instruction is executed in active (medium-speed) mode while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is cleared to 0, and the DTON bit in SYSCR2 is set to 1, a transition is made to active (high-speed) mode via sleep mode.
- Direct transfer from active (high-speed) mode to subactive mode

  When a SLEEP instruction is executed in active (high-speed) mode while the SSBY and LSON bits in SYSCR1 are set to 1, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made to subactive mode via watch mode.
- Direct transfer from subactive mode to active (high-speed) mode

  When a SLEEP instruction is executed in subactive mode while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, the MSON bit in SYSCR2 is cleared to 0, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made directly to active (high-speed) mode via watch mode after the waiting time set in bits STS2 to STS0 in SYSCR1 has elapsed.
- Direct transfer from active (medium-speed) mode to subactive mode

  When a SLEEP instruction is executed in active (medium-speed) while the SSBY and LSON bits in SYSCR1 are set to 1, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made to subactive mode via watch mode.

by re-setting the P or E bit. However, PV and EV bit setting is enabled, and a transition can be made to verify mode. Error protection can be cleared only by a power-on reset.

6.10 Programmer Mode

In programmer mode, a PROM programmer can be used to perform programming/erasing via a socket adapter, just as a discrete flash memory. Use a PROM programmer that supports the MCU device type with the on-chip Renesas Technology 64-kbyte flash memory (FZTAT64V3). A 10-MHz input clock is required. For the conditions for transition to programmer mode, see table 6.5.

6.10.1 Socket Adapter

The socket adapter converts the pin allocation of the HD64F38004, HD64F38002, HD64F38104, and HD64F38102 to that of the discrete flash memory HN28F101. The address of the on-chip flash memory is H'0000 to H'7FFF. Figure 6.12(1) shows a socket-adapter-pin correspondence diagram of the HD64F38004 and HD64F38002. Figure 6.12(2) shows a socket-adapter-pin correspondence of the HD64F38104 and HD64F38102.

6.10.2 Programmer Mode Commands

The following commands are supported in programmer mode.

- Memory Read Mode
- Auto-Program Mode
- Auto-Erase Mode
- Status Read Mode

Status polling is used for auto-programming, auto-erasing, and status read modes. In status read mode, detailed internal information is output after the execution of auto-programming or auto-erasing. Table 6.11 shows the sequence of each command. In auto-programming mode, 129 cycles are required since 128 bytes are written at the same time. In memory read mode, the number of cycles depends on the number of address write cycles (n).

8.1.3 Port Pull-Up Control Register 3 (PUCR3)

PUCR3 controls whether the pull-up MOS of each of the port 3 pins is on or off.

Bit	Bit Name	Initial Value	R/W	Description
7	PUCR37	0	R/W	When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.
6	PUCR36	0	R/W	
5	PUCR35	0	R/W	
4	PUCR34	0	R/W	
3	PUCR33	0	R/W	
2	PUCR32	0	R/W	
1	PUCR31	0	R/W	
0	—	—	W	Reserved The write value should always be 0.

8.6.1 Port Data Register 8 (PDR8)

PDR8 is a register that stores data of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	—	—	Reserved
0	P80	0	R/W	If port 8 is read while PCR8 bits are set to 1, the values stored in PDR8 are read, regardless of the actual pin states. If port 8 is read while PCR8 bits are cleared to 0, the pin states are read.

8.6.2 Port Control Register 8 (PCR8)

PCR8 controls whether each of the port 8 pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	—	W	Reserved The write value should always be 0.
0	PCR80	0	W	Setting a PCR8 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR8 and in PDR8 are valid only when the corresponding pin is designated by the SGS3 to SGS0 bits in LPCR as a general I/O pin. PCR8 is a write-only register.

Section 10 Serial Communication Interface 3 (SCI3)

Serial Communication Interface 3 (SCI3) can handle both asynchronous and clocked synchronous serial communication. In the asynchronous method, serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA).

Figure 10.1 shows a block diagram of the SCI3.

10.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- External clock or on-chip baud rate generator can be selected as a transfer clock source.
- Six interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, overrun error, framing error, and parity error.

Note: On the H8/38104 Group, the system clock generator must be used when carrying out this function.

Asynchronous mode

- Data length: 7, 8, or 5 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RXD32 pin level directly in the case of a framing error

Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors detected

10.3.7 Serial Status Register (SSR)

SSR is a register containing status flags of the SCI3 and multiprocessor bits for transfer. 1 cannot be written to flags TDRE, RDRF, OER, PER, and FER; they can only be cleared. SSR is initialized to H'84 at a reset and in standby, watch, or module standby mode.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Indicates that transmit data is stored in TDR. [Setting conditions] • When the TE bit in SCR3 is 0 • When data is transferred from TDR to TSR [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the transmit data is written to TDR
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates that the received data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When data is read from RDR If an error is detected in reception, or if the RE bit in SCR3 has been cleared to 0, RDR and bit RDRF are not affected and retain their previous state. Note that if data reception is completed while bit RDRF is still set to 1, an overrun error (OER) will occur and the receive data will be lost.

Table 10.2 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)

	φ											
	16.4 kHz			19.45 kHz			1 MHz			1.2288 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	—	—	—	—	—	—	2	17	–1.36	2	21	–0.83
150	—	—	—	0	3	0	2	12	0.16	3	3	0
200	—	—	—	0	2	0	2	9	–2.34	3	2	0
250	0	1	2.5	—	—	—	3	1	–2.34	0	153	–0.26
300	—	—	—	0	1	0	0	103	0.16	3	1	0
600	—	—	—	0	0	0	0	51	0.16	3	0	0
1200				—	—	—	0	25	0.16	2	1	0
2400							0	12	0.16	2	0	0
4800							—	—	—	0	7	0
9600							—	—	—	0	3	0
19200							—	—	—	0	1	0
31250							0	0	0	—	—	—
38400							—	—	—	0	0	0

14.2.2 Low-Voltage Detection Status Register (LVDSR)

LVDSR is used to control external input selection, indicates when the reference voltage is stable, and indicates if the power supply voltage goes below or above a specified range.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0*	R/W	LVD Reference Voltage Stabilized Flag Setting condition: When the low-voltage detection counter (LVDCNT) overflows Clearing condition: When 0 is written after reading 1
6 to 4	—	All 0	R/W	These are read/write enabled reserved bits.
3	VREFSEL	0	R/W	Reference Voltage External Input Select 0: The on-chip circuit is used to generate the reference voltage 1: The reference voltage is input to the Vref pin from an external source
2	—	0	R/W	This bit is reserved. It is always read as 0 and cannot be written to.
1	LVDDF	0*	R/W	LVD Power Supply Voltage Drop Flag Setting condition: When the power supply voltage drops below Vint(D) Clearing condition: When 0 is written after reading 1
0	LVDUF	0*	R/W	LVD Power Supply Voltage Rise Flag Setting condition: When the power supply voltage drops below Vint(D) while the LVDUE bit in LVDCR is set to 1, and it rises above Vint(U) before dropping below Vreset1 Clearing condition: When 0 is written after reading 1

Note: * These bits are initialized by resets trigged by LVDR.

Section 15 Power Supply Circuit (H8/38104 Group Only)

This LSI incorporates an internal power supply step-down circuit. Use of this circuit enables the internal power supply to be fixed at a constant level of approximately 3.0 V, independently of the voltage of the power supply connected to the external V_{cc} pin. As a result, the current consumed when an external power supply is used at 3.0 V or above can be held down to virtually the same low level as when used at approximately 3.0 V. If the external power supply is 3.0 V or below, the internal voltage will be practically the same as the external voltage. It is, of course, also possible to use the same level of external power supply voltage and internal power supply voltage without using the internal power supply step-down circuit.

15.1 When Using Internal Power Supply Step-Down Circuit

Connect the external power supply to the V_{cc} pin, and connect a capacitance of approximately 0.1 μF between CV_{cc} and V_{ss}, as shown in figure 15.1. The internal step-down circuit is made effective simply by adding this external circuit. In the external circuit interface, the external power supply voltage connected to V_{cc} and the GND potential connected to V_{ss} are the reference levels. For example, for port input/output levels, the V_{cc} level is the reference for the high level, and the V_{ss} level is that for the low level. The A/D converter analog power supply is not affected by the internal step-down circuit.

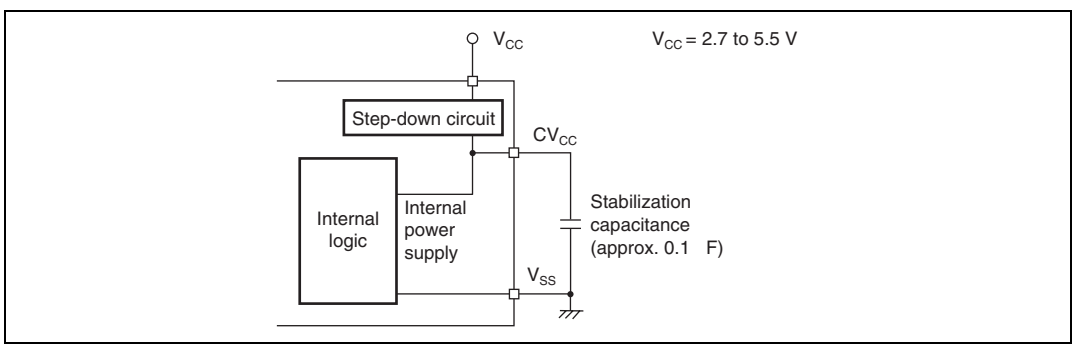
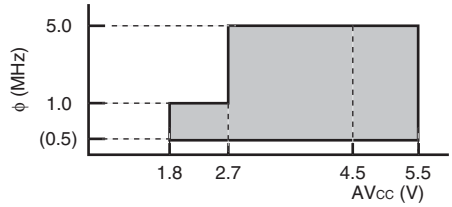
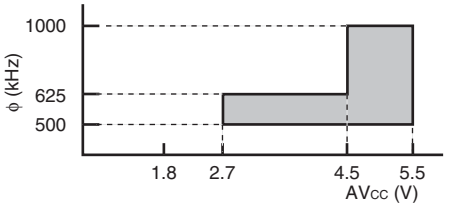


Figure 15.1 Power Supply Connection when Internal Step-Down Circuit Is Used

Analog Power Supply Voltage and A/D Converter Operating Range



• Active (high-speed) mode
• Sleep (high-speed) mode



• Active (medium-speed) mode
• Sleep (medium-speed) mode

Note: When AVcc = 1.8 V to 2.7 V, the operating range is limited to φ = 1.0 MHz when using a resonator and is φ = 0.5 MHz to 1.0 MHz when using an external clock.

17.3 Absolute Maximum Ratings of H8/38004 Group (F-ZTAT Version, Mask ROM Version), H8/38002S Group (Mask ROM Version)

Table 17.7 lists the absolute maximum ratings.

Table 17.7 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +4.3	V	*1
Analog power supply voltage		AV_{CC}	–0.3 to +4.3	V	
Input voltage	Other than port B	V_{in}	–0.3 to V_{CC} +0.3	V	
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	
Port 9 pin voltage		V_{P9}	–0.3 to V_{CC} +0.3	V	
Operating temperature		T_{opr}	Regular specifications: –20 to +75*2	°C	
			Wide-range temperature specifications: –40 to +85*3		
			Bare die product: +75*4		
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

2. When the operating voltage is V_{CC} = 2.7 to 3.6 V during flash memory reading, the operating temperature ranges from –20°C to +75°C when programming or erasing the flash memory. When the operating voltage is V_{CC} = 2.2 to 3.6 V during flash memory reading, the operating temperature ranges from –20°C to +50°C when programming or erasing the flash memory.
3. The operating temperature ranges from –20°C to +75°C when programming or erasing the flash memory.
4. The current-carrying temperature ranges from –20°C to +75°C.

Table A.1 Instruction Set

Mnemonic		Operand Size	Addressing Modes/Instruction Length (bytes)									Operation	Condition Code						Number of Execution States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	—		I	H	N	Z	V	C	
MOV	MOV.B #xx:8, Rd	B	2									#xx:8→Rd8	—	↕	↕	↕	0	—	2
	MOV.B Rs, Rd	B		2								Rs8→Rd8	—	↕	↕	↕	0	—	2
	MOV.B @Rs, Rd	B			2							@Rs16→Rd8	—	↕	↕	↕	0	—	4
	MOV.B @(d:16, Rs), Rd	B				4						@(d:16, Rs16)→Rd8	—	↕	↕	↕	0	—	6
	MOV.B @Rs+, Rd	B					2					@Rs16→Rd8 Rs16+1→Rs16	—	↕	↕	↕	0	—	6
	MOV.B @aa:8, Rd	B						2				@aa:8→Rd8	—	↕	↕	↕	0	—	4
	MOV.B @aa:16, Rd	B						4				@aa:16→Rd8	—	↕	↕	↕	0	—	6
	MOV.B Rs, @Rd	B		2								Rs8→@Rd16	—	↕	↕	↕	0	—	4
	MOV.B Rs, @(d:16, Rd)	B				4						Rs8→@(d:16, Rd16)	—	↕	↕	↕	0	—	6
	MOV.B Rs, @-Rd	B					2					Rd16-1→Rd16 Rs8→@Rd16	—	↕	↕	↕	0	—	6
	MOV.B Rs, @aa:8	B						2				Rs8→@aa:8	—	↕	↕	↕	0	—	4
	MOV.B Rs, @aa:16	B						4				Rs8→@aa:16	—	↕	↕	↕	0	—	6
	MOV.W #xx:16, Rd	W	4									#xx:16→Rd	—	↕	↕	↕	0	—	4
	MOV.W Rs, Rd	W		2								Rs16→Rd16	—	↕	↕	↕	0	—	2
	MOV.W @Rs, Rd	W			2							@Rs16→Rd16	—	↕	↕	↕	0	—	4
	MOV.W @(d:16, Rs), Rd	W				4						@(d:16, Rs16)→Rd16	—	↕	↕	↕	0	—	6
	MOV.W @Rs+, Rd	W					2					@Rs16→Rd16 Rs16+2→Rs16	—	↕	↕	↕	0	—	6
	MOV.W @aa:16, Rd	W						4				@aa:16→Rd16	—	↕	↕	↕	0	—	6
	MOV.W Rs, @Rd	W			2							Rs16→@Rd16	—	↕	↕	↕	0	—	4
	MOV.W Rs, @(d:16, Rd)	W				4						Rs16→@(d:16, Rd16)	—	↕	↕	↕	0	—	6

Item	Page	Revisions (See Manual for Details)
17.2.2 DC Characteristics Table 17.2 DC Characteristics (1)	377	Table amended

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ0}$, AEVL, AEVH, SCK32	V_{CC} = 4.0 V to 5.5 V	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
			Other than above	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$		
		$\overline{IRQ1}$	V_{CC} = 4.0 V to 5.5 V	$V_{CC} \times 0.8$	—	$AV_{CC} + 0.3$	V	
			Other than above	$V_{CC} \times 0.9$	—	$AV_{CC} + 0.3$		

17.4.2 DC Characteristics Table 17.8 DC Characteristics	395	Table amended

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ0}$, AEVL, AEVH, SCK32		$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
		$\overline{IRQ1}$		$V_{CC} \times 0.9$	—	AV_{CC} + 0.3	V	

398 Table amended

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Active mode current consumption	I_{OPE2}	V_{CC}	Active (medium-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz, ϕ_{OSC}/128	—	0.2	—	mA	*1*3*4 Approx. max. value = 1.1 × Typ.
				—	0.7	1.3		*2*3*4 Condition B

399 Table amepnded

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 1.8 V, LCD on 32-kHz External Clock ($\phi_{SUB} = \phi_W/2$)	—	6.2	—	µA	*1*3*4 Reference value
			V_{CC} = 1.8 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	5.4	—		
			V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	4.4	—		*1*3*4 Reference value
				—	8.0	—		*2*3*4 Reference value