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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38004fp10wv

2.7.2 On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states or three states. The data bus width is 8 bits, so access is by byte size only. This means that for accessing word data, two instructions must be used. For details on the data bus width and number of access states of each register, refer to section 16.1, Register Addresses (Address Order).

Two-State Access to On-Chip Peripheral Modules:

Figure 2.13 shows the operation timing in the case of two-state access to an on-chip peripheral module.

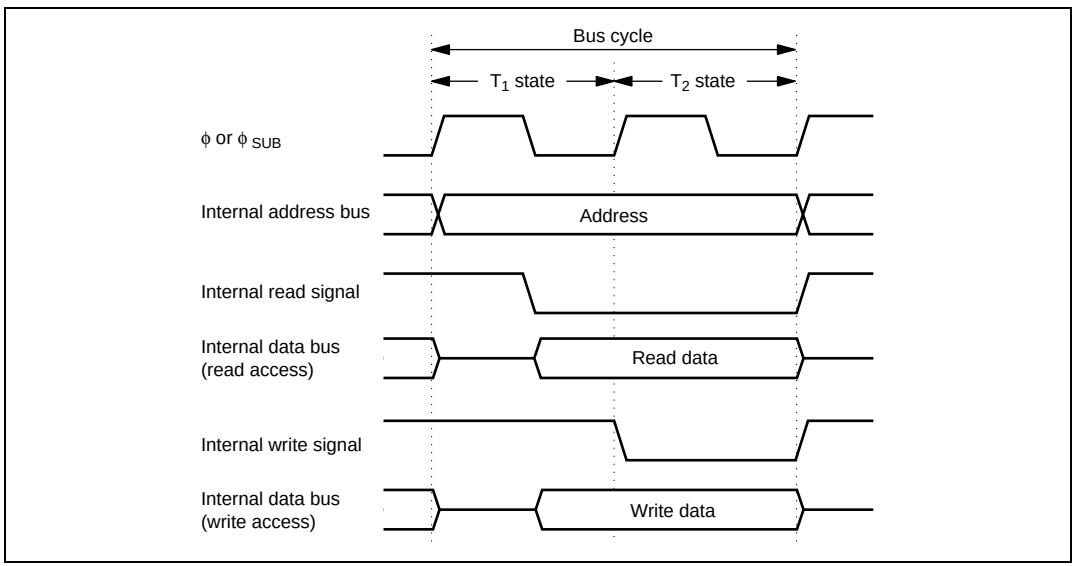
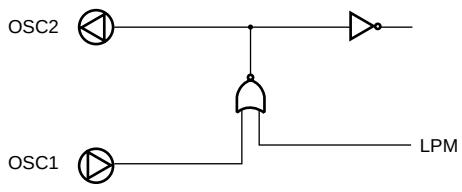


Figure 2.13 On-Chip Peripheral Module Access Cycle (2-State Access)

4.3 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic resonator, or by providing external clock input. Figure 4.3 shows a block diagram of the system clock generator.

As shown in figure 4.2, the H8/38104 Group supports selection between a system clock oscillator and an on-chip oscillator. See section 4.3.4, on-chip oscillator selection method, for information on selecting the on-chip oscillator.

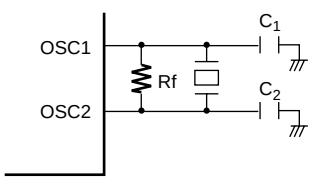


Note: LPM: Power-down mode (standby mode, subactive mode, subsleep mode, watch mode)

Figure 4.3 Block Diagram of System Clock Generator

4.3.1 Connecting Crystal Resonator

Figure 4.4(1) shows a typical method of connecting a crystal oscillator to the H8/3802 Group, and figure 4.4(2) shows a typical method of connecting a crystal oscillator to the H8/38004, H8/38104 and H8/38002S Group. Figure 4.5 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 4.1 should be used.



Frequency	Manufacturer	C1, C2 Recommendation Value
4.19 MHz	NIHON DEMPA KOGYO CO., LTD.	12 pF ±20%

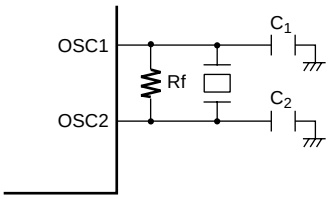
$C_1 = C_2 = 12$ pF ±20%
Rf = 1 MΩ ±20%

Note: Consult with the crystal resonator manufacturer to determine the circuit constants.

Figure 4.4(1) Typical Connection to Crystal Resonator (H8/3802 Group)

4.3.2 Connecting Ceramic Resonator

Figure 4.6(1) shows a typical method of connecting a ceramic oscillator to the H8/3802 Group, and figure 4.6(2) shows a typical method of connecting a crystal oscillator to the H8/38004, H8/38002S and H8/38104 Group.

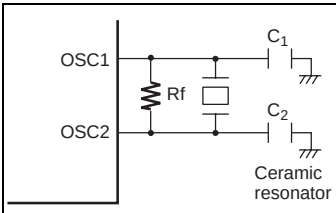


Frequency	Manufacturer	C1, C2 Recommendation Value
4.0 MHz	Murata Manufacturing Co., Ltd.	30 pF ±10%

$C_1 = C_2$ = 30 pF ±10%
Rf = 1 MΩ ±20%

Note: Consult with the ceramic resonator manufacturer to determine the circuit constants.

Figure 4.6(1) Typical Connection to Ceramic Resonator (H8/3802 Group)



Frequency	Manufacturer	Prodoct Name	C1, C2 Recommendation Value
2.0 MHz	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0	15 pF ±20%
		CSTCC2M00G56-B0	47 pF ±20%
10.0 MHz		CSTLS10M0G53-B0	15 pF ±20%
		CSTLS10M0G56-B0	47 pF ±20%
16.0 MHz*1		CSTLS16M0X53-B0	15 pF ±20%
20.0 MHz*2		CSTLS20M0X53-B0	15 pF ±20%

Rf = 1 MΩ ±20%

Notes: Consult with the crystal resonator manufacturer to determine the circuit constants.
1. This does not apply to the H8/38004 and H8/38002S Group.
2. H8/38104 Group only.

Figure 4.6(2) Typical Connection to Ceramic Resonator (H8/38004, H8/38002S, H8/38104 Group)

5.1.3 Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2)

CKSTPR1 and CKSTPR2 allow the on-chip peripheral modules to enter a standby state in module units.

- CKSTPR1

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved
5	S32CKSTP	1	R/W	SCI Module Standby SCI3 enters standby mode when this bit is cleared to 0.*1
4	ADCKSTP	1	R/W	A/D Converter Module Standby A/D converter enters standby mode when this bit is cleared to 0.
3	—	1	—	Reserved
2	TFCKSTP	1	R/W	Timer F Module Standby Timer F enters standby mode when this bit is cleared to 0.
1	—	1	—	Reserved
0	TACKSTP	1	R/W	Timer A Module Standby*2 Timer A enters standby mode when this bit is cleared to 0.

2. When external input signals cannot be captured because internal clock stops

   The case of falling edge capture is shown in figure 5.3.

   As shown in the case marked "Capture not possible," when an external input signal falls immediately after a transition to active (high-speed or medium-speed) mode or subactive mode, after oscillation is started by an interrupt via a different signal, the external input signal cannot be captured if the high-level width at that point is less than 2 t_{cyc} or 2 t_{subcyc}.

3. Recommended timing of external input signals

   To ensure dependable capture of an external input signal, high- and low-level signal widths of at least 2 t_{cyc} or 2 t_{subcyc} are necessary before a transition is made to standby mode or watch mode, as shown in "Capture possible: case 1."

   External input signal capture is also possible with the timing shown in "Capture possible: case 2" and "Capture possible: case 3," in which a 2 t_{cyc} or 2 t_{subcyc} level width is secured.

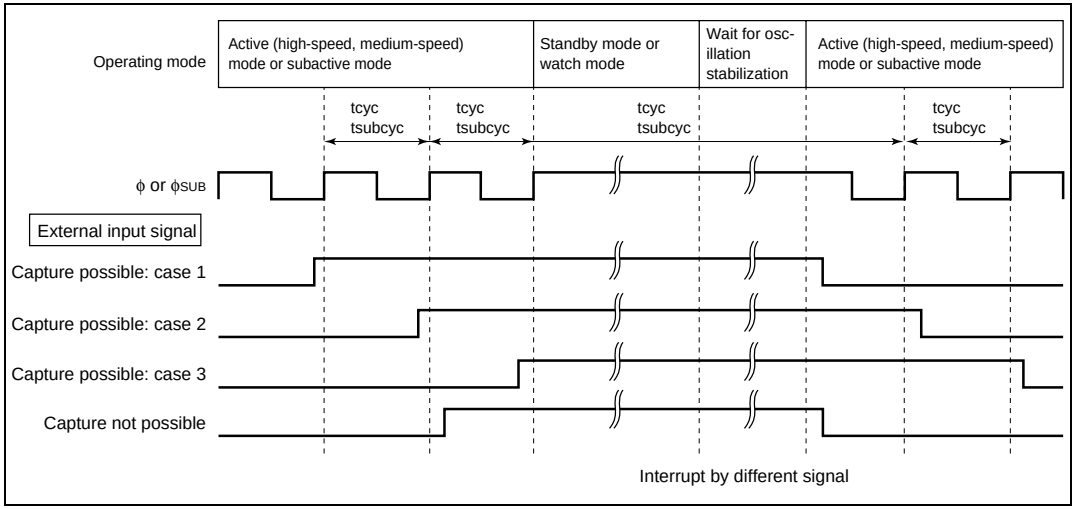


Figure 5.3 External Input Signal Capture when Signal Changes before/after Standby Mode or Watch Mode

4. Input pins to which these notes apply:
   $\overline{IRQ1}$, $\overline{IRQ0}$, $\overline{WKP7}$ to $\overline{WKP0}$, and IRQAEC

8.1.3 Port Pull-Up Control Register 3 (PUCR3)

PUCR3 controls whether the pull-up MOS of each of the port 3 pins is on or off.

Bit	Bit Name	Initial Value	R/W	Description
7	PUCR37	0	R/W	When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.
6	PUCR36	0	R/W	
5	PUCR35	0	R/W	
4	PUCR34	0	R/W	
3	PUCR33	0	R/W	
2	PUCR32	0	R/W	
1	PUCR31	0	R/W	
0	—	—	W	Reserved The write value should always be 0.

Event Counter PWM Data Register H (ECPWDRH): ECPWDRH controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRH7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRH6	0	W	
5	ECPWDRH5	0	W	
4	ECPWDRH4	0	W	
3	ECPWDRH3	0	W	
2	ECPWDRH2	0	W	
1	ECPWDRH1	0	W	
0	ECPWDRH0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRH should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRH.

Event Counter PWM Data Register L (ECPWDRL): ECPWDRL controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRL7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRL6	0	W	
5	ECPWDRL5	0	W	
4	ECPWDRL4	0	W	
3	ECPWDRL3	0	W	
2	ECPWDRL2	0	W	
1	ECPWDRL1	0	W	
0	ECPWDRL0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRL should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRL.

Event Counter Control/Status Register (ECCSR): ECCSR controls counter overflow detection, counter clear resetting, and the count-up function.

Bit	Bit Name	Initial Value	R/W	Description
7	OVH	0	R/W*	Counter Overflow H This is a status flag indicating that ECH has overflowed. [Setting condition] When ECH overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVH = 1
6	OVL	0	R/W*	Counter Overflow L This is a status flag indicating that ECL has overflowed. [Setting condition] When ECL overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVL = 1
5	—	0	R/W	Reserved This bit can be read from or written to. However, the initial value should not be changed.
4	CH2	0	R/W	Channel Select Selects how ECH and ECL event counters are used 0: ECH and ECL are used together as a single-channel 16-bit event counter 1: ECH and ECL are used as two-channel 8-bit event counter
3	CUEH	0	R/W	Count-Up Enable H Enables event clock input to ECH. 0: ECH event clock input is disabled (ECH value is retained) 1: ECH event clock input is enabled
2	CUEL	0	R/W	Count-Up Enable L Enables event clock input to ECL. 0: ECL event clock input is disabled (ECL value is retained) 1: ECL event clock input is enabled

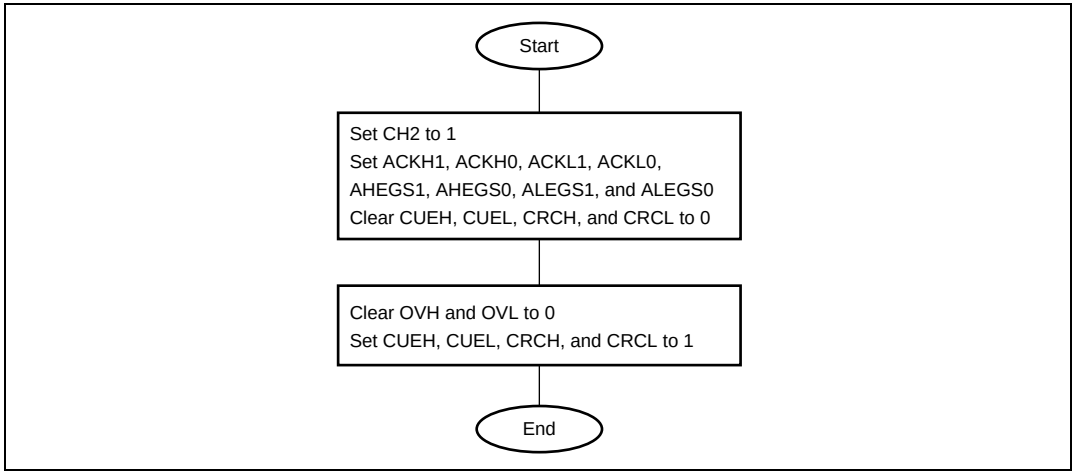


Figure 9.9 Example of Software Processing when Using ECH and ECL as 8-Bit Event Counters

ECH and ECL can be used as 8-bit event counters by carrying out the software processing shown in the example in figure 9.9. When the next clock is input after the ECH count value reaches H'FF, ECH overflows, the OVH flag is set to 1 in ECCSR, the ECH count value returns to H'00, and counting up is restarted. Similarly, when the next clock is input after the ECL count value reaches H'FF, ECL overflows, the OVL flag is set to 1 in ECCSR, the ECL count value returns to H'00, and counting up is restarted. When an overflow occurs, the IRREC bit is set to 1 in IRR2. If the IENEC bit in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

IRQAEC Operation: When ECPWME in AEGSR is 0, the ECH and ECL input clocks are enabled only when IRQAEC is high. When IRQAEC is low, the input clocks are not input to the counters, and so ECH and ECL do not count. ECH and ECL count operations can therefore be controlled from outside by controlling IRQAEC. In this case, ECH and ECL cannot be controlled individually.

IRQAEC can also operate as an interrupt source. In this case the vector number is 6 and the vector addresses are H'000C and H'000D.

Interrupt enabling is controlled by IENEC2 in IENR1. When an IRQAEC interrupt is generated, IRR1 interrupt request flag IRREC2 is set to 1. If IENEC2 in IENR1 is set to 1 at this time, an interrupt request is sent to the CPU.

Rising, falling, or both edge sensing can be selected for the IRQAEC input pin with bits AIAGS1 and AIAGS0 in AEGSR.

Bit	Bit Name	Initial Value	R/W	Description
0	WRST	0	R/(W)*1	Watchdog Timer Reset [Setting condition] When TCW overflows and an internal reset signal is generated [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit while writing 0 to the B0WI bit when the TCSRWE bit = 1

Notes: 1. These bits can be written only when the writing conditions are satisfied.
2. Initial value 0 on H8/38004, H8/38002S Group and 1 on H8/38104 Group.
3. On reset, cleared to 0 on H8/38004, H8/38002S Group and set to 1 on H8/38104 Group.

Timer Counter W (TCW): TCW is an 8-bit readable/writable up-counter. When TCW overflows from H'FF to H'00, the internal reset signal is generated and the WRST bit in TCSRW is set to 1. TCW is initialized to H'00.

Timer Mode Register W (TMW): TMW selects the input clock. Clock source selection using this register is enabled when WDCKS in port mode register 2 (PMR2) is cleared to 0. If WDCKS is set to 1, $\phi w/32$ is selected as the clock source, regardless of the setting of TMW.

Note: TMW is implemented on H8/38104 Group only.

10.2 Input/Output Pins

Table 10.1 shows the SCI3 pin configuration.

Table 10.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
SCI3 clock	SCK32	I/O	SCI3 clock input/output
SCI3 receive data input	RXD32	Input	SCI3 receive data input
SCI3 transmit data output	TXD32	Output	SCI3 transmit data output

10.3 Register Descriptions

The SCI3 has the following registers.

- Receive shift register (RSR)
- Receive data register (RDR)
- Transmit shift register (TSR)
- Transmit data register (TDR)
- Serial mode register (SMR)
- Serial control register 3 (SCR3)
- Serial status register (SSR)
- Bit rate register (BRR)
- Serial port control register (SPCR)

10.3.1 Receive Shift Register (RSR)

RSR is a shift register that is used to receive serial data input from the RXD32 pin and convert it into parallel data. When one byte of data has been received, it is transferred to RDR automatically. RSR cannot be directly accessed by the CPU.

transmitter is initialized regardless of the current transmission state, the TXD32 pin becomes an I/O port, and 0 is output from the TXD32 pin.

10.7.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

10.7.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 10.16.

Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ \left(0.5 - \frac{1}{2N}\right) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

Where N : Ratio of bit rate to clock (N = 16)
D : Clock duty (D = 0.5 to 1.0)
L : Frame length (L = 9 to 12)
F : Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

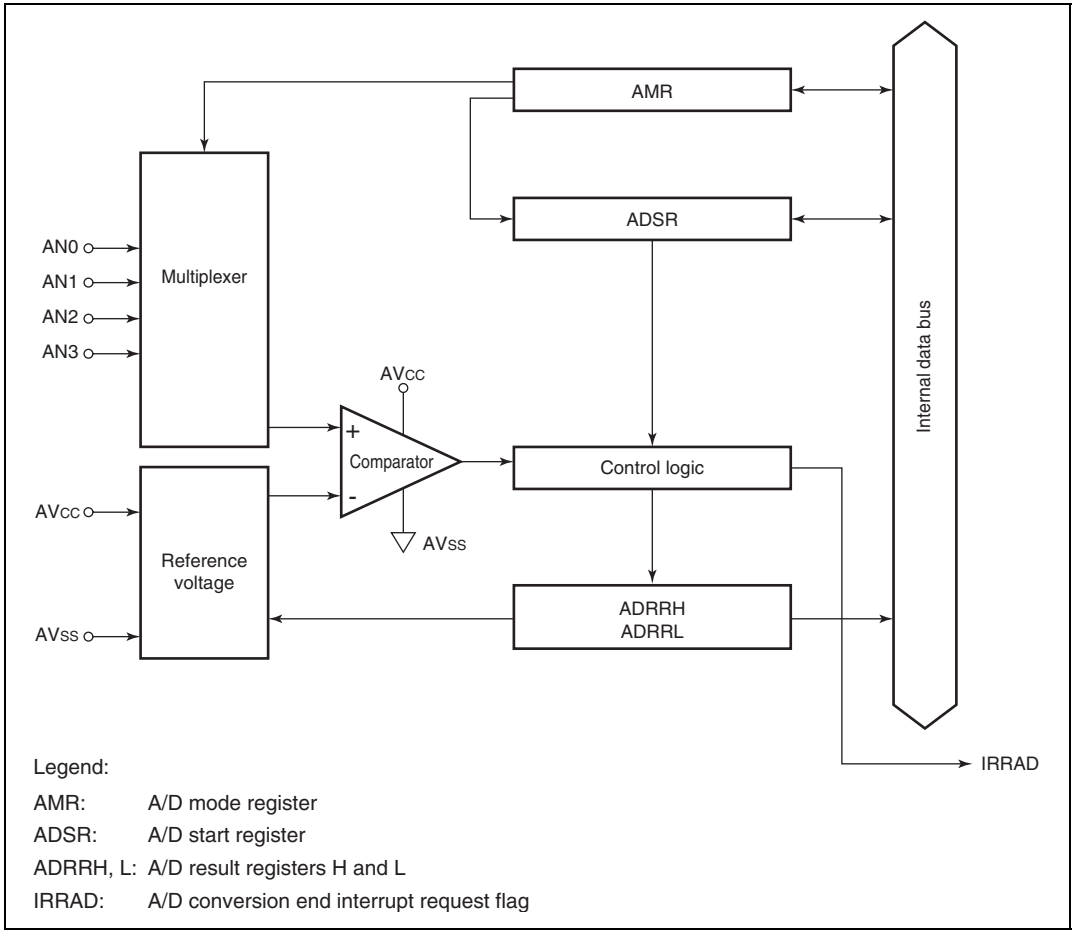


Figure 12.1 Block Diagram of A/D Converter

14.2.2 Low-Voltage Detection Status Register (LVDSR)

LVDSR is used to control external input selection, indicates when the reference voltage is stable, and indicates if the power supply voltage goes below or above a specified range.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0*	R/W	LVD Reference Voltage Stabilized Flag Setting condition: When the low-voltage detection counter (LVDCNT) overflows Clearing condition: When 0 is written after reading 1
6 to 4	—	All 0	R/W	These are read/write enabled reserved bits.
3	VREFSEL	0	R/W	Reference Voltage External Input Select 0: The on-chip circuit is used to generate the reference voltage 1: The reference voltage is input to the Vref pin from an external source
2	—	0	R/W	This bit is reserved. It is always read as 0 and cannot be written to.
1	LVDDF	0*	R/W	LVD Power Supply Voltage Drop Flag Setting condition: When the power supply voltage drops below Vint(D) Clearing condition: When 0 is written after reading 1
0	LVDUF	0*	R/W	LVD Power Supply Voltage Rise Flag Setting condition: When the power supply voltage drops below Vint(D) while the LVDUE bit in LVDCR is set to 1, and it rises above Vint(U) before dropping below Vreset1 Clearing condition: When 0 is written after reading 1

Note: * These bits are initialized by resets trigged by LVDR.

Table 17.4 Serial Interface (SCI3) Timing

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified (including subactive mode), T_a = –20°C to +75°C (product with regular specifications), T_a = –40°C to +85°C (product with wide-range temperature specifications), T_a = +75°C (bare die product)

Item		Symbol	Test Condition	Values			Unit	Reference Figure
				Min	Typ	Max		
Input clock cycle	Asynchronous	t_{scyc}		4	—	—	t_{cyc} or t_{subcyc}	Figure 17.5
	Clocked synchronous			6	—	—		
Input clock pulse width		t_{SCKW}		0.4	—	0.6	t_{scyc}	Figure 17.5
Transmit data delay time (clocked synchronous)		t_{TXD}	V_{CC} = 4.0 V to 5.5 V	—	—	1	t_{cyc} or t_{subcyc}	Figure 17.6
			Other than above	—	—	1		
Receive data setup time (clocked synchronous)		t_{RXS}	V_{CC} = 4.0 V to 5.5 V	200.0	—	—	ns	Figure 17.6
			Other than above	400.0	—	—		
Receive data hold time (clocked synchronous)		t_{RXH}	V_{CC} = 4.0 V to 5.5 V	200.0	—	—	ns	Figure 17.6
			Other than above	400.0	—	—		

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Reference Figure
Input pin high width	t_{IH}	$\overline{IRQ0}$, $\overline{IRQ1}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$,		2	—	—	t_{cyc} t_{subcyc}	Figure 17.4
		AEVL, AEVH		0.5	—	—	t_{OSC}	
Input pin low width	t_{IL}	$\overline{IRQ0}$, $\overline{IRQ1}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$,		2	—	—	t_{cyc} t_{subcyc}	Figure 17.4
		AEVL, AEVH		0.5	—	—	t_{OSC}	

Notes: 1. Determined by the SA1 and SA0 bits in the system control register 2 (SYSCR2).
2. These characteristics are given as ranges between minimum and maximum values in order to account for factors such as temperature, power supply voltage, and variation among production lots. When designing systems, make sure to give due consideration to the SPEC range. Please see the Web site for this product for actual performance data.

Table 17.18 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item		Symbol	Test Condition	Values Min	Typ	Max	Unit	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}		4	—	—	t_{cyc} or t_{subcyc}	Figure 17.5
	Clocked synchronous			6	—	—		
Input clock pulse width		t_{SCKW}		0.4	—	0.6	t_{scyc}	Figure 17.5
Transmit data delay time (clocked synchronous)		t_{TXD}		—	—	1	t_{cyc} or t_{subcyc}	Figure 17.6
Receive data setup time (clocked synchronous)		t_{RXS}		150.0	—	—	ns	Figure 17.6
Receive data hold time (clocked synchronous)		t_{RXH}		150.0	—	—	ns	Figure 17.6

Table D.2 Product Code Lineup of H8/38004 Group

Product Type			Part No.	Model Marking	Package (Package Code)
H8/38004	Flash memory version	Regular product (2.7 V)	HD64F38004H10	64F38004H10	64-pin QFP (FP-64A)
			HD64F38004FP10	F38004FP10	64-pin LQFP (FP-64E)
			HD64F38004FT10	F38004FT10	64-pin QFP (TNP-64B)
			HCD64F38004	—	Die
		Regular product (2.2 V)	HD64F38004H4	64F38004H4	64-pin QFP (FP-64A)
			HD64F38004FP4	F38004FP4	64-pin LQFP (FP-64E)
			HD64F38004FT4	F38004FT4	64-pin QFP (TNP-64B)
			HCD64F38004C4	—	Die
		Product with wide-range temperature specifications (2.7 V)	HD64F38004H10W	64F38004H10	64-pin QFP (FP-64A)
			HD64F38004FP10W	F38004FP10	64-pin LQFP (FP-64E)
			HD64F38004FT10W	F38004FT10	64-pin QFP (TNP-64B)
	Mask ROM version	Regular product	HD64338004H	HD64338004H	64-pin QFP (FP-64A)
			HD64338004FP	38004 (***) FP	64-pin LQFP (FP-64E)
			HD64338004FT	38004 (***) FT	64-pin QFP (TNP-64B)
			HCD64338004	—	Die
		Product with wide-range temperature specifications	HD64338004HW	HD64338004H	64-pin QFP (FP-64A)
			HD64338004FPW	38004 (***) FP	64-pin LQFP (FP-64E)
			HD64338004FTW	38004 (***) FT	64-pin QFP (TNP-64B)
H8/38003	Mask ROM version	Regular product	HD64338003H	HD64338003H	64-pin QFP (FP-64A)
			HD64338003FP	38003 (***) FP	64-pin LQFP (FP-64E)
			HD64338003FT	38003 (***) FT	64-pin QFP (TNP-64B)
			HCD64338003	—	Die
		Product with wide-range temperature specifications	HD64338003HW	HD64338003H	64-pin QFP (FP-64A)
			HD64338003FPW	38003 (***) FP	64-pin LQFP (FP-64E)
			HD64338003FTW	38003 (***) FT	64-pin QFP (TNP-64B)

Table D.3 Product Code Lineup of H8/38002S Group

Product Type			Part No.	Model Marking	Package (Package Code)
H8/38002S	Mask ROM version	Regular product	HD64338002SH	38002 (***) H	64-pin QFP (FP-64A)
			HD64338002SFZ	38002 (***)	64-pin LQFP (FP-64K)
			HD64338002SFT	38002 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338002SHW	38002 (***) H	64-pin QFP (FP-64A)
			HD64338002SFZW	38002 (***)	64-pin LQFP (FP-64K)
			HD64338002SFTW	38002 (***) FT	64-pin QFP (TNP-64B)
H8/38001S	Mask ROM version	Regular product	HD64338001SH	38001 (***) H	64-pin QFP (FP-64A)
			HD64338001SFZ	38001 (***)	64-pin LQFP (FP-64K)
			HD64338001SFT	38001 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338001SHW	38001 (***) H	64-pin QFP (FP-64A)
			HD64338001SFZW	38001 (***)	64-pin LQFP (FP-64K)
			HD64338001SFTW	38001 (***) FT	64-pin QFP (TNP-64B)
H8/38000S	Mask ROM version	Regular product	HD64338000SH	38000 (***) H	64-pin QFP (FP-64A)
			HD64338000SFZ	38000 (***)	64-pin LQFP (FP-64K)
			HD64338000SFT	38000 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338000SHW	38000 (***) H	64-pin QFP (FP-64A)
			HD64338000SFZW	38000 (***)	64-pin LQFP (FP-64K)
			HD64338000SFTW	38000 (***) FT	64-pin QFP (TNP-64B)

Legend:

(***): ROM code

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Hardware Manual
H8/3802, H8/38004, H8/38002S, H8/38104 Group

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