Renesas Electronics America Inc - DF38004FP4V Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38004fp4v

Configuration of This Manual

This manual comprises the following items:

1. General Precautions in the Handling of MPU/MCU Products
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

     The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions for This Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

Appendices

2.2 Address Space and Memory Map

The address space of this LSI is 64 kbytes, which includes the program area and the data area. Figures 2.1 show the memory map.

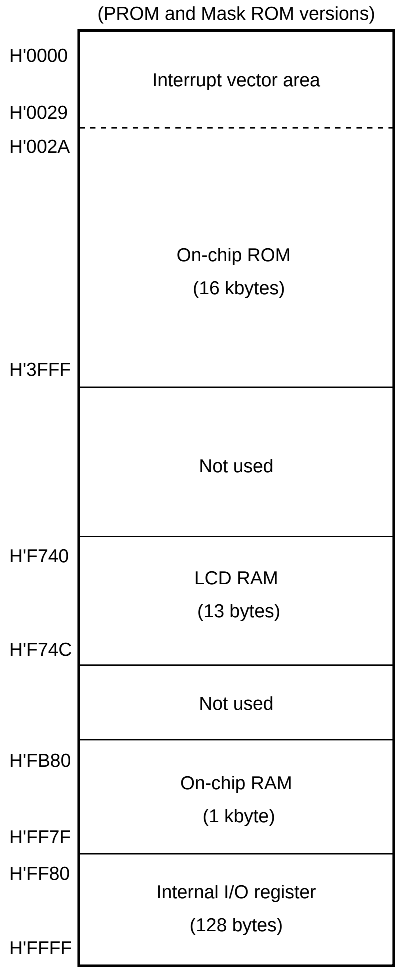


Figure 2.1(1) H8/3802 Memory Map

Immediate—#xx:8/#xx:16

The instruction contains an 8-bit operand (#xx:8) in its second byte, or a 16-bit operand (#xx:16) in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data in the second or fourth byte of the instruction, specifying a bit number.

Program-Counter Relative—@(d:8, PC)

This mode is used in the Bcc and BSR instructions. An 8-bit displacement in byte 2 of the instruction code is sign-extended to 16 bits and added to the program counter contents to generate a branch destination address. The possible branching range is –126 to +128 bytes (–63 to +64 words) from the current address. The displacement should be an even number.

Memory Indirect—@@aa:8

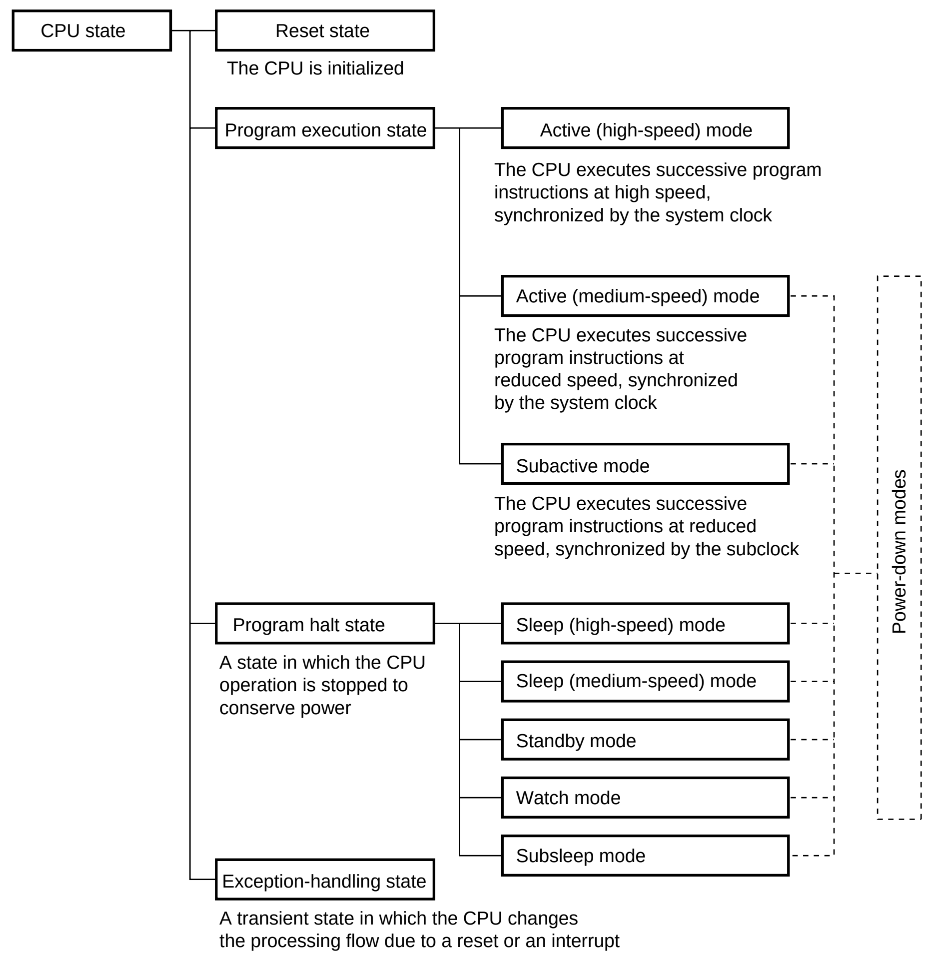
This mode can be used by the JMP and JSR instructions. The second byte of the instruction code specifies an 8-bit absolute address. The word located at this address contains the branch destination address. The upper 8 bits of the absolute address are assumed to be 0 (H'00), so the address range is from H'0000 to H'00FF (0 to 255). Note that with the H8/300L Series, the lower end of the address area is also used as a vector area. See section 3.1, Exception Sources and Vector Address, for details on the vector area.

If an odd address is specified as a branch destination or as the operand address of a MOV.W instruction, the least significant bit is regarded as 0, causing word access to be performed at the address preceding the specified address. See section 2.4.2, Memory Data Formats, for further information.

2.8 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active (high-speed or medium-speed) mode and subactive mode. In the program halt state, there are a sleep (high-speed or medium-speed) mode, standby mode, watch mode, and sub-sleep mode.

These states are shown in figure 2.15. Figure 2.16 shows the state transitions.



Note: See section 5, Power-Down Modes, for details on the modes and their transitions.

Figure 2.15 CPU Operation States

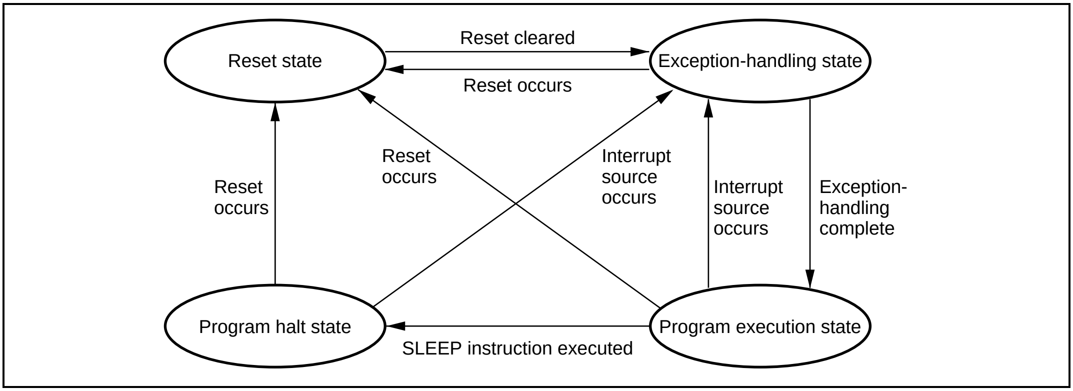


Figure 2.16 State Transitions

2.9 Usage Notes

2.9.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.9.2 Access to Internal I/O Registers

Internal data transfer to or from on-chip peripheral modules other than the on-chip ROM and RAM areas makes use of an 8-bit data width. If word access is attempted to these areas, the following results will occur.

Word access from CPU to I/O register area:

Upper byte: Will be written to I/O register.

Lower byte: Transferred data will be lost.

Word access from I/O register to CPU:

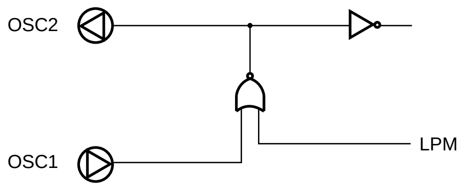
Upper byte: Will be written to upper part of CPU register.

Lower byte: Data which is written to lower part of CPU register is not guaranteed.

4.3 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic resonator, or by providing external clock input. Figure 4.3 shows a block diagram of the system clock generator.

As shown in figure 4.2, the H8/38104 Group supports selection between a system clock oscillator and an on-chip oscillator. See section 4.3.4, on-chip oscillator selection method, for information on selecting the on-chip oscillator.

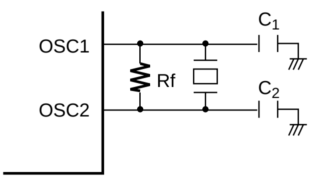


Note: LPM: Power-down mode (standby mode, subactive mode, subsleep mode, watch mode)

Figure 4.3 Block Diagram of System Clock Generator

4.3.1 Connecting Crystal Resonator

Figure 4.4(1) shows a typical method of connecting a crystal oscillator to the H8/3802 Group, and figure 4.4(2) shows a typical method of connecting a crystal oscillator to the H8/38004, H8/38104 and H8/38002S Group. Figure 4.5 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 4.1 should be used.

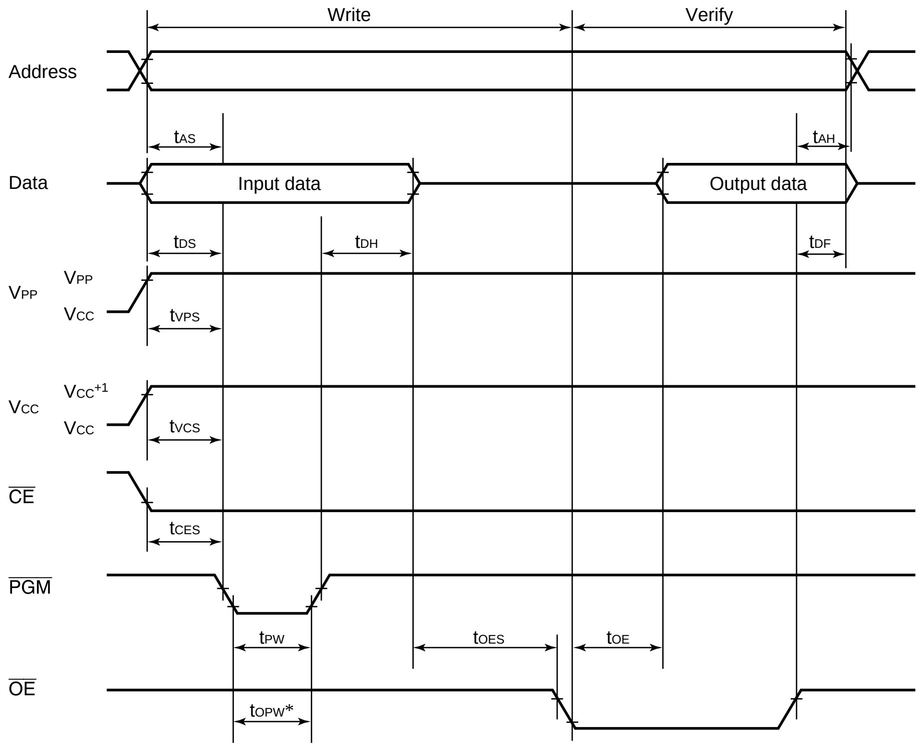


Frequency	Manufacturer	C1, C2 Recommendation Value
4.19 MHz	NIHON DEMPA KOGYO CO., LTD.	12 pF ±20%

$C_1 = C_2 = 12$ pF ±20%
Rf = 1 MΩ ±20%

Note: Consult with the crystal resonator manufacturer to determine the circuit constants.

Figure 4.4(1) Typical Connection to Crystal Resonator (H8/3802 Group)



Note: * tOPW is defined by the value shown in figure 6.4, High-Speed, High-Reliability Programming Flowchart.

Figure 6.5 PROM Write/Verify Timing

6.3.2 Programming Precautions

- Use the specified programming voltage and timing.

  The programming voltage in PROM mode (Vpp) is 12.5 V. Use of a higher voltage can permanently damage the chip. Be especially careful with respect to PROM programmer overshoot.

  Setting the PROM programmer to Renesas specifications for the HN27C101 will result in correct Vpp of 12.5 V.
- Make sure the index marks on the PROM programmer socket, socket adapter, and chip are properly aligned. If they are not, the chip may be destroyed by excessive current flow. Before programming, be sure that the chip is properly mounted in the PROM programmer.
- Avoid touching the socket adapter or chip while programming, since this may cause contact faults and write errors.

6.5.3 Block Configuration

Figure 6.8 shows the block configuration of 32-kbyte flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The 32-kbyte flash memory is divided into 1 kbyte × 4 blocks and 28 kbytes × 1 block. Erasing is performed in these units. The 16-kbyte flash memory is divided into 1 kbyte × 4 blocks and 12 kbytes × 1 block. Programming is performed in 128-byte units starting from an address with lower eight bits H'00 or H'80.

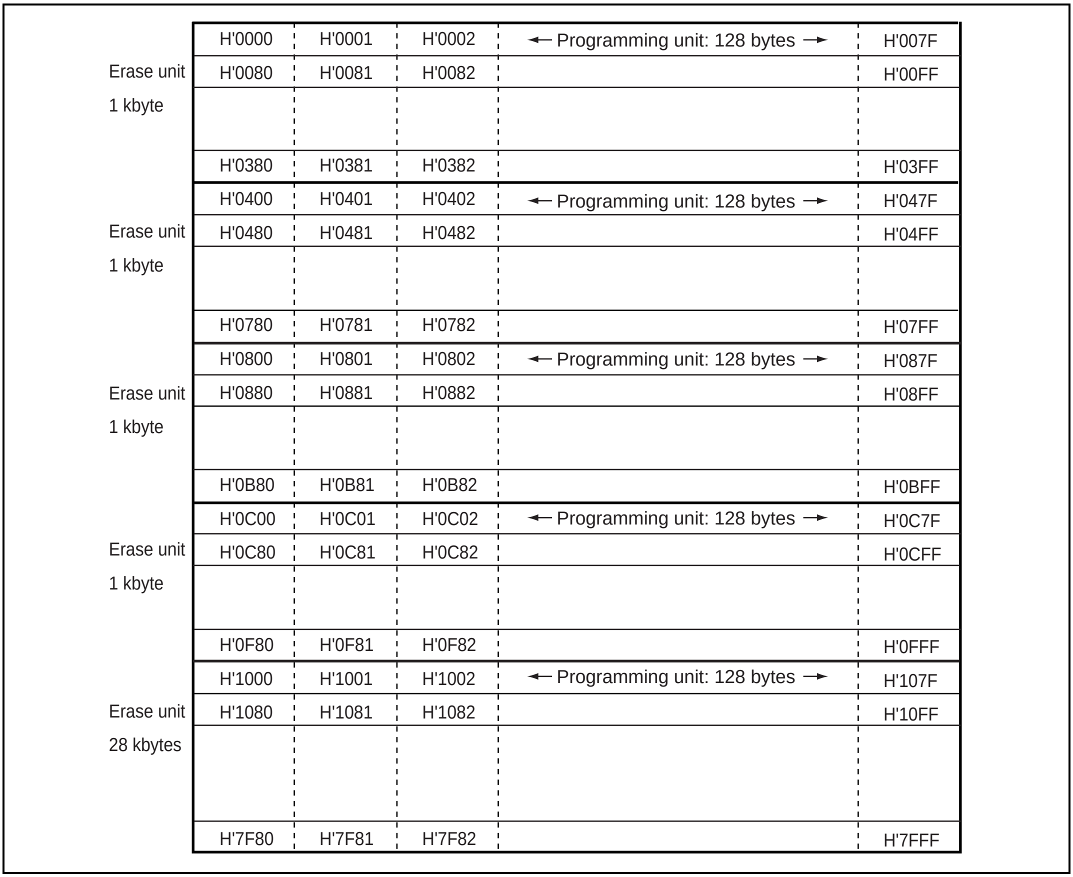


Figure 6.8(1) Block Configuration of 32-kbyte Flash Memory

6.10.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

Table 6.20 Stipulated Transition Times to Command Wait State

Item	Symbol	Min	Max	Unit	Test Condition
Oscillation stabilization time (crystal resonator)	t_{osc1}	10	—	ms	Figure 6.20
Oscillation stabilization time (ceramic resonator)		5	—	ms	
Programmer mode setup time	t_{bmv}	10	—	ms	
V_{CC} hold time	t_{dwn}	0	—	ms	

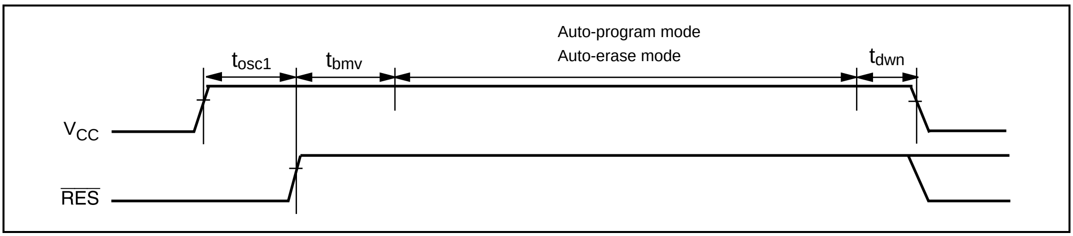


Figure 6.20 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence

6.10.9 Notes on Memory Programming

1. When performing programming using programmer mode on a chip that has been programmed/erased in on-board programming mode, auto-erasing is recommended before carrying out auto-programming.
2. The flash memory is initially in the erased state when the device is shipped by Renesas. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.

10.7.6 Relation between Writing to TDR and Bit TDRE

Bit TDRE in the serial status register (SSR) is a status flag that indicates that data for serial transmission has not been prepared in TDR. When data is written to TDR, bit TDRE is cleared to 0 automatically. When the SCI3 transfers data from TDR to TSR, bit TDRE is set to 1.

Data can be written to TDR irrespective of the state of bit TDRE, but if new data is written to TDR while bit TDRE is cleared to 0, the data previously stored in TDR will be lost if it has not yet been transferred to TSR. Accordingly, to ensure that serial transmission is performed dependably, you should first check that bit TDRE is set to 1, then write the transmit data to TDR only once (not two or more times).

10.7.7 Relation between RDR Reading and bit RDRF

In a receive operation, the SCI3 continually checks the RDRF flag. If bit RDRF is cleared to 0 when reception of one frame ends, normal data reception is completed. If bit RDRF is set to 1, this indicates that an overrun error has occurred.

When the contents of RDR are read, bit RDRF is cleared to 0 automatically. Therefore, if RDR is read more than once, the second and subsequent read operations will be performed while bit RDRF is cleared to 0. Note that, when an RDR read is performed while bit RDRF is cleared to 0, if the read operation coincides with completion of reception of a frame, the next frame of data may be read. This is shown in figure 10.17.

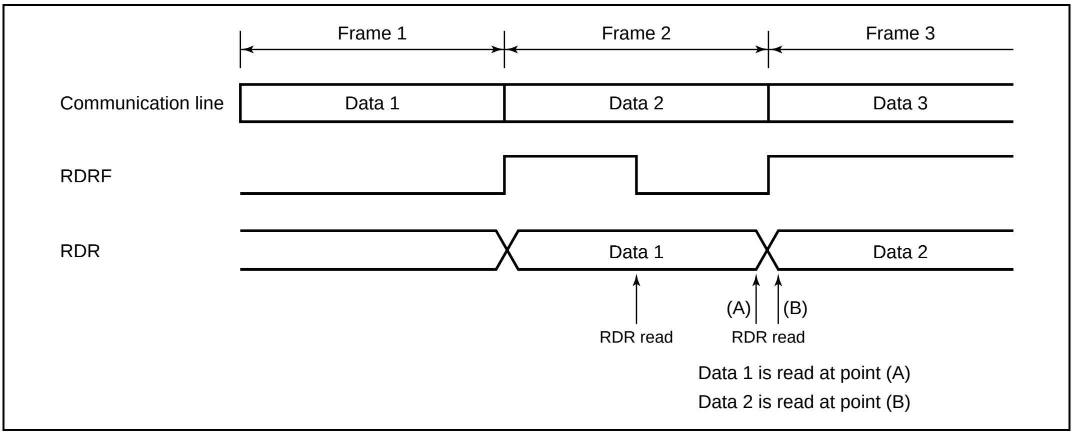


Figure 10.17 Relation between RDR Read Timing and Data

In this case, only a single RDR read operation (not two or more) should be performed after first checking that bit RDRF is set to 1. If two or more reads are performed, the data read the first time

Selects the PWCR output format and the conversion period on the H8/38104 Group.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved This bit is reserved. It is always read as 1 and cannot be written to.
2	PWCR2	0	W	Output Format Select 0: 10-bit PWM 1: Event counter PWM (PWM incorporating AEC)
1 0	PWCR1 PWCR0	0 0	W W	Clock Select 1, 0 00: The input clock is φ (tφ = 1/φ) — The conversion period is 512/φ, with a minimum modulation width of 1/2φ 01: The input clock is φ/2 (tφ = 2/φ) — The conversion period is 1,024/φ, with a minimum modulation width of 1/φ 10: The input clock is φ/4 (tφ = 4/φ) — The conversion period is 2,048/φ, with a minimum modulation width of 2/φ 11: The input clock is φ/8 (tφ = 8/φ) — The conversion period is 4,096/φ, with a minimum modulation width of 4/φ

Legend: tφ: Period of PWM clock input

15.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the CV_{cc} pin and V_{cc} pin, as shown in figure 15.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 2.7 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.

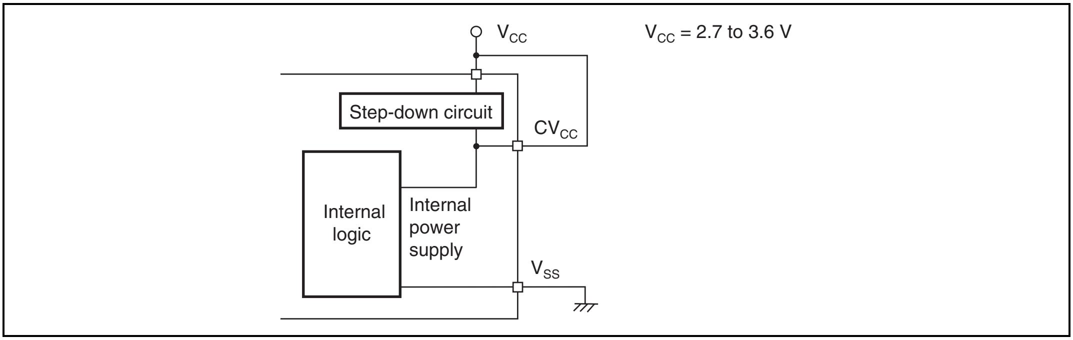


Figure 15.2 Power Supply Connection when Internal Step-Down Circuit Is Not Used

Table 17.2 DC Characteristics (4)

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified (including subactive mode), T_a = –20°C to +75°C (product with regular specifications), T_a = –40°C to +85°C (product with wide-range temperature specifications), T_a = +75°C (bare die product)

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Pull-up MOS current	$-I_p$	P31 to P37, P50 to P57, P60 to P67	V_{CC} = 5.0 V, V_{IN} = 0.0 V	50.0	—	300.0	µA	
			V_{CC} = 2.7 V, V_{IN} = 0.0 V	—	35.0	—		Reference value
Input capaci-tance	C_{in}	All input pins except power supply, $\overline{RES}$, P43, IRQAEC, PB0 to PB3 pins	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	—	—	15.0	pF	
		IRQAEC		—	—	30.0		
		$\overline{RES}$		—	—	80.0		*2
				—	—	15.0		*1
		P43		—	—	50.0		*2
				—	—	15.0		*1
		PB0 to PB3		—	—	15.0		
Active mode current consump-tion	I_{OPE1}	V_{CC}	Active (high-speed) mode V_{CC} = 5.0 V, f_{OSC} = 10 MHz	—	7.0	10.0	mA	*3 *4
	I_{OPE2}	V_{CC}	Active (medium-speed) mode V_{CC} = 5.0 V, f_{OSC} = 10 MHz, $\phi_{OSC}/128$	—	2.2	3.0	mA	*3 *4
Sleep mode current consump-tion	I_{SLEEP}	V_{CC}	V_{CC} = 5.0 V, f_{OSC} = 10 MHz	—	3.8	5.0	mA	*3 *4

17.3 Absolute Maximum Ratings of H8/38004 Group (F-ZTAT Version, Mask ROM Version), H8/38002S Group (Mask ROM Version)

Table 17.7 lists the absolute maximum ratings.

Table 17.7 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +4.3	V	*1
Analog power supply voltage		AV_{CC}	–0.3 to +4.3	V	
Input voltage	Other than port B	V_{in}	–0.3 to V_{CC} +0.3	V	
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	
Port 9 pin voltage		V_{P9}	–0.3 to V_{CC} +0.3	V	
Operating temperature		T_{opr}	Regular specifications: –20 to +75*2	°C	
			Wide-range temperature specifications: –40 to +85*3		
			Bare die product: +75*4		
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

2. When the operating voltage is V_{CC} = 2.7 to 3.6 V during flash memory reading, the operating temperature ranges from –20°C to +75°C when programming or erasing the flash memory. When the operating voltage is V_{CC} = 2.2 to 3.6 V during flash memory reading, the operating temperature ranges from –20°C to +50°C when programming or erasing the flash memory.

3. The operating temperature ranges from –20°C to +75°C when programming or erasing the flash memory.

4. The current-carrying temperature ranges from –20°C to +75°C.

Item		Symbol	Test Conditions	Values			Unit
				Min	Typ	Max	
Programming	Wait time after SWE-bit clear*1	θ		100	—	—	µs
	Maximum programming count*1*4*5	N		—	—	1000	times
Erase	Wait time after SWE-bit setting*1	x		1	—	—	µs
	Wait time after ESU-bit setting*1	y		100	—	—	µs
	Wait time after E-bit setting*1*6	z		10	—	100	ms
	Wait time after E-bit clear*1	α		10	—	—	µs
	Wait time after ESU-bit clear*1	β		10	—	—	µs
	Wait time after EV-bit setting*1	γ		20	—	—	µs
	Wait time after dummy write*1	ε		2	—	—	µs
	Wait time after EV-bit clear*1	η		4	—	—	µs
	Wait time after SWE-bit clear*1	θ		100	—	—	µs
	Maximum erase count*1*6*7	N		—	—	120	times

Notes:
1. Set the times according to the program/erase algorithms.
2. Programming time per 128 bytes (Shows the total period for which the P bit in FLMCR1 is set. It does not include the programming verification time.)
3. Block erase time (Shows the total period for which the E bit in FLMCR1 is set. It does not include the erase verification time.)
4. Maximum programming time (t_P (max))

   t_P (max) = Wait time after P-bit setting (z) • maximum number of writes (N)
5. The maximum number of writes (N) should be set according to the actual set value of z1, z2, and z3 to allow programming within the maximum programming time (t_P (max)).

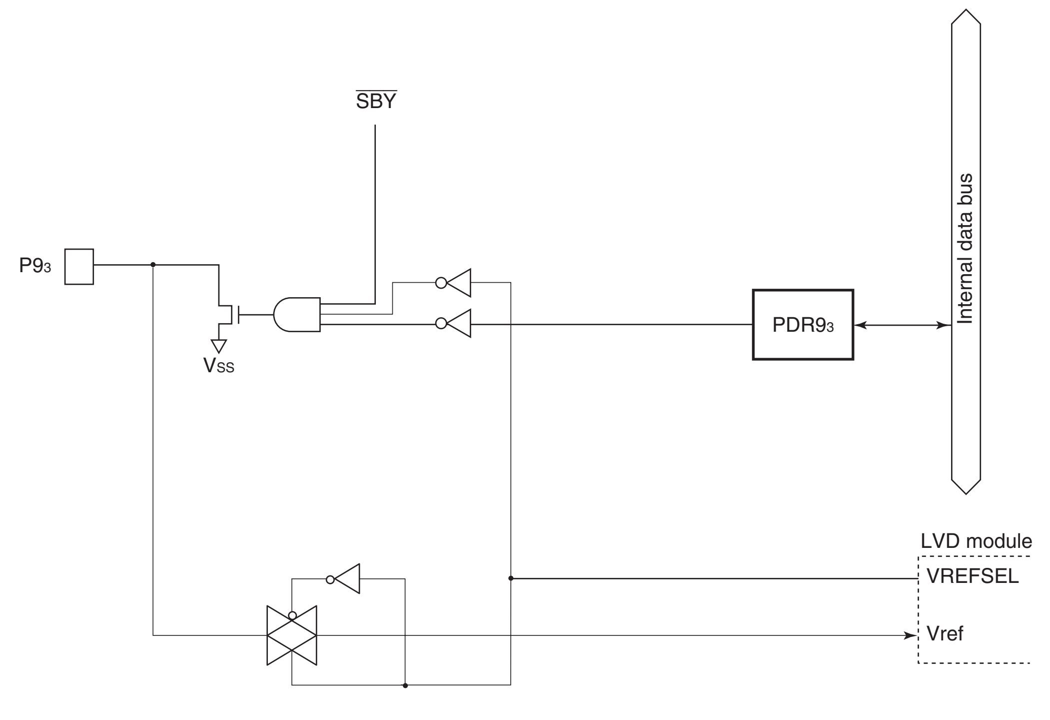
   The wait time after P-bit setting (z1 and z2) should be alternated according to the number of writes (n) as follows:

   $1 \leq n \leq 6$ z1 = 30 µs
   $7 \leq n \leq 1000$ z2 = 200 µs
6. Maximum erase time (t_E (max))

   t_E (max) = Wait time after E-bit setting (z) • maximum erase count (N)
7. The maximum number of erases (N) should be set according to the actual set value of z to allow erasing within the maximum erase time (t_E (max)).
8. This minimum value guarantees all characteristics after reprogramming (the guaranteed range is from 1 to the minimum value).

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ROTXR	ROTXR.B Rd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
SHAR	SHAR.B Rd	1					
SHLL	SHLL.B Rd	1					
SHLR	SHLR.B Rd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

Note: n: Specified value in R4L. The source and destination operands are accessed n+1 times respectively.



PDR9: Port data register 9

Figure B.7(c) Port 9 Block Diagram (Pin P93, H8/38104 Group Only)

Appendix G Bonding Pad Form

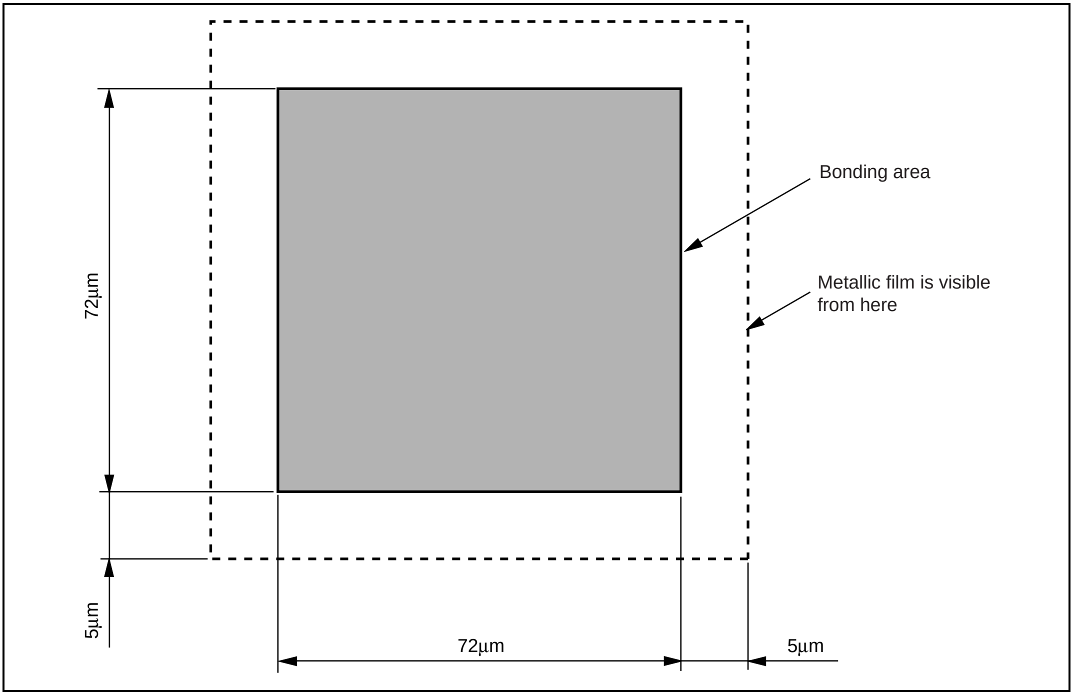


Figure G.1 Bonding Pad Form (HCD6433802, HCD6433801, HCD6433800, HCD64338004, HCD64338003, HCD64338002, HCD64338001, HCD64338000, HCD64F38004, and HCD64F38002)