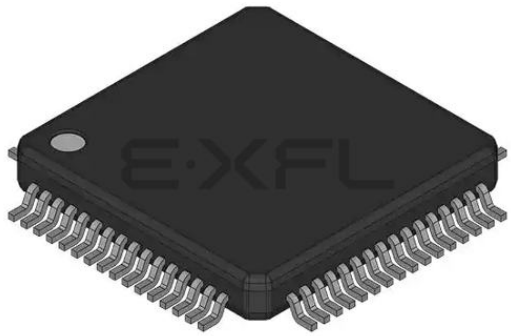

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38004h10v

Section 7 RAM

Section 8 I/O Ports

Section 9 Timers

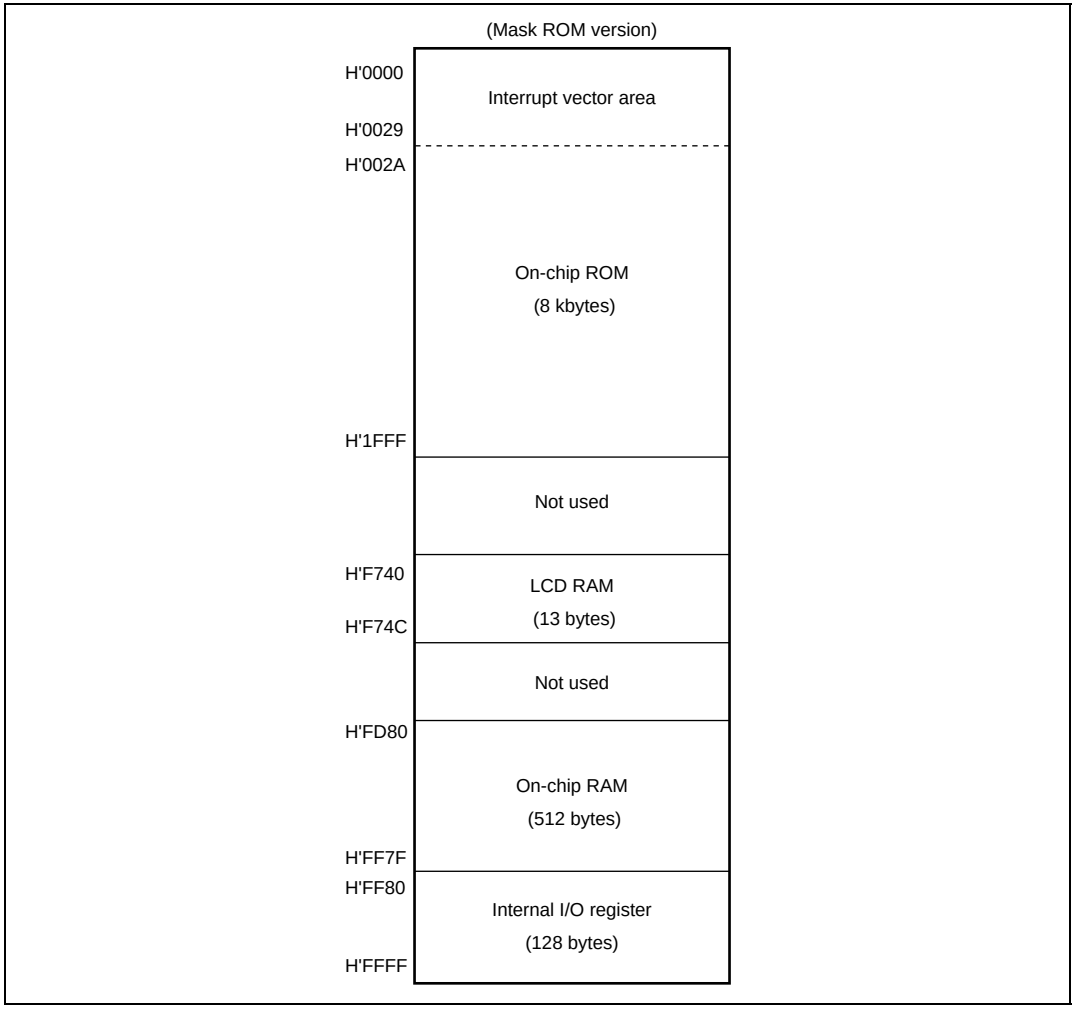


Figure 2.1(3) H8/3800 Memory Map

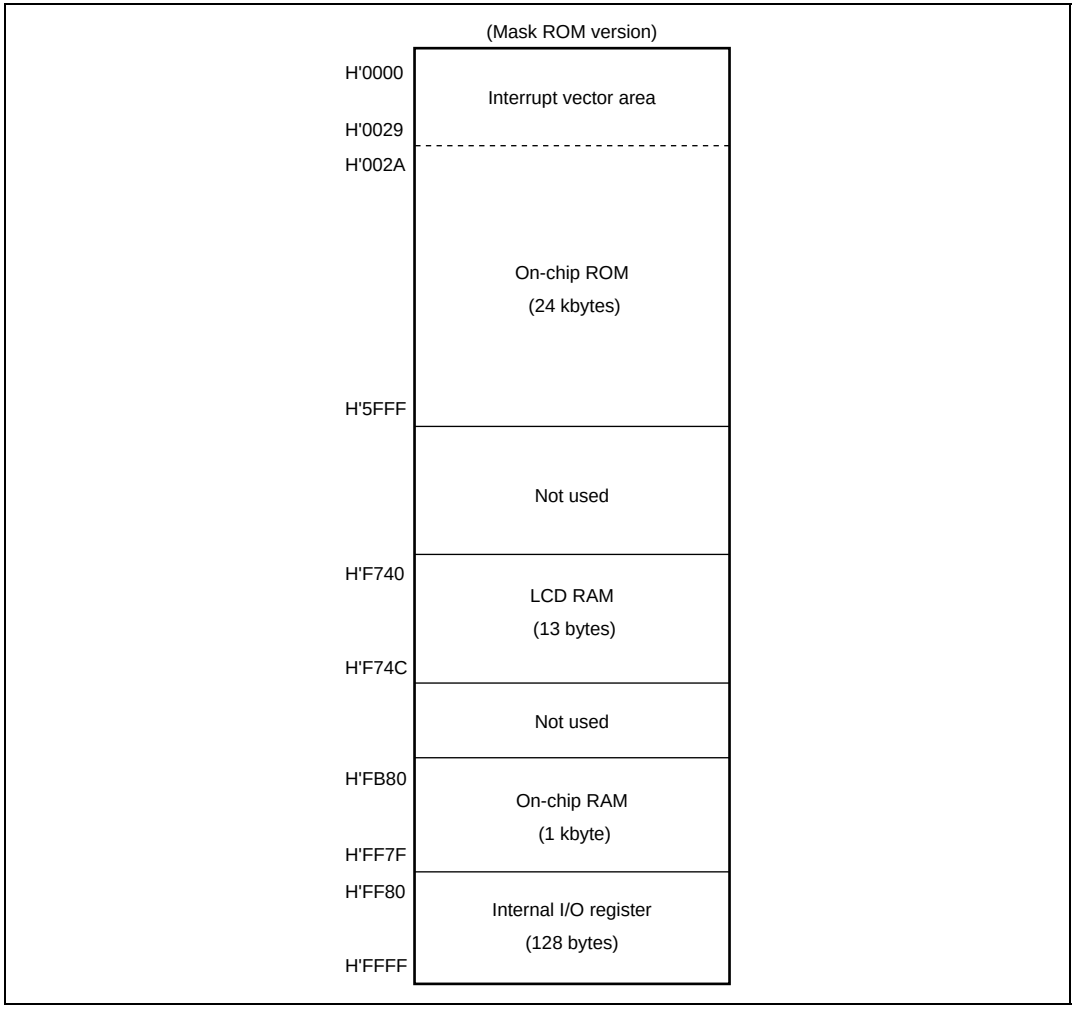


Figure 2.1(5) H8/38003, H8/38103 Memory Map

Figure 2.10 shows the instruction formats of system control instructions.

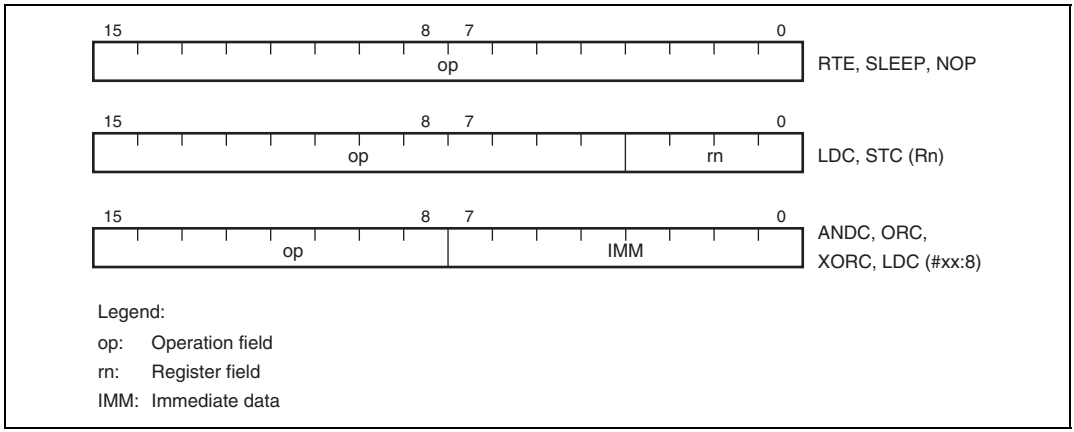


Figure 2.10 Instruction Formats of System Control Instructions

2.5.8 Block Data Transfer Instructions

Table 2.10 describes the block data transfer instructions.

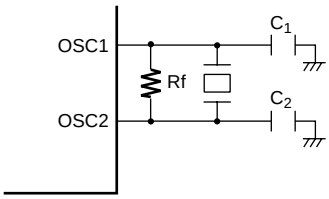
Table 2.10 Block Data Transfer Instructions

Instruction	Size	Function
EEPMOV	—	If R4L ≠ 0 then repeat @R5+ → @R6+ R4L – 1 → R4L until R4L = 0 else next; Block data transfer instruction. Transfers the number of data bytes specified by R4L from locations starting at the address indicated by R5 to locations starting at the address indicated by R6. After the transfer, the next instruction is executed.

Certain precautions are required in using the EEPMOV instruction. See section 2.9.3, EEPMOV Instruction, for details.

4.3.2 Connecting Ceramic Resonator

Figure 4.6(1) shows a typical method of connecting a ceramic oscillator to the H8/3802 Group, and figure 4.6(2) shows a typical method of connecting a crystal oscillator to the H8/38004, H8/38002S and H8/38104 Group.

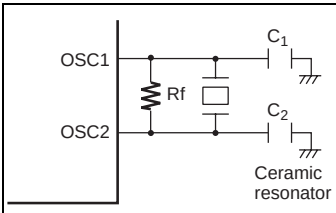


Frequency	Manufacturer	C1, C2 Recommendation Value
4.0 MHz	Murata Manufacturing Co., Ltd.	30 pF ±10%

$C_1 = C_2$ = 30 pF ±10%
Rf = 1 MΩ ±20%

Note: Consult with the ceramic resonator manufacturer to determine the circuit constants.

Figure 4.6(1) Typical Connection to Ceramic Resonator (H8/3802 Group)



Frequency	Manufacturer	Prodoct Name	C1, C2 Recommendation Value
2.0 MHz	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0	15 pF ±20%
		CSTCC2M00G56-B0	47 pF ±20%
10.0 MHz		CSTLS10M0G53-B0	15 pF ±20%
		CSTLS10M0G56-B0	47 pF ±20%
16.0 MHz*1		CSTLS16M0X53-B0	15 pF ±20%
20.0 MHz*2		CSTLS20M0X53-B0	15 pF ±20%

Rf = 1 MΩ ±20%

Notes: Consult with the crystal resonator manufacturer to determine the circuit constants.
1. This does not apply to the H8/38004 and H8/38002S Group.
2. H8/38104 Group only.

Figure 4.6(2) Typical Connection to Ceramic Resonator (H8/38004, H8/38002S, H8/38104 Group)

6.10.3 Memory Read Mode

After completion of auto-program/auto-erase/status read operations, a transition is made to the command wait state. When reading memory contents, a transition to memory read mode must first be made with a command write, after which the memory contents are read. Once memory read mode has been entered, consecutive reads can be performed.

1. In memory read mode, command writes can be performed in the same way as in the command wait state.
2. After powering on, memory read mode is entered.
3. Tables 6.12 to 6.14 show the AC characteristics.

Table 6.12 AC Characteristics in Transition to Memory Read Mode

(Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Test Condition
Command write cycle	t_{nxtc}	20	—	µs	Figure 6.13
$\overline{CE}$ hold time	t_{ceh}	0	—	ns	
$\overline{CE}$ setup time	t_{ces}	0	—	ns	
Data hold time	t_{dh}	50	—	ns	
Data setup time	t_{ds}	50	—	ns	
Write pulse width	t_{wep}	70	—	ns	
$\overline{WE}$ rise time	t_r	—	30	ns	
$\overline{WE}$ fall time	t_f	—	30	ns	

Table 6.18 Return Codes in Status Read Mode

Pin Name	Initial Value	Description
I/O7	0	1: Abnormal end 0: Normal end
I/O6	0	1: Command error 0: Otherwise
I/O5	0	1: Programming error 0: Otherwise
I/O4	0	1: Erasing error 0: Otherwise
I/O3	0	Undefined
I/O2	0	Undefined
I/O1	0	1: Over counting of writing or erasing 0: Otherwise
I/O0	0	1: Effective address error 0: Otherwise

6.10.7 Status Polling

1. The I/O7 status polling flag indicates the operating status in auto-program/auto-erase mode.
2. The I/O6 status polling flag indicates a normal or abnormal end in auto-program/auto-erase mode.

Table 6.19 Status Polling Output

I/O7	I/O6	I/O0 to I/O5	Status
0	0	0	During internal operation
1	0	0	Abnormal end
1	1	0	Normal end
0	1	0	—

8.2.2 Port Control Register 4 (PCR4)

PCR4 controls whether each of the port 4 pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	PCR42	0	W	Setting a PCR4 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR4 and in PDR4 are valid only when the corresponding pin is designated in SCR3 and SCR2 as a general I/O pin. PCR4 is a write-only register. Bits 2 to 0 are always read as 1.
1	PCR41	0	W	
0	PCR40	0	W	

8.2.3 Serial Port Control Register (SPCR)

SPCR performs input/output data inversion switching of the RXD32 and TXD32 pins. Figure 8.3 shows the configuration.

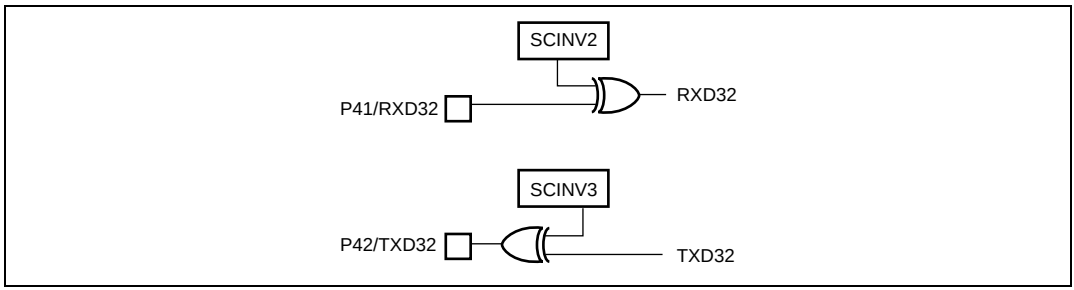


Figure 8.3 Input/Output Data Inversion Function

8.3.5 Pin Functions

The port 5 pin functions are shown below.

- P57/$\overline{\text{WKP7}}$/SEG8 to P54/$\overline{\text{WKP4}}$/SEG5 pins

The pin function depends on the combination of bit WKPn in PMR5, bit PCR5n in PCR5, and bits SGS3 to SGS0 in LPCR.

(n = 7 to 4)

SGS3 to SGS0	Other than B′0010, B′0011, B′0100, B′0101, B′0110, B′0111, B′1000, B′1001			B′0010, B′0011, B′0100, B′0101, B′0110, B′0111, B′1000, B′1001
WKPn	0		1	*
PCR5n	0	1	*	*
Pin Function	P5n input pin	P5n output pin	WKPn input pin	SEGn+1 output pin

Legend: *: Don't care.

- P53/$\overline{\text{WKP3}}$/SEG4 to P50/$\overline{\text{WKP0}}$/SEG1 pins

The pin function depends on the combination of bit WKPm in PMR5, bit PCR5m in PCR5, and bits SGS3 to SGS0 in LPCR.

(m = 3 to 0)

SGS3 to SGS0	Other than B′0001, B′0010, B′0011, B′0100, B′0101, B′0110, B′0111, B′1000			B′0001, B′0010, B′0011, B′0100, B′0101, B′0110, B′0111, B′1000
WKPm	0		1	*
PCR5m	0	1	*	*
Pin Function	P5m input pin	P5m output pin	WKPm input pin	SEGm+1 output pin

Legend: *: Don't care.

9.2 Timer A

The timer A is an 8-bit timer with interval timing and realtime clock time-base functions. The clock time-base function is available when a 32.768kHz crystal oscillator is connected. Figure 9.1 shows a block diagram of the timer A.

9.2.1 Features

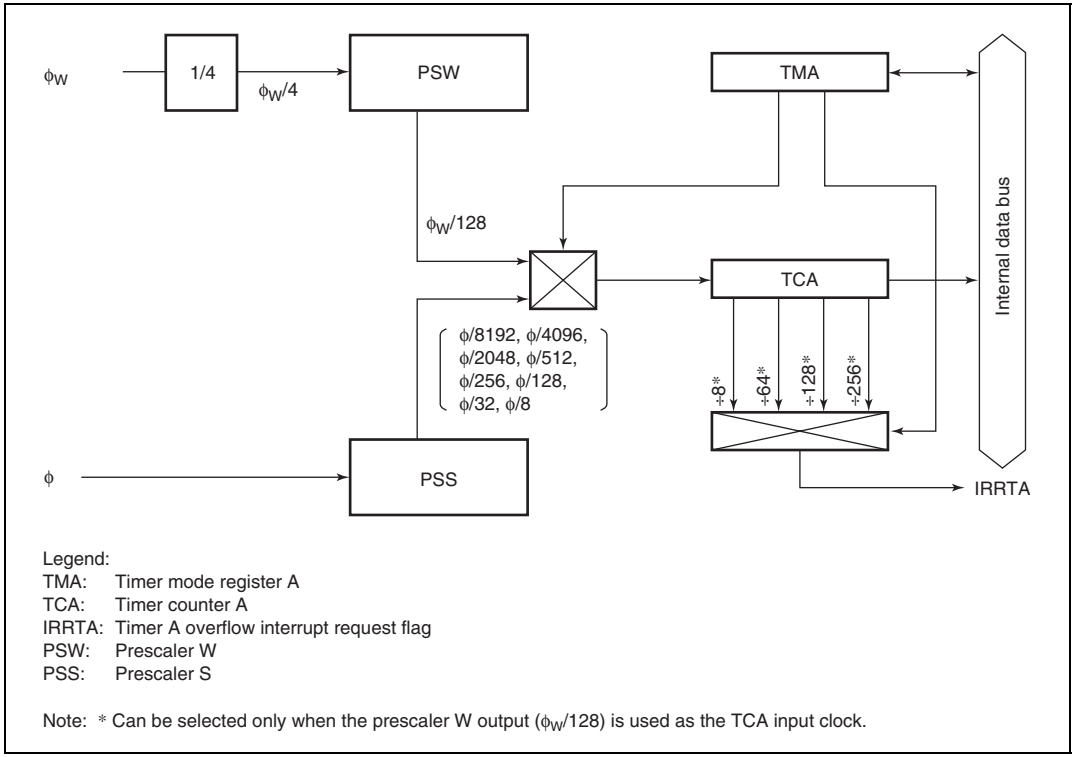
- The timer A can be used as an interval timer or a clock time base.
- An interrupt is requested when the counter overflows.
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 5.4, Module Standby Function.)

Interval Timer

- Choice of eight internal clock sources (ϕ/8192, ϕ/4096, ϕ/2048, ϕ/512, ϕ/256, ϕ/128, ϕ/32, and ϕ8)

Clock Time Base

- Choice of four overflow periods (1 s, 0.5 s, 0.25 s, and 31.25 ms) when timer A is used as a clock time base (using a 32.768 kHz crystal oscillator).



Legend:
TMA: Timer mode register A
TCA: Timer counter A
IRRTA: Timer A overflow interrupt request flag
PSW: Prescaler W
PSS: Prescaler S

Note: * Can be selected only when the prescaler W output (ϕ_W/128) is used as the TCA input clock.

Figure 9.1 Block Diagram of Timer A

9.2.2 Register Descriptions

The timer A has the following registers.

- Timer mode register A (TMA)
- Timer counter A (TCA)

Timer Mode Register A (TMA): TMA selects the operating mode, the divided clock output, and the input clock.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	—	W	Reserved The write value should always be 0.

9.4.2 Input/Output Pins

Table 9.5 shows the pin configuration of the asynchronous event counter.

Table 9.5 Pin Configuration

Name	Abbreviation	I/O	Function
Asynchronous event input H	AEVH	Input	Event input pin for input to event counter H
Asynchronous event input L	AEVL	Input	Event input pin for input to event counter L
Event input enable interrupt input	IRQAEC	Input	Input pin for interrupt enabling event input

9.4.3 Register Descriptions

The asynchronous event counter has the following registers.

- Event counter PWM compare register H (ECPWCRH)
- Event counter PWM compare register L (ECPWCRL)
- Event counter PWM data register H (ECPWDRH)
- Event counter PWM data register L (ECPWDRL)
- Input pin edge select register (AEGSR)
- Event counter control register (ECCR)
- Event counter control/status register (ECCSR)
- Event counter H (ECH)
- Event counter L (ECL)

Event Counter PWM Data Register H (ECPWDRH): ECPWDRH controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRH7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRH6	0	W	
5	ECPWDRH5	0	W	
4	ECPWDRH4	0	W	
3	ECPWDRH3	0	W	
2	ECPWDRH2	0	W	
1	ECPWDRH1	0	W	
0	ECPWDRH0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRH should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRH.

Event Counter PWM Data Register L (ECPWDRL): ECPWDRL controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRL7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRL6	0	W	
5	ECPWDRL5	0	W	
4	ECPWDRL4	0	W	
3	ECPWDRL3	0	W	
2	ECPWDRL2	0	W	
1	ECPWDRL1	0	W	
0	ECPWDRL0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRL should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRL.

10.5 Operation in Clocked Synchronous Mode

Figure 10.9 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received synchronous with clock pulses. A single character in the transmit data consists of the 8-bit data starting from the LSB. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI3 receives data in synchronous with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex communication through the use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

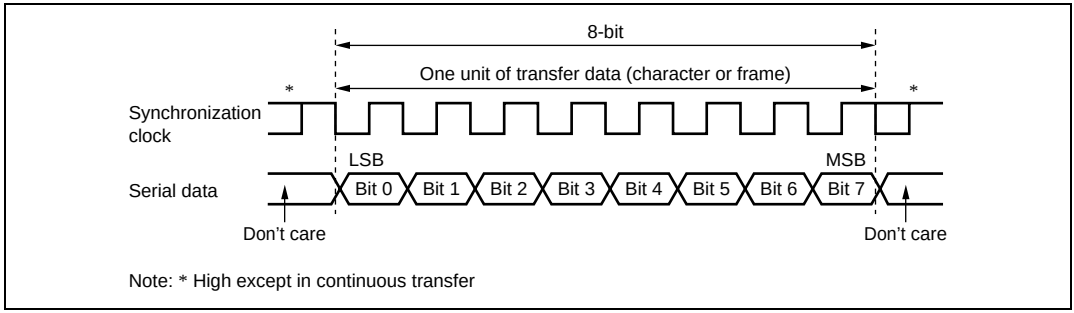


Figure 10.9 Data Format in Clocked Synchronous Communication

10.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK32 pin can be selected, according to the setting of the COM bit in SMR and CKE0 and CKE1 bits in SCR3. When the SCI3 is operated on an internal clock, the serial clock is output from the SCK32 pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

10.5.2 SCI3 Initialization

Before transmitting and receiving data, the SCI3 should be initialized as described in a sample flowchart in figure 10.4.

12.4.2 Operating States of A/D Converter

Table 12.2 shows the operating states of the A/D converter.

Table 12.2 Operating States of A/D Converter

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
AMR	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
ADSR	Reset	Functions	Functions	Reset	Reset	Reset	Reset	Reset
ADRRH	Retained*	Functions	Functions	Retained	Retained	Retained	Retained	Retained
ADRRL	Retained*	Functions	Functions	Retained	Retained	Retained	Retained	Retained

Note: * Undefined in a power-on reset.

12.5 Example of Use

An example of how the A/D converter can be used is given below, using channel 1 (pin AN1) as the analog input channel. Figure 12.2 shows the operation timing.

1. Bits CH3 to CH0 in the A/D mode register (AMR) are set to 0101, making pin AN1 the analog input channel. A/D interrupts are enabled by setting bit IENAD to 1, and A/D conversion is started by setting bit ADSF to 1.
2. When A/D conversion is completed, bit IRRAD is set to 1, and the A/D conversion result is stored in ADRRH and ADRRL. At the same time bit ADSF is cleared to 0, and the A/D converter goes to the idle state.
3. Bit IENAD = 1, so an A/D conversion end interrupt is requested.
4. The A/D interrupt handling routine starts.
5. The A/D conversion result is read and processed.
6. The A/D interrupt handling routine ends.

If bit ADSF is set to 1 again afterward, A/D conversion starts and steps 2 through 6 take place.

Figures 12.3 and 12.4 show flowcharts of procedures for using the A/D converter.

12.6 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 12.5).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (see figure 12.6).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (see figure 12.6).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristics between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error.
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

12.7.3 Additional Usage Notes

1. ADRRH and ADRRL should be read only when the ADSF bit in ADSR is cleared to 0.
2. Changing the digital input signal at an adjacent pin during A/D conversion may adversely affect conversion accuracy.
3. When A/D conversion is started after clearing module standby mode, wait for 10ϕ clock cycles before starting A/D conversion.
4. In active mode and sleep mode, the analog power supply current flows in the ladder resistance even when the A/D converter is on standby. Therefore, if the A/D converter is not used, it is recommended that AVcc be connected to the system power supply and the ADCKSTP bit be cleared to 0 in CKSTPR1.

Mnemonic		Operand Size	Addressing Modes/Instruction Length (bytes)								Operation	Condition Code						Number of Execution States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	—		I	H	N	Z	V	C	
BSET	BSET #xx:3, @aa:8	B						4			(#xx:3 of @aa:8) ← 1		—	—	—	—	—	—	8
	BSET Rn, Rd	B		2							(Rn8 of Rd8) ← 1		—	—	—	—	—	—	2
	BSET Rn, @Rd	B			4						(Rn8 of @Rd16) ← 1		—	—	—	—	—	—	8
	BSET Rn, @aa:8	B						4			(Rn8 of @aa:8) ← 1		—	—	—	—	—	—	8
BCLR	BCLR #xx:3, Rd	B		2							(#xx:3 of Rd8) ← 0		—	—	—	—	—	—	2
	BCLR #xx:3, @Rd	B			4						(#xx:3 of @Rd16) ← 0		—	—	—	—	—	—	8
	BCLR #xx:3, @aa:8	B						4			(#xx:3 of @aa:8) ← 0		—	—	—	—	—	—	8
	BCLR Rn, Rd	B		2							(Rn8 of Rd8) ← 0		—	—	—	—	—	—	2
	BCLR Rn, @Rd	B			4						(Rn8 of @Rd16) ← 0		—	—	—	—	—	—	8
	BCLR Rn, @aa:8	B						4			(Rn8 of @aa:8) ← 0		—	—	—	—	—	—	8
BNOT	BNOT #xx:3, Rd	B		2							(#xx:3 of Rd8)←(#xx:3 of Rd8)		—	—	—	—	—	—	2
	BNOT #xx:3, @Rd	B			4						(#xx:3 of @Rd16) ←(#xx:3 of @Rd16)		—	—	—	—	—	—	8
	BNOT #xx:3, @aa:8	B						4			(#xx:3 of @aa:8) ←(#xx:3 of @aa:8)		—	—	—	—	—	—	8
	BNOT Rn, Rd	B		2							(Rn8 of Rd8) ←(Rn8 of Rd8)		—	—	—	—	—	—	2
	BNOT Rn, @Rd	B			4						(Rn8 of @Rd16) ←(Rn8 of @Rd16)		—	—	—	—	—	—	8
	BNOT Rn, @aa:8	B						4			(Rn8 of @aa:8) ←(Rn8 of @aa:8)		—	—	—	—	—	—	8
BTST	BTST #xx:3, Rd	B		2							(#xx:3 of Rd8)→Z		—	—	—	↕	—	—	2
	BTST #xx:3, @Rd	B			4						(#xx:3 of @Rd16)→Z		—	—	—	↕	—	—	6
	BTST #xx:3, @aa:8	B						4			(#xx:3 of @aa:8)→Z		—	—	—	↕	—	—	6
	BTST Rn, Rd	B		2							(Rn8 of Rd8)→Z		—	—	—	↕	—	—	2

Appendix F Chip Form Specifications

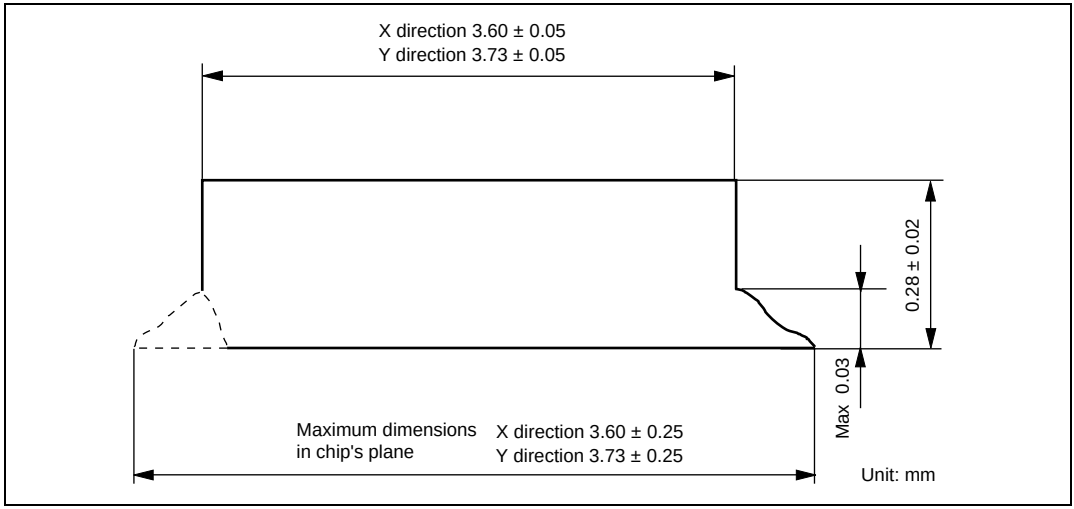


Figure F.1 Cross-Sectional View of Chip (HCD6433802, HCD6433801, and HCD6433800)

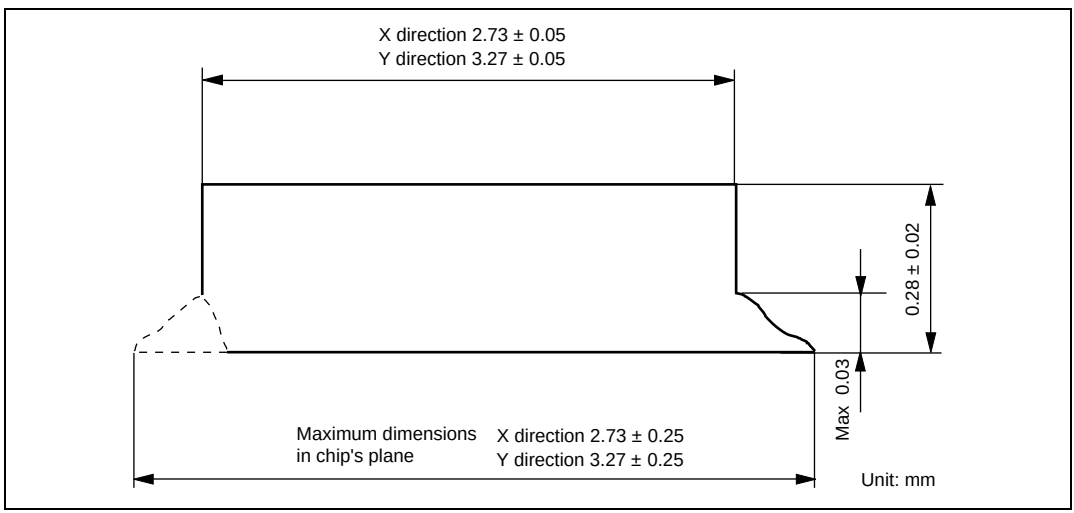


Figure F.2 Cross-Sectional View of Chip (HCD64338004, HCD64338003, HCD64338002, HCD64338001, and HCD64338000)