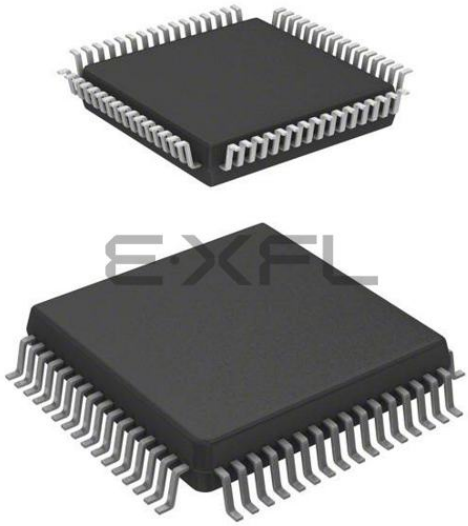

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38004h4v

Section 6 ROM

Section 8 I/O Ports

Section 9 Timers

Section 10 Serial Communication Interface 3 (SCI3)

Table 1.3 Pad Coordinate of HCD64F38004 and HCD64F38002

Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)	Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)
1	PB3/$\overline{\text{IRQ1}}$/AN3	-1915	1490	32	P71/SEG18	1411	-1779
2	X1	-1915	1182	33	P70/SEG17	1628	-1779
3	X2	-1915	1022	34	P67/SEG16	1914	-1496
4	Vss	-1915	926	35	P66/SEG15	1914	-1297
5	Vss = AVss	-1915	786	36	P65/SEG14	1914	-1098
6	OSC2	-1915	648	37	P64/SEG13	1914	-899
7	OSC1	-1915	495	38	P63/SEG12	1914	-700
8	TEST	-1915	295	39	P62/SEG11	1914	-500
9	$\overline{\text{RES}}$	-1915	96	40	P61/SEG10	1914	-302
10	P31/TMOFL	-1915	-103	41	P60/SEG9	1914	-103
11	P32/TMOFH	-1915	-302	42	P57/$\overline{\text{WKP7}}$/SEG8	1914	96
12	P33	-1915	-486	43	P56/$\overline{\text{WKP6}}$/SEG7	1914	295
13	P34	-1915	-657	44	P55/$\overline{\text{WKP5}}$/SEG6	1914	495
14	P35	-1915	-750	45	P54/$\overline{\text{WKP4}}$/SEG5	1914	694
15	P36/AEVH	-1915	-989	46	P53/$\overline{\text{WKP3}}$/SEG4	1914	893
16	P37/AEVL	-1915	-1247	47	P52/$\overline{\text{WKP2}}$/SEG3	1914	1092
17	Vcc	-1915	-1438	48	P51/$\overline{\text{WKP1}}$/SEG2	1914	1291
18	V1	-1623	-1779	49	P50/$\overline{\text{WKP0}}$/SEG1	1914	1490
19	V2	-1406	-1779	50	P90/PWM1	1628	1779
20	V3	-1189	-1779	51	P91/PWM2	1368	1779
21	PA3/COM4	-973	-1779	52	P92	1113	1779
22	PA2/COM3	-756	-1779	53	P93	976	1779
23	PA1/COM2	-539	-1779	54	P94	759	1779
24	PA0/COM1	-323	-1779	55	P95	542	1779
25	P80/SEG25	-106	-1779	56	Vss	324	1779
26	P77/SEG24	111	-1779	57	IRQAEC	96	1779
27	P76/SEG23	328	-1779	58	P40/SCK32	-109	1779
28	P75/SEG22	544	-1779	59	P41/RXD32	-327	1779
29	P74/SEG21	761	-1779	60	P42/TXD32	-545	1779
30	P73/SEG20	978	-1779	61	P43/$\overline{\text{IRQ0}}$	-762	1779
31	P72/SEG19	1194	-1779	62	AVcc	-980	1779

2.7 Basic Bus Cycle

CPU operation is synchronized by a system clock (ϕ) or a subclock (ϕ_{SUB}). For details on these clock signals see section 4, Clock Pulse Generators. The period from a rising edge of ϕ or ϕ_{SUB} to the next rising edge is called one state. A bus cycle consists of two states or three states. The cycle differs depending on whether access is to on-chip memory or to on-chip peripheral modules.

2.7.1 Access to On-Chip Memory (RAM, ROM)

Access to on-chip memory takes place in two states. The data bus width is 16 bits, allowing access in byte or word size. Figure 2.12 shows the on-chip memory access cycle.

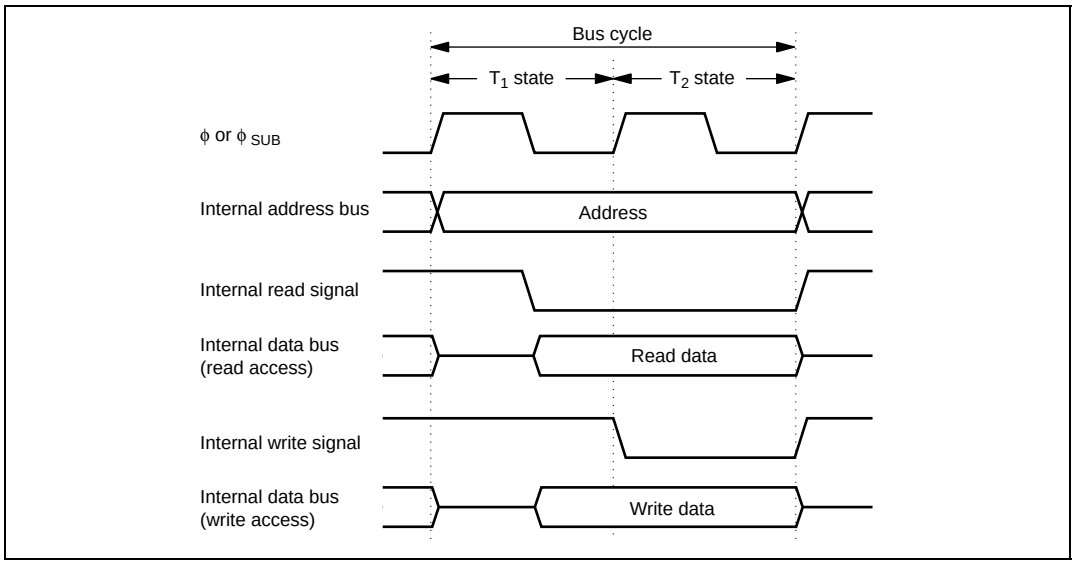


Figure 2.12 On-Chip Memory Access Cycle

Three-State Access to On-Chip Peripheral Modules:

Figure 2.14 shows the operation timing in the case of three-state access to an on-chip peripheral module.

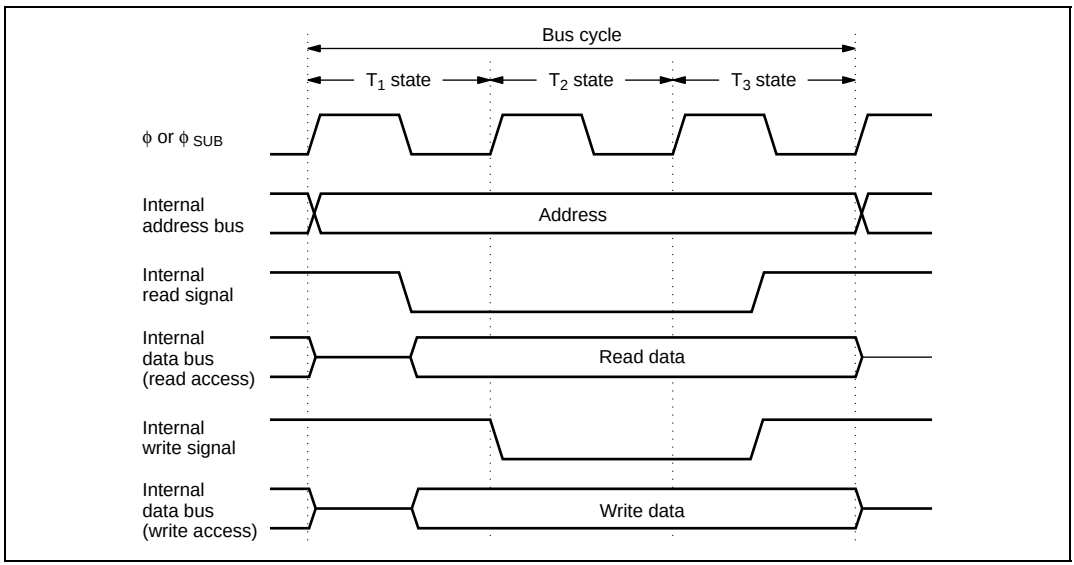


Figure 2.14 On-Chip Peripheral Module Access Cycle (3-State Access)

5.1.2 System Control Register 2 (SYSCR2)

SYSCR2 controls the power-down modes, as well as SYSCR1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select Selects the frequency at which the watch clock signal (ϕ_w) generated by the subclock pulse generator is sampled, in relation to the oscillator clock (ϕ_{osc}) generated by the system clock pulse generator. When ϕ_{osc} = 2 to 16 MHz, clear this bit to 0. 0: Sampling rate is ϕ_{osc}/16. 1: Sampling rate is ϕ_{osc}/4.
3	DTON	0	R/W	Direct Transfer on Flag Selects the mode to which the transition is made after the SLEEP instruction is executed with bits SSBY and LSON in SYSCR1, bit MSON in SYSCR2, and bit TMA3 in TMA. For details, see table 5.2.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode. 0: Operation in active (high-speed) mode 1: Operation in active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

Legend: X: Don't care.

- Direct transfer from subactive mode to active (medium-speed) mode

  When a SLEEP instruction is executed in subactive mode while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, the MSON bit in SYSCR2 is set to 1, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made directly to active (medium-speed) mode via watch mode after the waiting time set in bits STS2 to STS0 in SYSCR1 has elapsed.

5.3.1 Direct Transition from Active (High-Speed) Mode to Active (Medium-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (1).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of internal processing states)} × (tcyc before transition) + (Number of interrupt exception handling execution states) × (tcyc after transition)

……(1)

Example: Direct transition time = (2 + 1) × 2tosc + 14 × 16tosc = 230tosc (when ϕ/8 is selected as the CPU operating clock)

Legend:
tosc: OSC clock cycle time
tcyc: System clock (ϕ) cycle time

6.8 Flash Memory Programming/Erasing

A software method using the CPU is employed to program and erase flash memory in the on-board programming modes. Depending on the FLMCR1 setting, the flash memory operates in one of the following four modes: Program mode, program-verify mode, erase mode, and erase-verify mode. The programming control program in boot mode and the user program/erase control program in user program mode use these operating modes in combination to perform programming/erasing. Flash memory programming and erasing should be performed in accordance with the descriptions in section 6.8.1, Program/Program-Verify and section 6.8.2, Erase/Erase-Verify, respectively.

6.8.1 Program/Program-Verify

When writing data or programs to the flash memory, the program/program-verify flowchart shown in figure 6.10 should be followed. Performing programming operations according to this flowchart will enable data or programs to be written to the flash memory without subjecting the chip to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to which programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer must be performed even if writing fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data area, a 128-byte reprogramming data area, and a 128-byte additional-programming data area. Perform reprogramming data computation according to table 6.8, and additional programming data computation according to table 6.9.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data area or additional-programming data area to the flash memory. The program address and 128-byte data are latched in the flash memory. The lower 8 bits of the start address in the flash memory destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Table 6.10 shows the allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. An overflow cycle of approximately 6.6 ms is allowed.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower one bit is B'0. Verify data can be read in word units from the address to which a dummy write was performed.

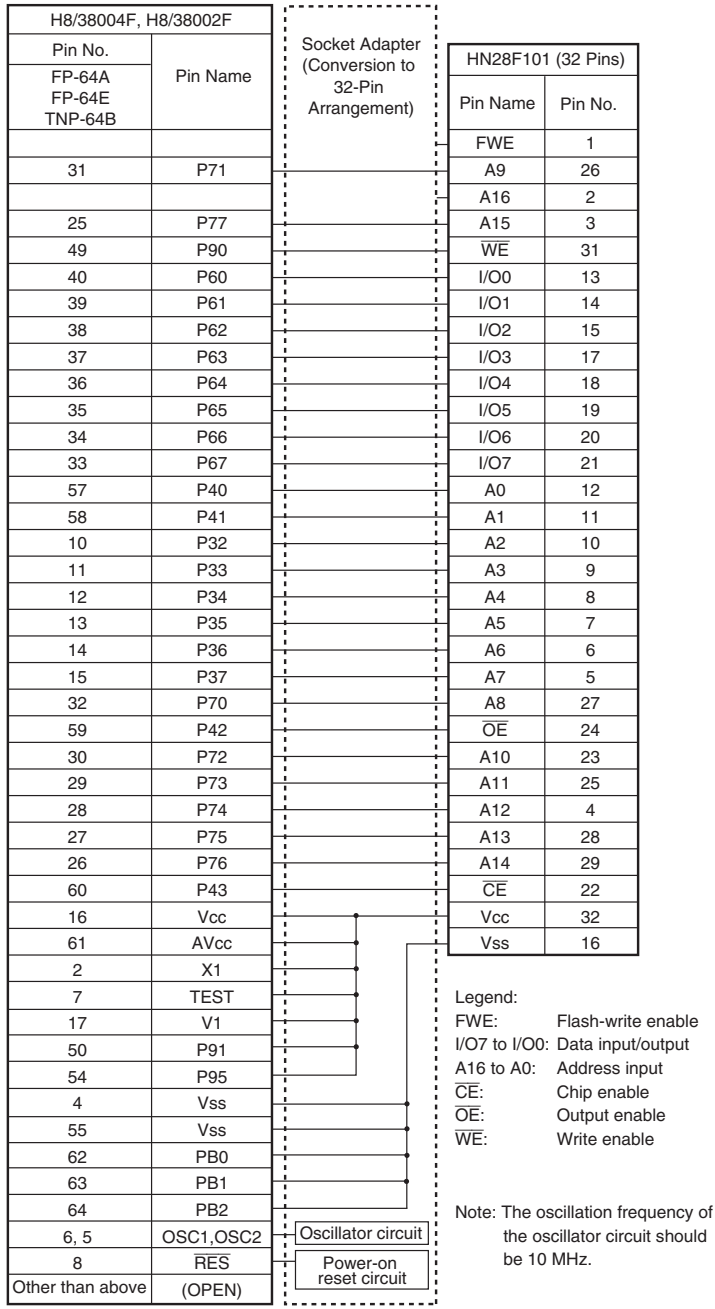


Figure 6.12(1) Socket Adapter Pin Correspondence Diagram (H8/38004F, H8/38002F)

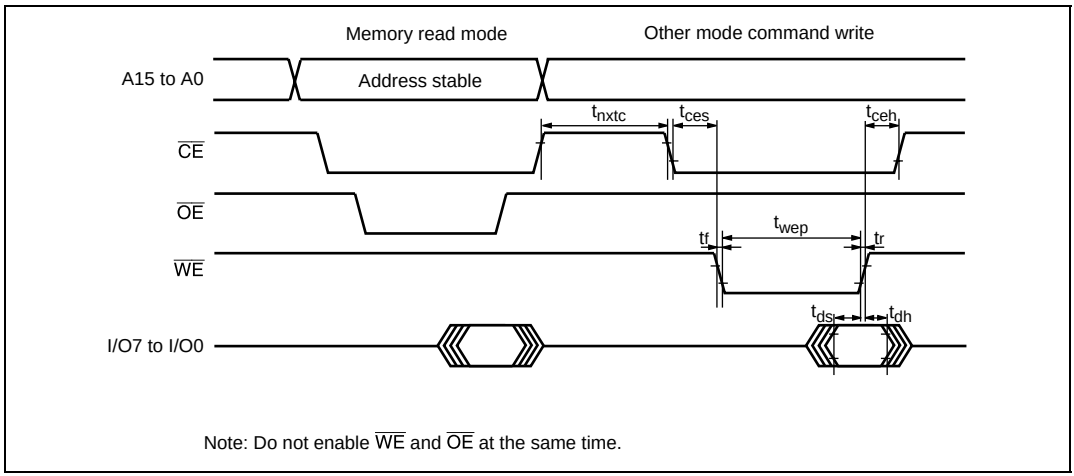


Figure 6.14 Timing Waveforms in Transition from Memory Read Mode to Another Mode

Table 6.14 AC Characteristics in Memory Read Mode

(Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Test Condition
Access time	t_{acc}	—	20	µs	Figures 6.15 and 6.16
$\overline{CE}$ output delay time	t_{ce}	—	150	ns	
$\overline{OE}$ output delay time	t_{oe}	—	150	ns	
Output disable delay time	t_{df}	—	100	ns	
Data output hold time	t_{oh}	5	—	ns	

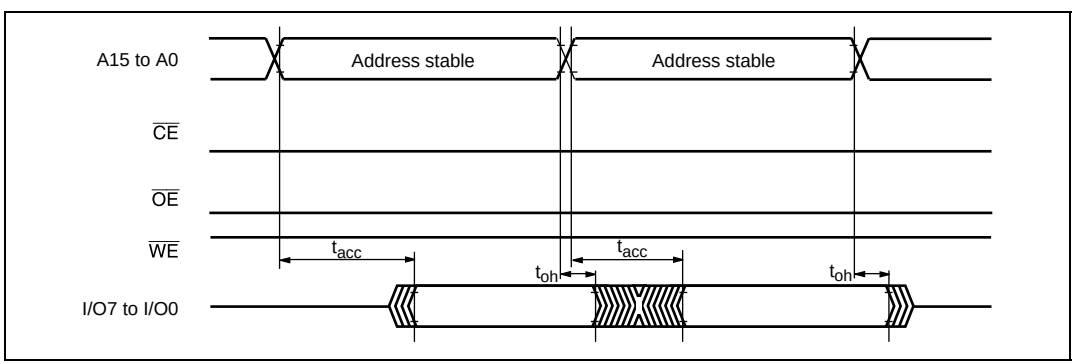


Figure 6.15 Timing Waveforms in $\overline{CE}$ and $\overline{OE}$ Enable State Read

8.3.1 Port Data Register 5 (PDR5)

PDR5 is a register that stores data of port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	P57	0	R/W	If port 5 is read while PCR5 bits are set to 1, the values stored in PDR5 are read, regardless of the actual pin states. If port 5 is read while PCR5 bits are cleared to 0, the pin states are read.
6	P56	0	R/W	
5	P55	0	R/W	
4	P54	0	R/W	
3	P53	0	R/W	
2	P52	0	R/W	
1	P51	0	R/W	
0	P50	0	R/W	

8.3.2 Port Control Register 5 (PCR5)

PCR5 controls whether each of the port 5 pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR57	0	W	Setting a PCR5 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR5 and in PDR5 are valid only when the corresponding pin is designated by PMR5 and the SGS3 to SGS0 bits in LPCR as a general I/O pin.
6	PCR56	0	W	
5	PCR55	0	W	
4	PCR54	0	W	
3	PCR53	0	W	PCR5 is a write-only register. Bits 7 to 0 are always read as 1.
2	PCR52	0	W	
1	PCR51	0	W	
0	PCR50	0	W	

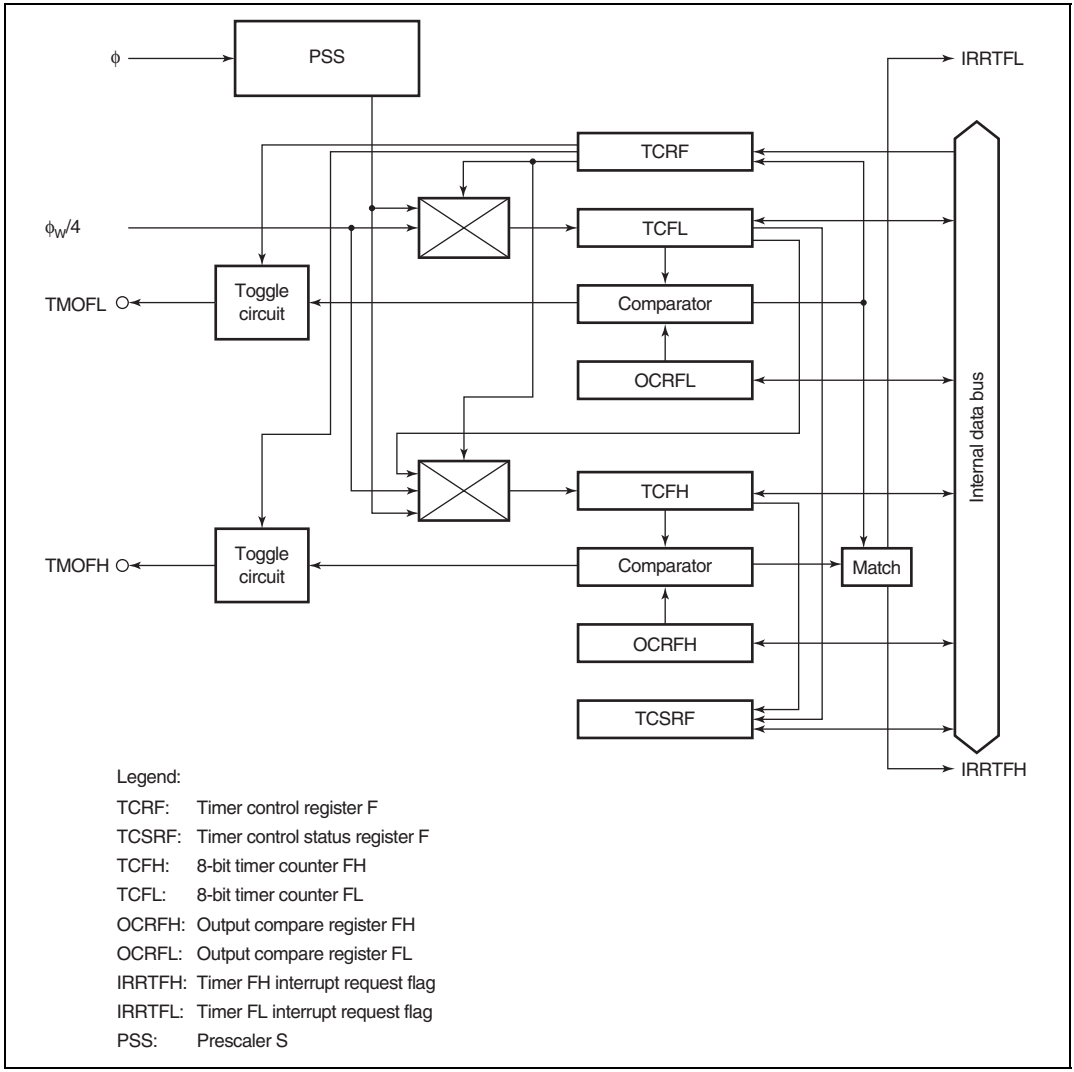


Figure 9.2 Block Diagram of Timer F

9.4.2 Input/Output Pins

Table 9.5 shows the pin configuration of the asynchronous event counter.

Table 9.5 Pin Configuration

Name	Abbreviation	I/O	Function
Asynchronous event input H	AEVH	Input	Event input pin for input to event counter H
Asynchronous event input L	AEVL	Input	Event input pin for input to event counter L
Event input enable interrupt input	IRQAEC	Input	Input pin for interrupt enabling event input

9.4.3 Register Descriptions

The asynchronous event counter has the following registers.

- Event counter PWM compare register H (ECPWCRH)
- Event counter PWM compare register L (ECPWCRL)
- Event counter PWM data register H (ECPWDRH)
- Event counter PWM data register L (ECPWDRL)
- Input pin edge select register (AEGSR)
- Event counter control register (ECCR)
- Event counter control/status register (ECCSR)
- Event counter H (ECH)
- Event counter L (ECL)

Table 10.4 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

			Setting	
OSC (MHz)	**ϕ (MHz)**	**Maximum Bit Rate (bit/s)**	**n**	**N**
0.0384*	0.0192	600	0	0
2	1	31250	0	0
2.4576	1.2288	38400	0	0
4	2	62500	0	0
10	5	156250	0	0
16	8	250000	0	0
20	10	312500	0	0

Note: * When CKS1 = 0 and CKS0 = 1 in SMR

Table 10.5 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)

	ϕ								
	19.2 kHz			**1 MHz**			**2 MHz**		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
200	0	23	0	—	—	—	—	—	—
250	—	—	—	—	—	—	2	124	0
300	2	0	0	—	—	—	—	—	—
500				—	—	—	—	—	—
1k				0	249	0	—	—	—
2.5k				0	99	0	0	199	0
5k				0	49	0	0	99	0
10k				0	24	0	0	49	0
25k				0	9	0	0	19	0
50k				0	4	0	0	9	0
100k				—	—	—	0	4	0
250k				0	0	0	0	1	0
500k							0	0	0
1M									

12.7.3 Additional Usage Notes

1. ADRRH and ADRRL should be read only when the ADSF bit in ADSR is cleared to 0.
2. Changing the digital input signal at an adjacent pin during A/D conversion may adversely affect conversion accuracy.
3. When A/D conversion is started after clearing module standby mode, wait for 10ϕ clock cycles before starting A/D conversion.
4. In active mode and sleep mode, the analog power supply current flows in the ladder resistance even when the A/D converter is on standby. Therefore, if the A/D converter is not used, it is recommended that AVcc be connected to the system power supply and the ADCKSTP bit be cleared to 0 in CKSTPR1.

Resistance Value Calculation Table

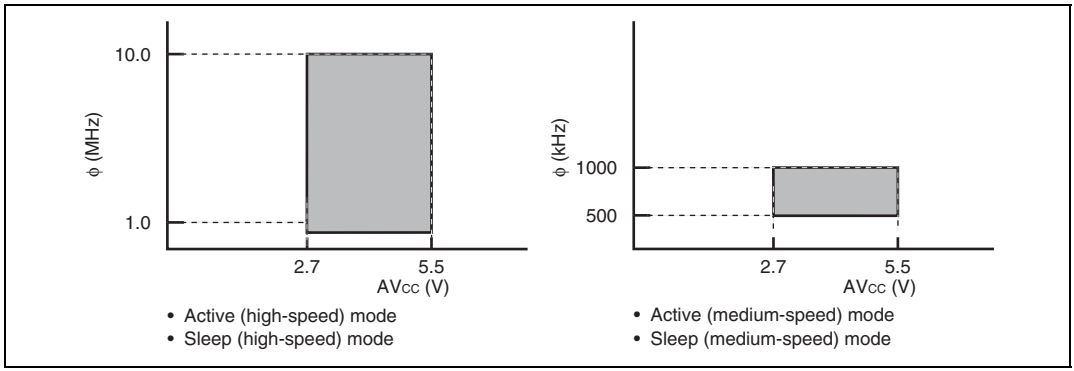
Ex. No	Vref (V)	R (kΩ)	Vreset1	Vint(D)	Vint(U)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
1	1.30	1000	2.5	2.7	2.9	517	33	450
2	1.41	1000	2.7	2.9	3	514	16	470
3	1.57	1000	3	3.2	3.5	511	42	447
4	2.09	1000	4	4.5	4.7	536	20	444

4. Using an error calculation table like the one shown below, plug in values for R1, R2, R3, and Vref to calculate the deviation of Vreset1, Vint(D), and Vint(U). Make sure to double check the maximum and minimum values for each value.

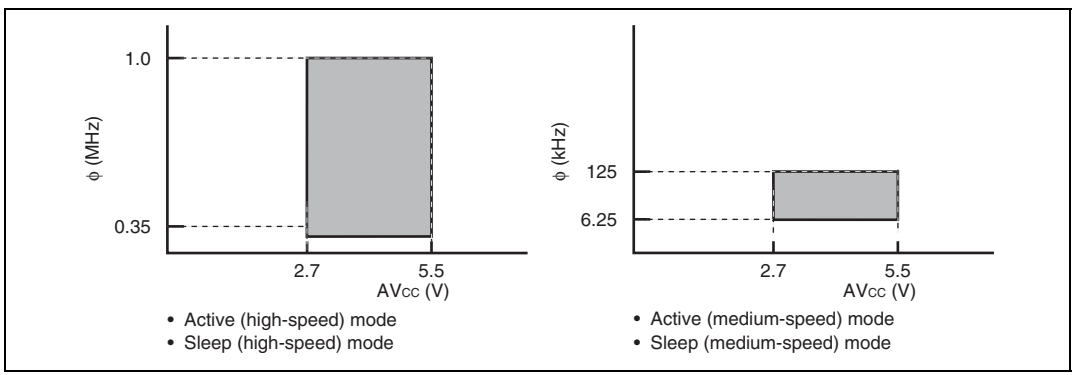
Error Calculation Table

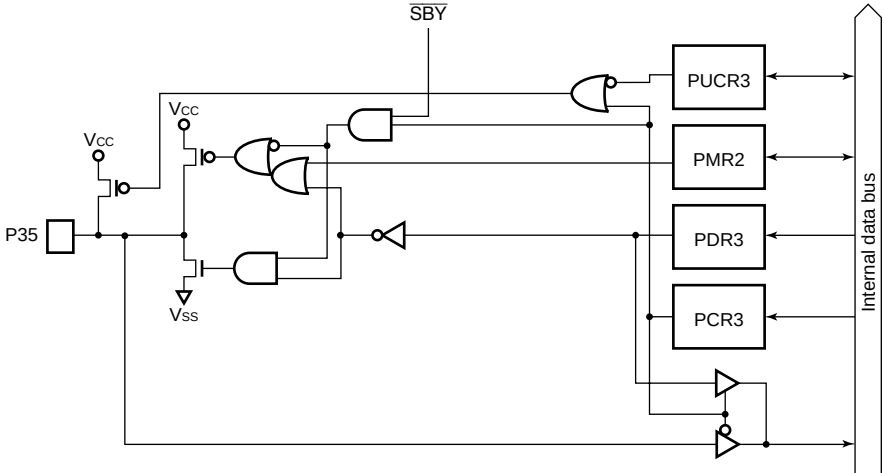
Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Resistance Value Error (%) 5	Comparator Error (V)	Vreset1 (V)	Vint(D) (V)	Vint(U) (V)
1.3	517	33	450	R1+Err, R2/R3-Err	0.1	2.59	2.94	3.15
					0	2.49	2.84	3.05
					-0.1	2.39	2.74	2.95
				R1-Err, R2/R3+Err	0.1	2.59	2.66	2.85
					0	2.49	2.56	2.75
					-0.1	2.39	2.46	2.65
				R1/R2/R3 No Err	0.1	2.59	2.79	2.99
					0	2.49	2.69	2.89
					-0.1	2.39	2.59	2.79
				R1/R2+Err, R3-Err	0.1	2.59	2.93	3.16
					0	2.49	2.83	3.06
					-0.1	2.39	2.73	2.96
				R1/R2-Err, R3+Err	0.1	2.59	2.67	2.84
					0	2.49	2.57	2.74
					-0.1	2.39	2.47	2.64

Analog Power Supply Voltage and A/D Converter Operating Range (System Clock Oscillator Selected)



Analog Power Supply Voltage and A/D Converter Operating Range (On-Chip Oscillator Selected)



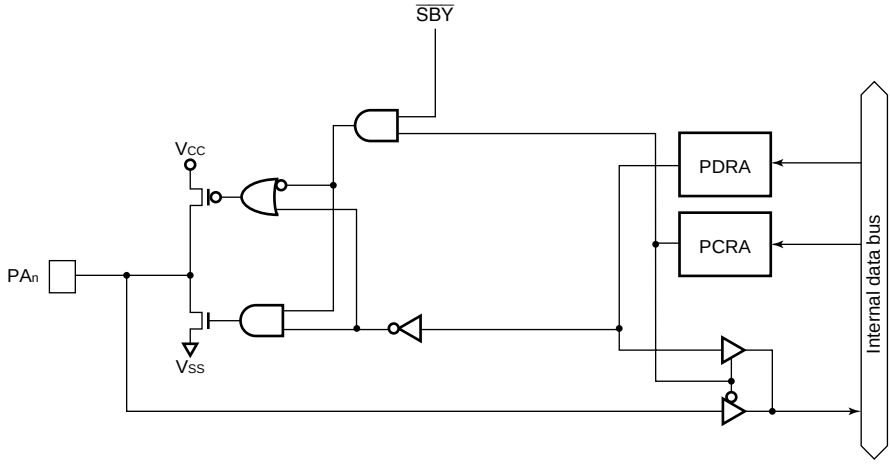


Legend:

PDR3: Port data register 3
PCR3: Port control register 3
PMR2: Port mode register 2
PUCR3: Port pull-up control register 3

Figure B.1(b) Port 3 Block Diagram (Pin P35)

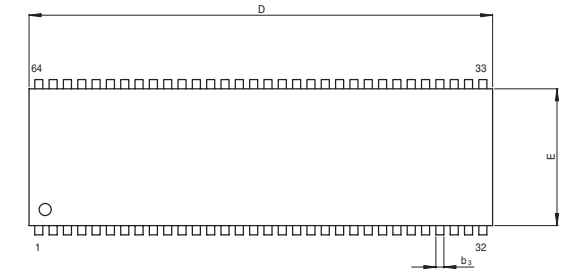
B.8 Port A Block Diagram

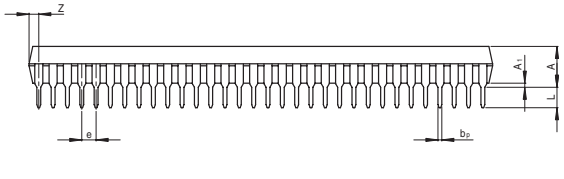


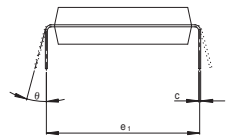
Legend:
PDRA: Port data register A
PCRA: Port control register A
n = 3 to 0

Figure B.8 Port A Block Diagram

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP64-17x57.6-1.78	PRDP0064BB-A	DP-64S/DP-64SV	8.8g







Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	——	19.05	——
D	——	57.6	58.5
E	——	17.0	18.6
A	——	——	5.08
A_1	0.51	——	——
b_p	0.38	0.48	0.58
b_3	——	1.0	——
c	0.20	0.25	0.36
θ	0°	——	15°
e	1.53	1.78	2.03
Z	——	——	1.46
L	2.54	——	——

Figure E.4 Package Dimensions (DP-64S)