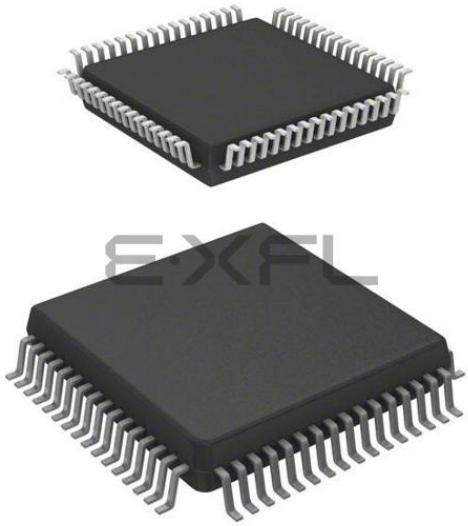


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38102hwv

4.4.2 Pin Connection when Not Using Subclock

When the subclock is not used, connect pin X1 to GND and leave pin X2 open, as shown in figure 4.11.

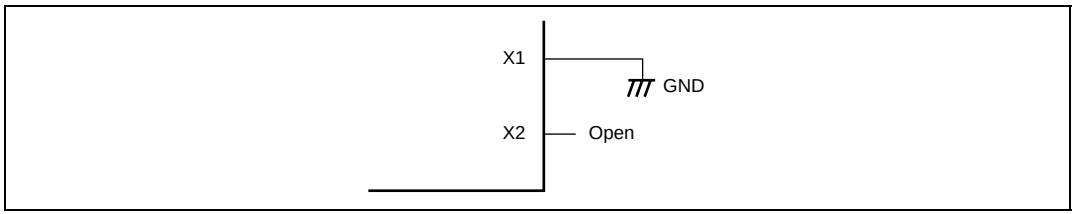


Figure 4.11 Pin Connection when Not Using Subclock

4.4.3 External Clock Input

Connect the external clock to pin X1 and leave pin X2 open, as shown in figure 4.12.

Note that input of an external clock is not supported on the H8/38104 Group.

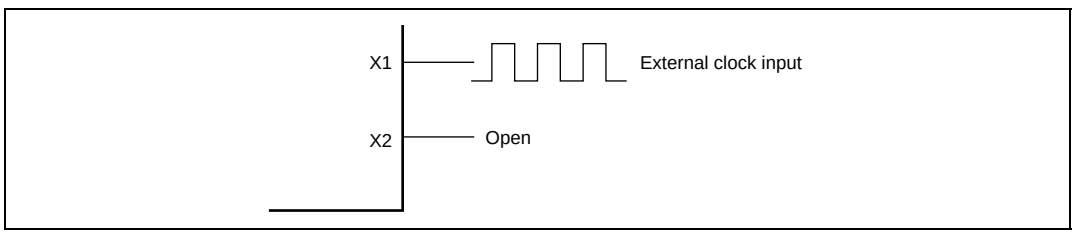


Figure 4.12 Pin Connection when Inputting External Clock

Frequency	Subclock (ϕ_w)
Duty	45% to 55%

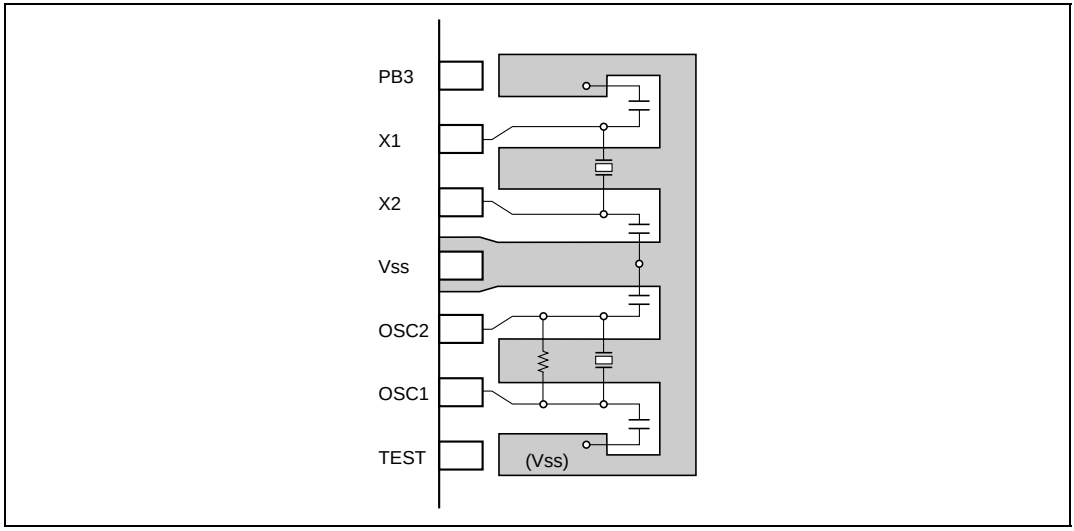


Figure 4.13 Example of Crystal and Ceramic Resonator Arrangement

Figure 4.14 (1) shows an example of the measurement circuit for the negative resistor which is recommended by the resonator manufacturer. Note that if the negative resistor in this circuit does not reach the level which is recommended by the resonator manufacturer, the main oscillator may be hard to start oscillation.

If the negative resistor does not reach the level which is recommended by the resonator manufacturer and oscillation is not started, changes as shown in figure 4.14 (2) to (4) should be made. The proposed change and capacitor size to be applied should be determined according to the evaluation result of the negative resistor and frequency deviation, etc.

5.3 Direct Transition

The CPU can execute programs in two modes: active and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition also enables operating frequency modification in active or subactive mode. After the mode transition, direct transition interrupt exception handling starts.

If the direct transition interrupt is disabled in interrupt permission register 2, a transition is made instead to sleep or watch mode. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep or watch mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

- Direct transfer from active (high-speed) mode to active (medium-speed) mode

  When a SLEEP instruction is executed in active (high-speed) mode while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is set to 1, and the DTON bit in SYSCR2 is set to 1, a transition is made to active (medium-speed) mode via sleep mode.
- Direct transfer from active (medium-speed) mode to active (high-speed) mode

  When a SLEEP instruction is executed in active (medium-speed) mode while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is cleared to 0, and the DTON bit in SYSCR2 is set to 1, a transition is made to active (high-speed) mode via sleep mode.
- Direct transfer from active (high-speed) mode to subactive mode

  When a SLEEP instruction is executed in active (high-speed) mode while the SSBY and LSON bits in SYSCR1 are set to 1, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made to subactive mode via watch mode.
- Direct transfer from subactive mode to active (high-speed) mode

  When a SLEEP instruction is executed in subactive mode while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, the MSON bit in SYSCR2 is cleared to 0, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made directly to active (high-speed) mode via watch mode after the waiting time set in bits STS2 to STS0 in SYSCR1 has elapsed.
- Direct transfer from active (medium-speed) mode to subactive mode

  When a SLEEP instruction is executed in active (medium-speed) while the SSBY and LSON bits in SYSCR1 are set to 1, the DTON bit in SYSCR2 is set to 1, and the TMA3 bit in TMA is set to 1, a transition is made to subactive mode via watch mode.

5.3.2 Direct Transition from Active (Medium-Speed) Mode to Active (High-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (2).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of internal processing states)} × (tcyc before transition) + (Number of interrupt exception handling execution states) × (tcyc after transition)

……..(2)

Example: Direct transition time = (2 + 1) × 16tosc + 14 × 2tosc = 76tosc (when ϕ/8 is selected as the CPU operating clock)

Legend:
tosc: OSC clock cycle time
tcyc: System clock (ϕ) cycle time

5.3.3 Direct Transition from Subactive Mode to Active (High-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (3).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of internal processing states)} × (tsubcyc before transition) + {(Wait time set in bits STS2 to STS0) + (Number of interrupt exception handling execution states)} × (tcyc after transition)

……..(3)

Example: Direct transition time = (2 + 1) × 8tw + (8192 + 14) × 2tosc = 24tw + 16412tosc (when ϕw/8 is selected as the CPU operating clock and wait time = 8192 states)

Legend:
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (ϕ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.6.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 is a register that displays the state of flash memory programming/erasing. FLMCR2 is a read-only register, and should not be written to.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash Memory Error Indicates that an error has occurred during an operation on flash memory (programming or erasing). When flash memory goes to the error-protection state, this bit is set to 1. See section 6.9.3, Error Protection, for details.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

6.6.3 Erase Block Register (EBR)

EBR specifies the flash memory erase area block. EBR is initialized to H'00 when the SWE bit in FLMCR1 is 0. Do not set more than one bit at a time, as this will cause all the bits in EBR to be automatically cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	—	Reserved These bits are always read as 0.
4	EB4	0	R/W	When this bit is set to 1, 28 kbytes of H'1000 to H'7FFF will be erased in the HD64F38004 and HD64F38104. When this bit is set to 1, 12 kbytes of H'1000 to H'3FFF will be erased in the HD64F38002 and HD64F38102.
3	EB3	0	R/W	When this bit is set to 1, 1 kbyte of H'0C00 to H'0FFF will be erased.
2	EB2	0	R/W	When this bit is set to 1, 1 kbyte of H'0800 to H'0BFF will be erased.
1	EB1	0	R/W	When this bit is set to 1, 1 kbyte of H'0400 to H'07FF will be erased.
0	EB0	0	R/W	When this bit is set to 1, 1 kbyte of H'0000 to H'03FF will be erased.

Table 6.17 AC Characteristics in Status Read Mode

(Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Test Condition
Read time after command write	t_{nxtc}	20	—	µs	Figure 6.19
$\overline{CE}$ hold time	t_{ceh}	0	—	ns	
$\overline{CE}$ setup time	t_{ces}	0	—	ns	
Data hold time	t_{dh}	50	—	ns	
Data setup time	t_{ds}	50	—	ns	
Write pulse width	t_{wep}	70	—	ns	
$\overline{OE}$ output delay time	t_{oe}	—	150	ns	
Disable delay time	t_{df}	—	100	ns	
$\overline{CE}$ output delay time	t_{ce}	—	150	ns	
$\overline{WE}$ rise time	t_r	—	30	ns	
$\overline{WE}$ fall time	t_f	—	30	ns	

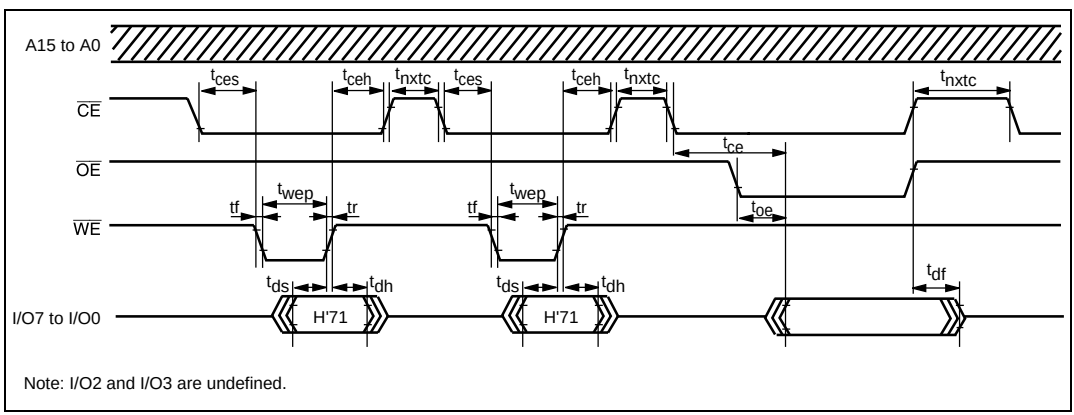


Figure 6.19 Timing Waveforms in Status Read Mode

8.8.1 Port Data Register A (PDRA)

PDRA is a register that stores data of port A.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved The initial value should not be changed.
3	PA3	0	R/W	If port A is read while PCRA bits are set to 1, the values stored in PDRA are read, regardless of the actual pin states. If port A is read while PCRA bits are cleared to 0, the pin states are read.
2	PA2	0	R/W	
1	PA1	0	R/W	
0	PA0	0	R/W	

8.8.2 Port Control Register A (PCRA)

PCRA controls whether each of the port A pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved The initial value should not be changed.
3	PCRA3	0	W	Setting a PCRA bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCRA and in PDRA are valid only when the corresponding pin is designated in LPCR as a general I/O pin. PCRA is a write-only register. Bits 3 to 0 are always read as 1.
2	PCRA2	0	W	
1	PCRA1	0	W	
0	PCRA0	0	W	

When TCF overflows, OVFH is set. OVFL is set if the setting conditions are satisfied when the lower 8 bits overflow. If a TCFL write and overflow signal output occur simultaneously, the overflow signal is not output.

8-Bit Timer Mode:

- TCFH, OCRFH

  In toggle output, TMOFH pin output is toggled when a compare match occurs. If a TCRF write by a MOV instruction and generation of the compare match signal occur simultaneously, TOLH data is output to the TMOFH pin as a result of the TCRF write.

  If an OCRFH write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, if the written data and the counter value match, a compare match signal will be generated at that point. The compare match signal is output in synchronization with the TCFH clock.

  If a TCFH write and overflow signal output occur simultaneously, the overflow signal is not output.

- TCFL, OCRFL

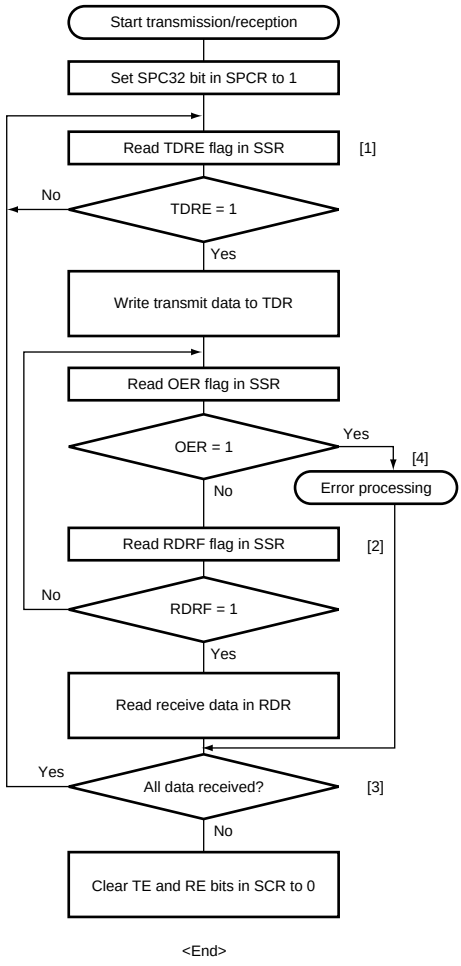
  In toggle output, TMOFL pin output is toggled when a compare match occurs. If a TCRF write by a MOV instruction and generation of the compare match signal occur simultaneously, TOLL data is output to the TMOFL pin as a result of the TCRF write.

  If an OCRFL write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, if the written data and the counter value match, a compare match signal will be generated at that point. As the compare match signal is output in synchronization with the TCFL clock, a compare match will not result in compare match signal generation if the clock is stopped.

  If a TCFL write and overflow signal output occur simultaneously, the overflow signal is not output.

Clear Timer FH, Timer FL Interrupt Request Flags (IRRTFH, IRRTFL), Timer Overflow Flags H, L (OVFH, OVFL), and Compare Match Flags H, L (CMFH, CMFL): When $\phi_w/4$ is selected as the internal clock, “Interrupt source generation signal” will be operated with ϕ_w and the signal will be outputted with ϕ_w width. And, “Overflow signal” and “Compare match signal” are controlled with 2 cycles of ϕ_w signals. Those signals are outputted with 2 cycles width of ϕ_w (figure 9.6)

In active (high-speed, medium-speed) mode, even if you cleared interrupt request flag during the term of validity of “Interrupt source generation signal”, same interrupt request flag is set. (1 in figure 9.6) And, the timer overflow flag and compare match flag cannot be cleared during the term of validity of “Overflow signal” and “Compare match signal”.



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR.
When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial transmission/ reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Transmission/reception cannot be resumed if the OER flag is set to 1. For overrun error processing, see figure 10.13.

Figure 10.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations (Clocked Synchronous Mode)

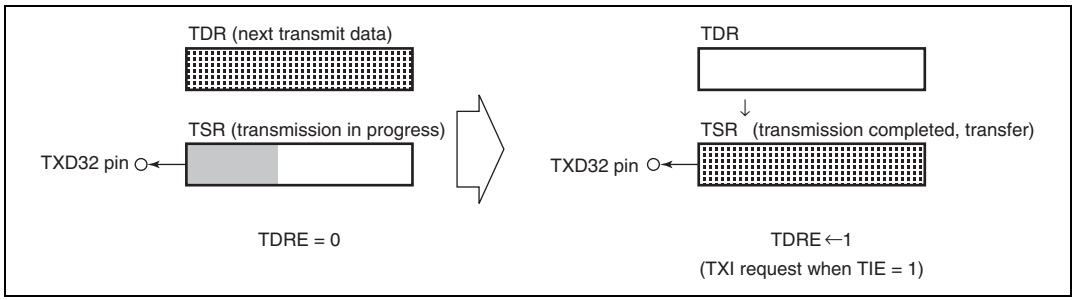


Figure 10.15(b) TDRE Setting and TXI Interrupt

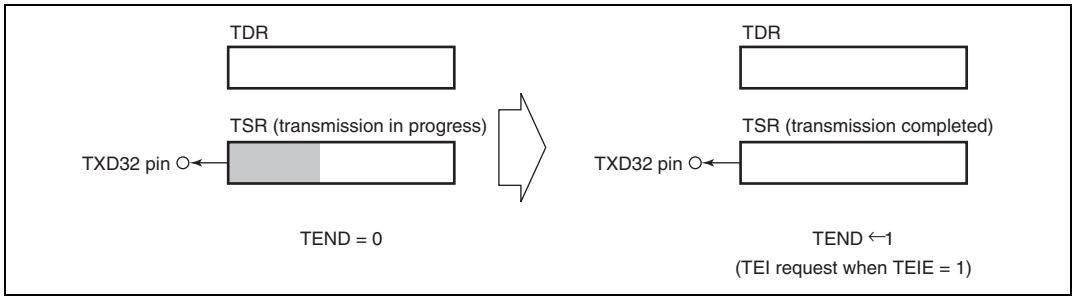


Figure 10.15(c) TEND Setting and TEI Interrupt

10.7 Usage Notes

10.7.1 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RXD32 pin value directly. In a break, the input from the RXD32 pin becomes all 0, setting the FER flag, and possibly the PER flag. Note that as the SCI3 continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

10.7.2 Mark State and Break Sending

When TE is 0, the TXD32 pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD32 pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TXD32 pin becomes an I/O port, and 1 is output from the TXD32 pin. To send a break during serial transmission, first set PCR to 1 and PDR to 0, and then clear TE to 0. When TE is cleared to 0, the

10.7.6 Relation between Writing to TDR and Bit TDRE

Bit TDRE in the serial status register (SSR) is a status flag that indicates that data for serial transmission has not been prepared in TDR. When data is written to TDR, bit TDRE is cleared to 0 automatically. When the SCI3 transfers data from TDR to TSR, bit TDRE is set to 1.

Data can be written to TDR irrespective of the state of bit TDRE, but if new data is written to TDR while bit TDRE is cleared to 0, the data previously stored in TDR will be lost if it has not yet been transferred to TSR. Accordingly, to ensure that serial transmission is performed dependably, you should first check that bit TDRE is set to 1, then write the transmit data to TDR only once (not two or more times).

10.7.7 Relation between RDR Reading and bit RDRF

In a receive operation, the SCI3 continually checks the RDRF flag. If bit RDRF is cleared to 0 when reception of one frame ends, normal data reception is completed. If bit RDRF is set to 1, this indicates that an overrun error has occurred.

When the contents of RDR are read, bit RDRF is cleared to 0 automatically. Therefore, if RDR is read more than once, the second and subsequent read operations will be performed while bit RDRF is cleared to 0. Note that, when an RDR read is performed while bit RDRF is cleared to 0, if the read operation coincides with completion of reception of a frame, the next frame of data may be read. This is shown in figure 10.17.

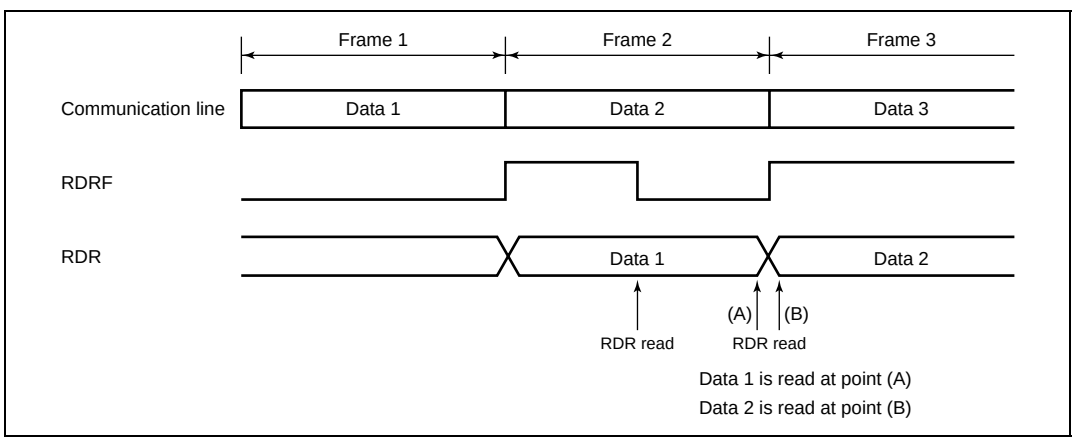


Figure 10.17 Relation between RDR Read Timing and Data

In this case, only a single RDR read operation (not two or more) should be performed after first checking that bit RDRF is set to 1. If two or more reads are performed, the data read the first time

12.2 Input/Output Pins

Table 12.1 shows the input pins used by the A/D converter.

Table 12.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
Analog power supply pin	AVcc	Input	Power supply and reference voltage of analog part
Analog ground pin	AVss	Input	Ground and reference voltage of analog part
Analog input pin 0	AN0	Input	Analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	

12.3 Register Descriptions

The A/D converter has the following registers.

- A/D result registers H and L (ADRRH and ADRRL)
- A/D mode register (AMR)
- A/D start register (ADSR)

12.3.1 A/D Result Registers H and L (ADRRH and ADRRL)

ADRRH and ADRRL are 16-bit read-only registers that store the results of A/D conversion.

The upper 8 bits of the data are stored in ADRRH, and the lower 2 bits in ADRRL.

ADRRH and ADRRL can be read by the CPU at any time, but the ADRRH and ADRRL values during A/D conversion are undefined. After A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion operation starts.

The initial values of ADRRH and ADRRL are undefined.

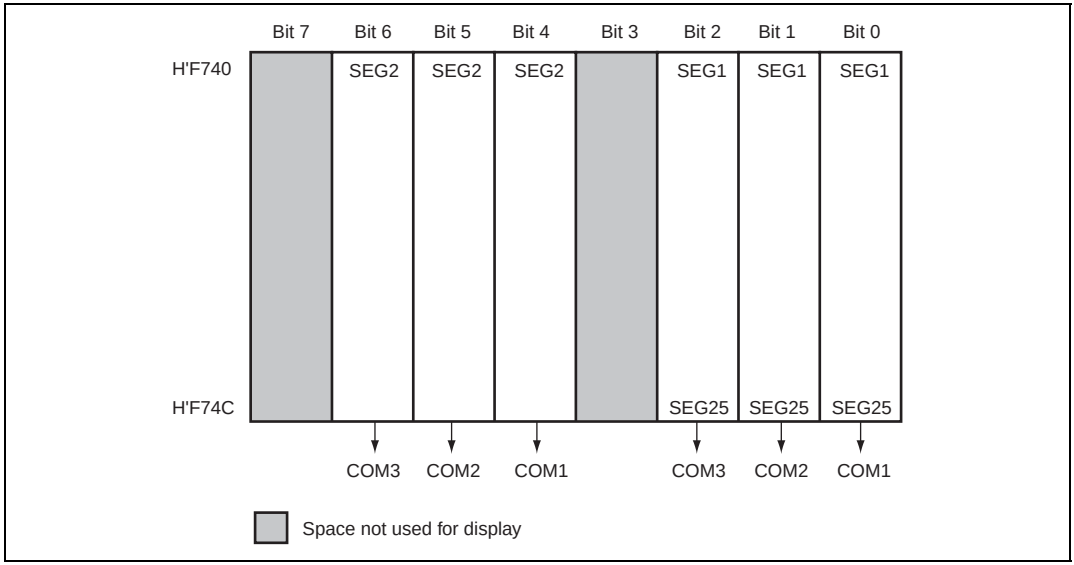


Figure 13.4 LCD RAM Map (1/3 Duty)

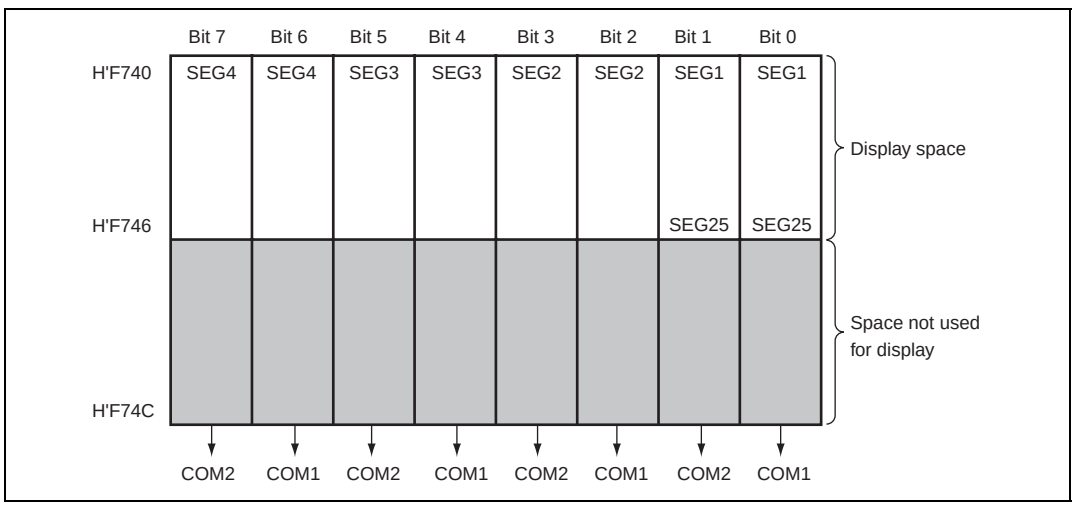


Figure 13.5 LCD RAM Map (1/2 Duty)

14.2.2 Low-Voltage Detection Status Register (LVDSR)

LVDSR is used to control external input selection, indicates when the reference voltage is stable, and indicates if the power supply voltage goes below or above a specified range.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0*	R/W	LVD Reference Voltage Stabilized Flag Setting condition: When the low-voltage detection counter (LVDCNT) overflows Clearing condition: When 0 is written after reading 1
6 to 4	—	All 0	R/W	These are read/write enabled reserved bits.
3	VREFSEL	0	R/W	Reference Voltage External Input Select 0: The on-chip circuit is used to generate the reference voltage 1: The reference voltage is input to the Vref pin from an external source
2	—	0	R/W	This bit is reserved. It is always read as 0 and cannot be written to.
1	LVDDF	0*	R/W	LVD Power Supply Voltage Drop Flag Setting condition: When the power supply voltage drops below Vint(D) Clearing condition: When 0 is written after reading 1
0	LVDUF	0*	R/W	LVD Power Supply Voltage Rise Flag Setting condition: When the power supply voltage drops below Vint(D) while the LVDUE bit in LVDCR is set to 1, and it rises above Vint(U) before dropping below Vreset1 Clearing condition: When 0 is written after reading 1

Note: * These bits are initialized by resets trigged by LVDR.

Resistance Value Calculation Table

Ex. No	Vref (V)	R (kΩ)	Vreset1	Vint(D)	Vint(U)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
1	1.30	1000	2.5	2.7	2.9	517	33	450
2	1.41	1000	2.7	2.9	3	514	16	470
3	1.57	1000	3	3.2	3.5	511	42	447
4	2.09	1000	4	4.5	4.7	536	20	444

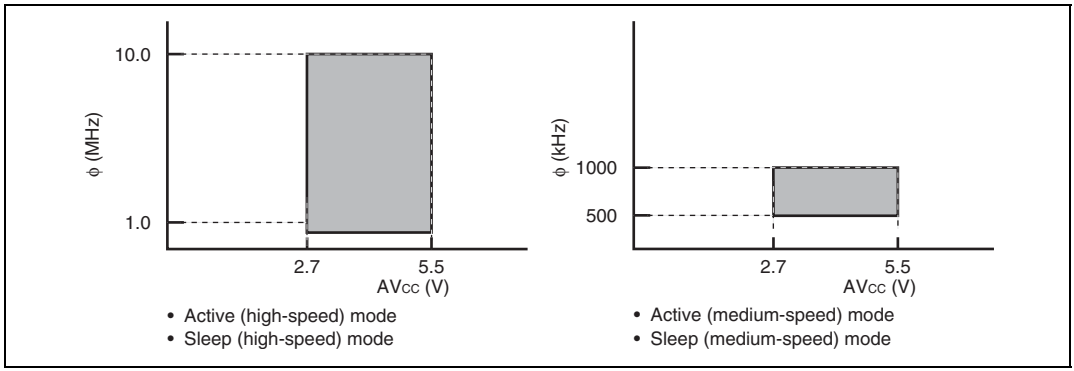
4. Using an error calculation table like the one shown below, plug in values for R1, R2, R3, and Vref to calculate the deviation of Vreset1, Vint(D), and Vint(U). Make sure to double check the maximum and minimum values for each value.

Error Calculation Table

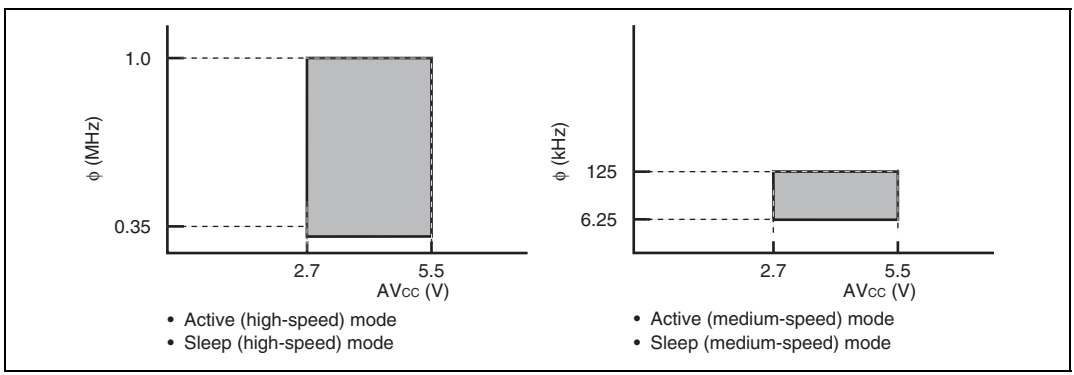
Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Resistance Value Error (%) 5	Comparator Error (V)	Vreset1 (V)	Vint(D) (V)	Vint(U) (V)
1.3	517	33	450	R1+Err, R2/R3-Err	0.1	2.59	2.94	3.15
					0	2.49	2.84	3.05
					-0.1	2.39	2.74	2.95
				R1-Err, R2/R3+Err	0.1	2.59	2.66	2.85
					0	2.49	2.56	2.75
					-0.1	2.39	2.46	2.65
				R1/R2/R3 No Err	0.1	2.59	2.79	2.99
					0	2.49	2.69	2.89
					-0.1	2.39	2.59	2.79
				R1/R2+Err, R3-Err	0.1	2.59	2.93	3.16
					0	2.49	2.83	3.06
					-0.1	2.39	2.73	2.96
				R1/R2-Err, R3+Err	0.1	2.59	2.67	2.84
					0	2.49	2.57	2.74
					-0.1	2.39	2.47	2.64

Notes: 1. AEC: Asynchronous event counter
2. WDT: Watchdog timer
3. LCD: LCD controller/driver
4. H8/38104 Group only

Analog Power Supply Voltage and A/D Converter Operating Range (System Clock Oscillator Selected)



Analog Power Supply Voltage and A/D Converter Operating Range (On-Chip Oscillator Selected)



Appendix A Instruction Set

A.1 Instruction List

Operation Notation

Symbol	Description
Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx:3/8/16	Immediate data (3, 8, or 16 bits)
d:8/16	Displacement (8 or 16 bits)
@aa:8/16	Absolute address (8 or 16 bits)
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
¬	Logical complement

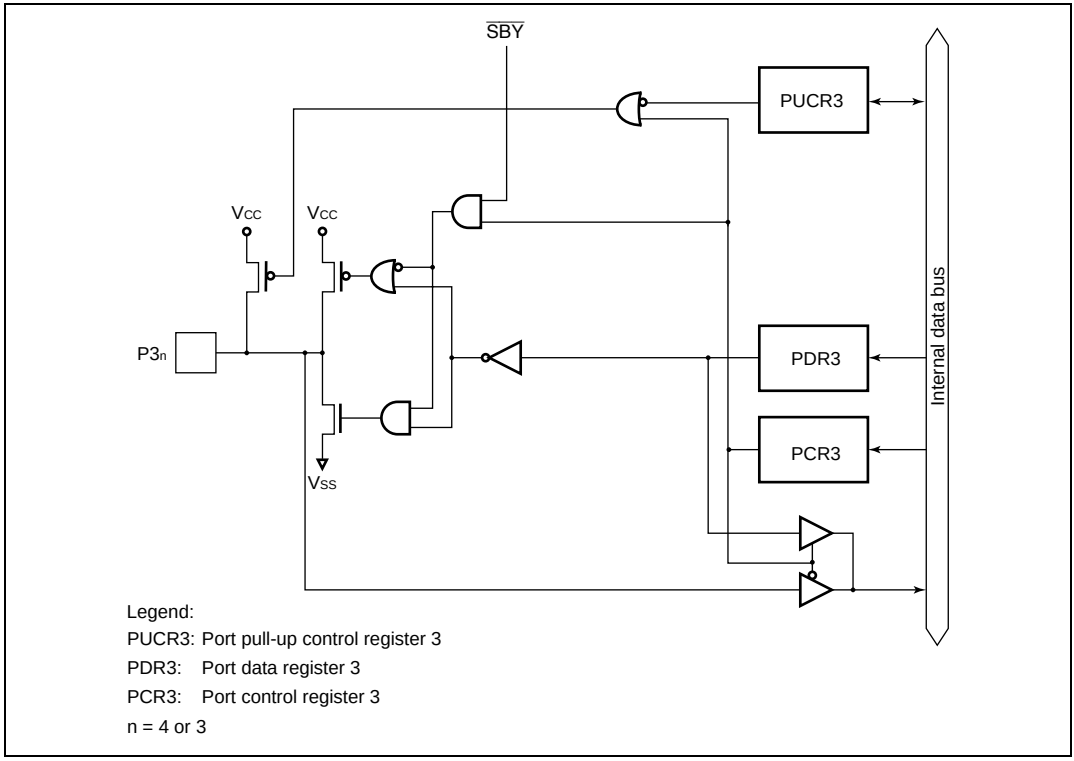
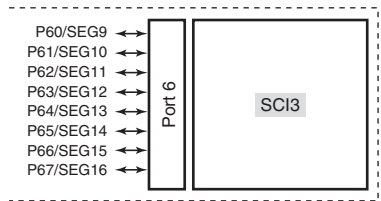


Figure B.1(c) Port 3 Block Diagram (Pins P34 and P33)

Main Revisions for This Edition

Item	Page	Revisions (See Manual for Details)
1.1 Features	3	Table amended **Package** / **Code** / **Body Size** / **Pin Pitch** QFP-64 / FP-64A / 14.0 × 14.0 mm / 0.8 mm LQFP-64 / FP-64E / 10.0 × 10.0 mm / 0.5 mm LQFP-64 / FP-64K* / 10.0 ×10.0 mm / 0.5 mm P-VQFN-64 / TNP-64B / 8.0 × 8.0 mm / 0.4 mm DP-64S / DP-64S / 17.0 × 57.6 mm / 1.0 mm Die / — / — / — Note amended Note: * The package dimensions of the FP-64K and FP-64E differ. For details, see appendix E, Package Dimensions.
1.2 Internal Block Diagram Figure 1.1 Internal Block Diagram of H8/3802 Group	4	Figure amended 
Figure 1.2 Internal Block Diagram of H8/38004 and H8/38002S Group	5	Figure title amended