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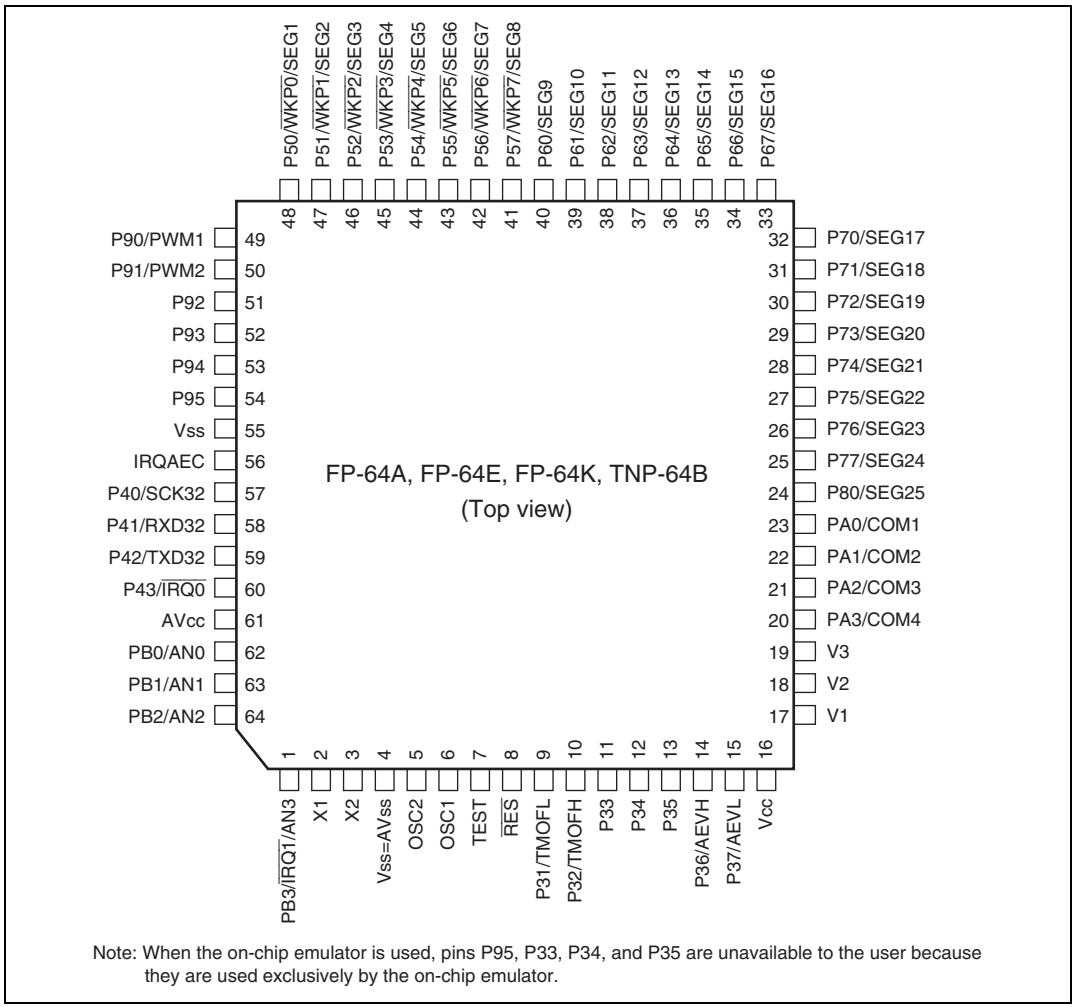
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38104fpwv

1.3 Pin Arrangement



Note: When the on-chip emulator is used, pins P95, P33, P34, and P35 are unavailable to the user because they are used exclusively by the on-chip emulator.

Figure 1.4 Pin Arrangement of H8/3802, H8/38004 and H8/38002S Group (FP-64A, FP-64E, FP-64K, TNP-64B)

Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)	Pad No.	Pad Name	Coordinate X (μm)	Coordinate Y (μm)
63	PB0/AN0	-1170	1742	65	PB2/AN2	-1578	1742
64	PB1/AN1	-1400	1742				

Note: The power supply (Vss) pads in pad numbers 4, 5, and 56 must not be open but connected. The TEST pad in pad number 8 must be connected to the Vss voltage level. If not, this LSI does not operate correctly. The coordinate values indicate center positions of pads and the accuracy is ±5 μm. The home-point position is center of the chip and the center is located at half the distance between the upper and lower pads and left and right pads.

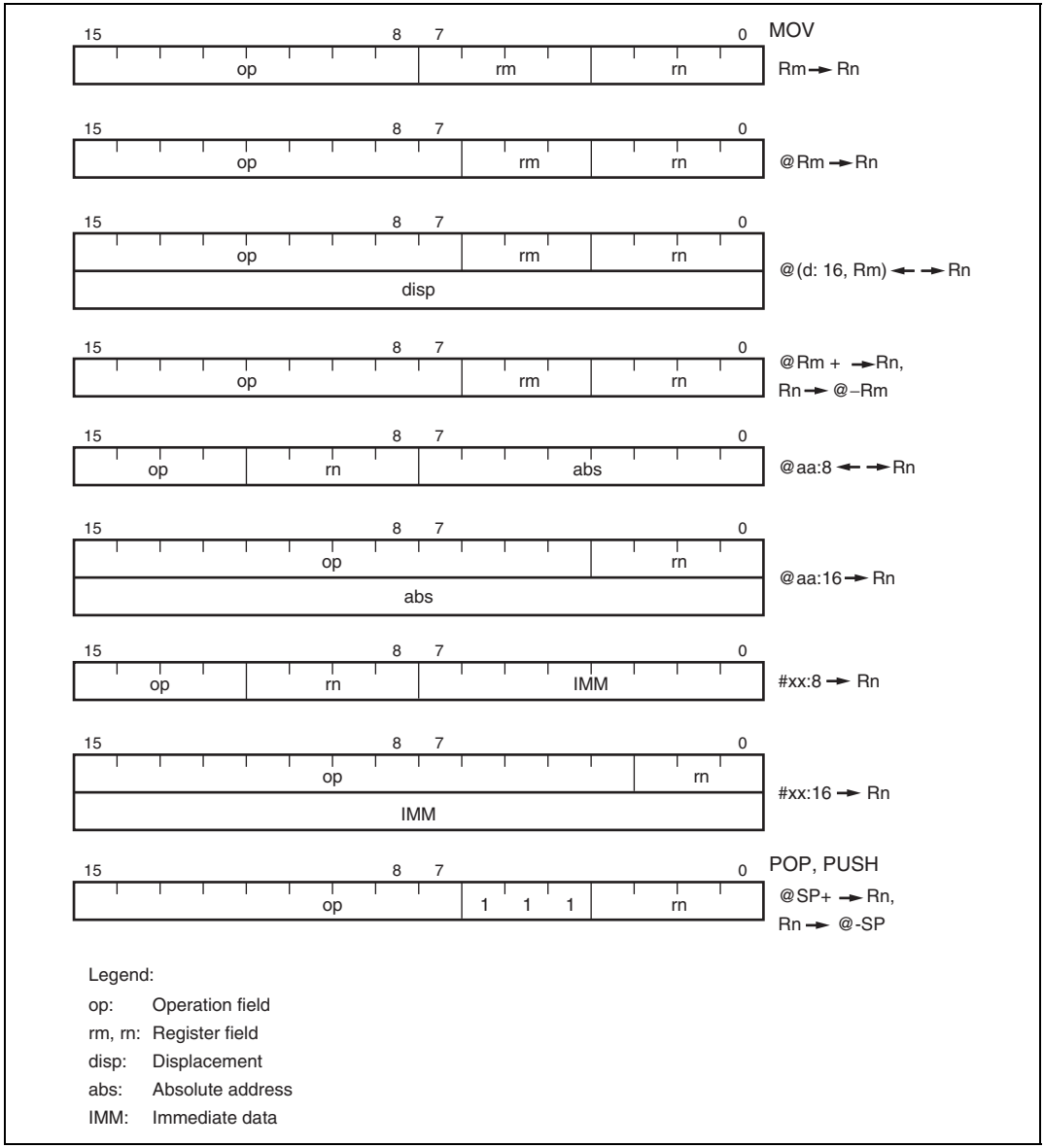


Figure 2.6 Instruction Formats of Data Transfer Instructions

No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
5	Absolute address @aa:8 15 8 7 0 op abs @aa:16 15 0 op abs		15 8 7 0 H'FF 15 0
6	Immediate #xx:8 15 8 7 0 op IMM #xx:16 15 0 op IMM		Operand is 1- or 2-byte immediate data
7	Program-counter relative@ (d: 8, PC) 15 8 7 0 op disp	15 0 PC contents Sign extension disp	15 0

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	—
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	1	1

BCLR instruction executed

```
BCLR   #1,    @RAM0
```

The BCLR instructions executed for the PCR3 work area (RAM0).

After executing BCLR

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR3
```

The work area (RAM0) value is written to PCR3.

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	High level	—
PCR3	0	0	1	1	1	1	0	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	0	1

Table 6.7 Oscillation Frequencies for which Automatic Adjustment of LSI Bit Rate Is Possible (f_{osc})

Product Group	Host Bit Rate	Oscillation Frequency Range of LSI (f_{osc})
H8/38004F Group	4,800 bps	8 to 10 MHz
	2,400 bps	4 to 10 MHz
	1,200 bps	2 to 10 MHz
H8/38104F Group	19,200 bps	16 to 20 MHz
	9,600 bps	8 to 20 MHz
	4,800 bps	4 to 20 MHz
	2,400 bps	2 to 20 MHz
	1,200 bps	2 to 20 MHz

6.7.2 Programming/Erasing in User Program Mode

User program mode means the execution state of the user program. On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 6.9 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 6.8, Flash Memory Programming/Erasing.

8.1.4 Port Mode Register 3 (PMR3)

PMR3 controls the selection of pin functions for port 3 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	AEVL	0	R/W	P37/AEVL Pin Function Switch This bit selects whether pin P37/AEVL is used as P37 or as AEVL. 0: P37 I/O pin 1: AEVL input pin
6	AEVH	0	R/W	P36/AEVH Pin Function Switch This bit selects whether pin P36/AEVH is used as P36 or as AEVH. 0: P36 I/O pin 1: AEVH input pin
5 to 3	—	—	W	Reserved The write value should always be 0.
2	TMOFH	0	R/W	P32/TMOFH Pin Function Switch This bit selects whether pin P32/TMOFH is used as P32 or as TMOFH. 0: P32 I/O pin 1: TMOFH output pin
1	TMOFL	0	R/W	P31/TMOFL Pin Function Switch This bit selects whether pin P31/TMOFL is used as P31 or as TMOFL. 0: P31 I/O pin 1: TMOFL output pin
0	—	—	W	Reserved The write value should always be 0.

8.2 Port 4

Port 4 is an I/O port also functioning as an interrupt input pin and SCI I/O pin. Figure 8.2 shows its pin configuration.

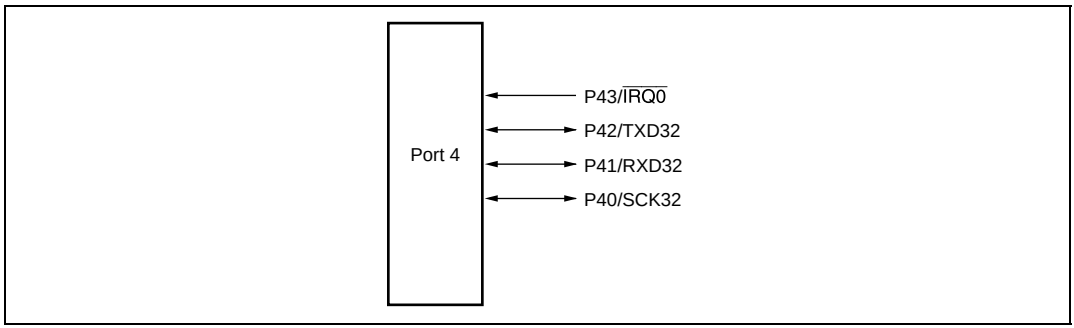


Figure 8.2 Port 4 Pin Configuration

Port 4 has the following registers.

- Port data register 4 (PDR4)
- Port control register 4 (PCR4)
- Serial port control register (SPCR)

8.2.1 Port Data Register 4 (PDR4)

PDR4 is a register that stores data of port 4.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	P43	1	R	If port 4 is read while PCR4 bits are set to 1, the values stored in PDR4 are read, regardless of the actual pin states. If port 4 is read while PCR4 bits are cleared to 0, the pin states are read.
2	P42	0	R/W	
1	P41	0	R/W	
0	P40	0	R/W	

8.2.2 Port Control Register 4 (PCR4)

PCR4 controls whether each of the port 4 pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	PCR42	0	W	Setting a PCR4 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR4 and in PDR4 are valid only when the corresponding pin is designated in SCR3 and SCR2 as a general I/O pin. PCR4 is a write-only register. Bits 2 to 0 are always read as 1.
1	PCR41	0	W	
0	PCR40	0	W	

8.2.3 Serial Port Control Register (SPCR)

SPCR performs input/output data inversion switching of the RXD32 and TXD32 pins. Figure 8.3 shows the configuration.

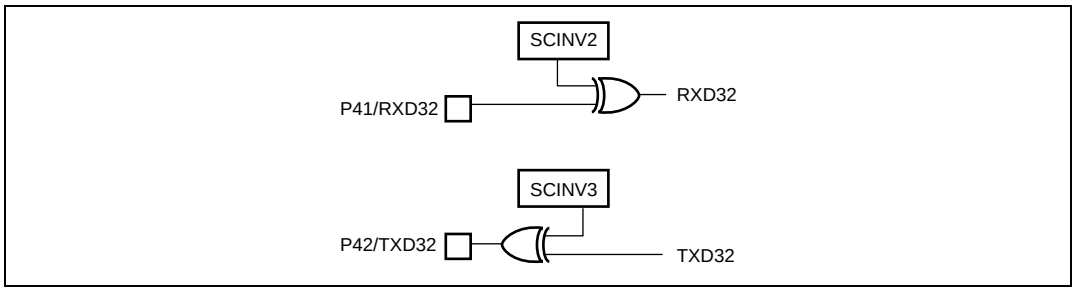


Figure 8.3 Input/Output Data Inversion Function

8.4.3 Port Pull-Up Control Register 6 (PUCR6)

PUCR6 controls whether the pull-up MOS of each of the port 6 pins is on or off.

Bit	Bit Name	Initial Value	R/W	Description
7	PUCR67	0	R/W	When a PCR6 bit is cleared to 0, setting the corresponding PUCR6 bit to 1 turns on the pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.
6	PUCR66	0	R/W	
5	PUCR65	0	R/W	
4	PUCR64	0	R/W	
3	PUCR63	0	R/W	
2	PUCR62	0	R/W	
1	PUCR61	0	R/W	
0	PUCR60	0	R/W	

8.4.4 Pin Functions

The port 6 pin functions are shown below.

- P67/SEG16 to P64/SEG13 pins

The pin function depends on the combination of bit PCR6n in PCR6 and bits SGS3 to SGS0 in LPCR.

(n = 7 to 4)

SGS3 to SGS0	Other than B′0100, B′0101, B′0110, B′0111, B′1000, B′1001, B′1010, B′1011		B′0100, B′0101, B′0110, B′0111, B′1000, B′1001, B′1010, B′1011
PCR6n	0	1	*
Pin Function	P6n input pin	P6n output pin	SEGn+9 output pin

Legend: *: Don't care.

Timer Control Status Register F (TCSRF): TCSRF performs counter clear selection, overflow flag setting, and compare match flag setting, and controls enabling of overflow interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	OVFH	0	R/W*	Timer Overflow Flag H [Setting condition] When TCFH overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVFH = 1
6	CMFH	0	R/W*	Compare Match Flag H This is a status flag indicating that TCFH has matched OCRFH. [Setting condition] When the TCFH value matches the OCRFH value [Clearing condition] When this bit is written to 0 after reading CMFH = 1
5	OVIEH	0	R/W	Timer Overflow Interrupt Enable H Selects enabling or disabling of interrupt generation when TCFH overflows. 0: TCFH overflow interrupt request is disabled 1: TCFH overflow interrupt request is enabled
4	CCLRH	0	R/W	Counter Clear H In 16-bit mode, this bit selects whether TCF is cleared when TCF and OCRF match. In 8-bit mode, this bit selects whether TCFH is cleared when TCFH and OCRFH match. In 16-bit mode: 0: TCF clearing by compare match is disabled 1: TCF clearing by compare match is enabled In 8-bit mode: 0: TCFH clearing by compare match is disabled 1: TCFH clearing by compare match is enabled

transmitter is initialized regardless of the current transmission state, the TXD32 pin becomes an I/O port, and 0 is output from the TXD32 pin.

10.7.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

10.7.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 10.16.

Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ \left(0.5 - \frac{1}{2N}\right) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

Where N : Ratio of bit rate to clock (N = 16)
D : Clock duty (D = 0.5 to 1.0)
L : Frame length (L = 9 to 12)
F : Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

Section 11 10-Bit PWM

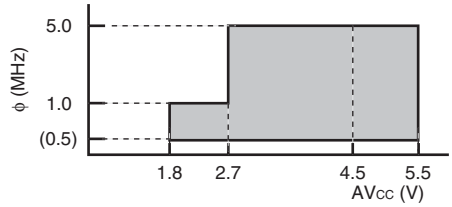
This LSI has a two-channel 10-bit PWM. The PWM with a low-path filter connected can be used as a D/A converter. Figure 11.1(1) shows a block diagram of the 10-bit PWM of the H8/3802 Group, H8/38004 Group and H8/38002S Group. Figure 11.1(2) shows a block diagram of the 10-bit PWM of the H8/38104 Group.

11.1 Features

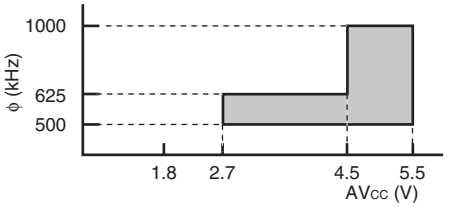
- Choice of four conversion periods

  A conversion period of 4096/ϕ with a minimum modulation width of 4/ϕ, a conversion period of 2048/ϕ with a minimum modulation width of 2/ϕ, a conversion period of 1024/ϕ with a minimum modulation width of 1/ϕ, or a conversion period of 512/ϕ with a minimum modulation width of 1/2ϕ can be selected.
- Pulse division method for less ripple
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 5.4, Module Standby Function.)
- On the H8/38104 Group it is possible to select between two types of PWM output: pulse-division 10-bit PWM and event counter PWM (PWM incorporating AEC). (The H8/3802 Group, H8/38004 Group and H8/38002S Group can only produce 10-bit PWM output.) Refer to section 9.4, Asynchronous Event Counter (AEC), for information on event counter PWM.

Analog Power Supply Voltage and A/D Converter Operating Range



• Active (high-speed) mode
• Sleep (high-speed) mode



• Active (medium-speed) mode
• Sleep (medium-speed) mode

Note: When AVcc = 1.8 V to 2.7 V, the operating range is limited to φ = 1.0 MHz when using a resonator and is φ = 0.5 MHz to 1.0 MHz when using an external clock.

Appendix A Instruction Set

A.1 Instruction List

Operation Notation

Symbol	Description
Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx:3/8/16	Immediate data (3, 8, or 16 bits)
d:8/16	Displacement (8 or 16 bits)
@aa:8/16	Absolute address (8 or 16 bits)
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
¬	Logical complement

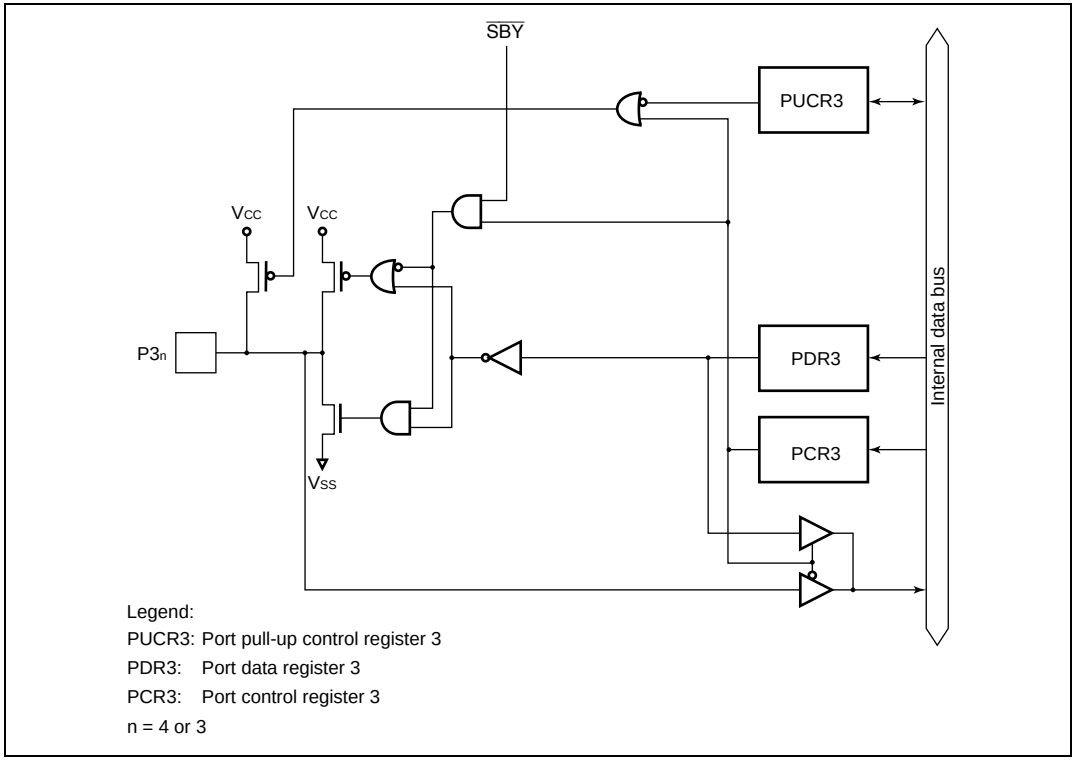
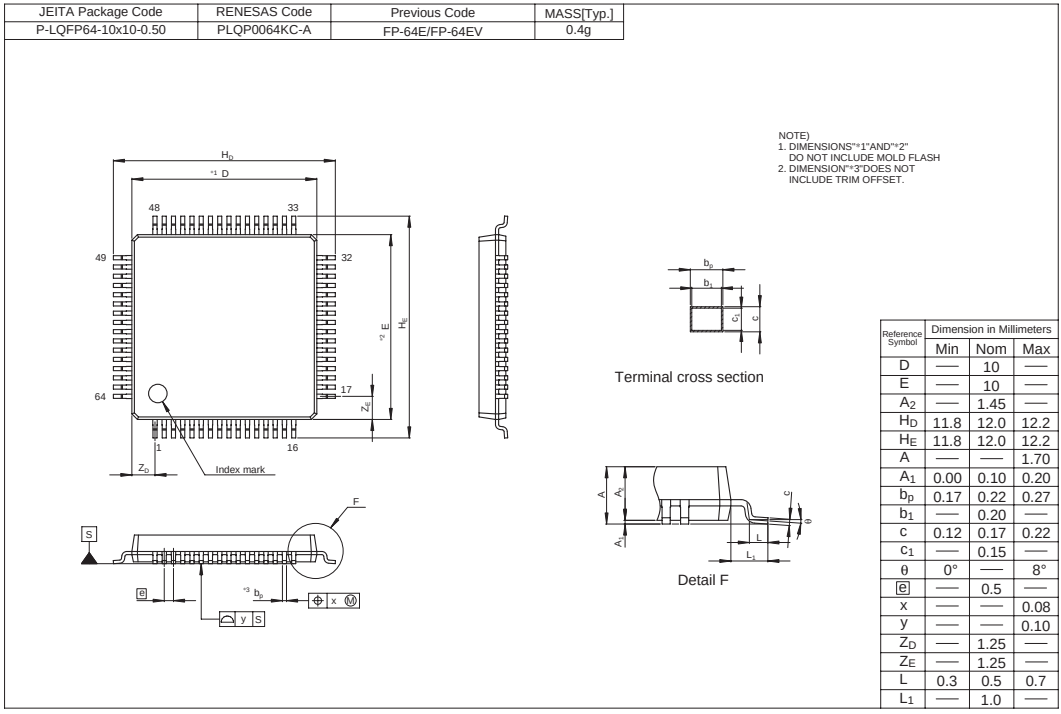


Figure B.1(c) Port 3 Block Diagram (Pins P34 and P33)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KC-A	FP-64E/FP-64EV	0.4g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10	—
E	—	10	—
A_2	—	1.45	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.70
A_1	0.00	0.10	0.20
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure E.2 Package Dimensions (FP-64E)